# HIGH-SPEED CMOS 8-BIT BUT INTERFACE REGISTER TRANSCEIVER

**IDTQS29FCT2052AT/BT/CT**

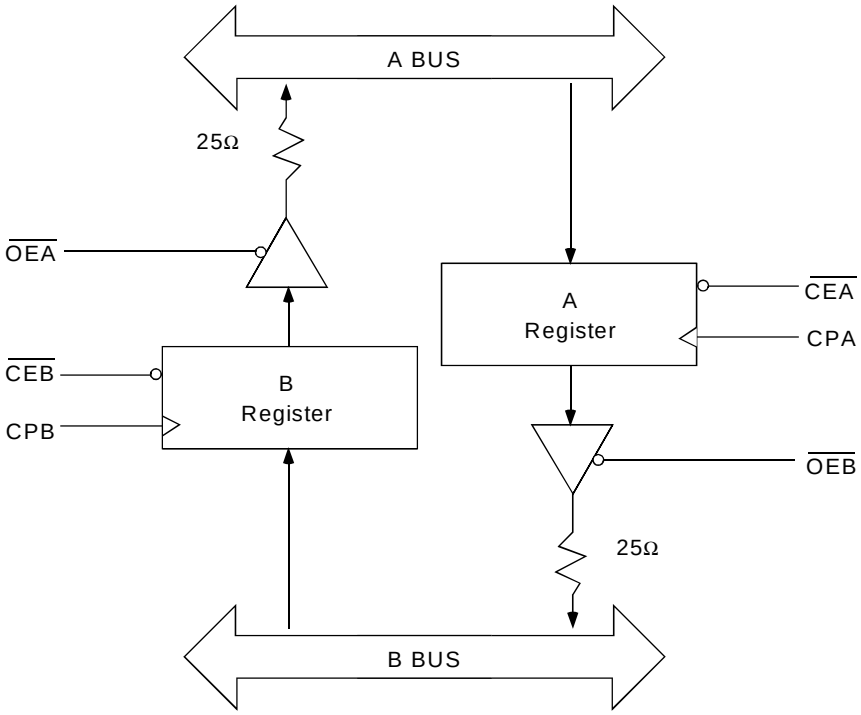
## FEATURES:

- Pin and function compatible to the 29FCT2052 and 29FCT2052/53T
- CMOS power levels: <7.5mW static
- Undershoot clamp diodes on all inputs
- True TTL input and output compatibility
- Ground bounce controlled outputs
- Reduced output swing of 0 to 3.5V
- Built-in 25Ω series resistor outputs reduce reflection and other system noise
- A, B, and C speed grades with 5.8ns $t_{PD}$ for C speed guaranteed with 50pF loads
- Available in SOIC and QSOP packages

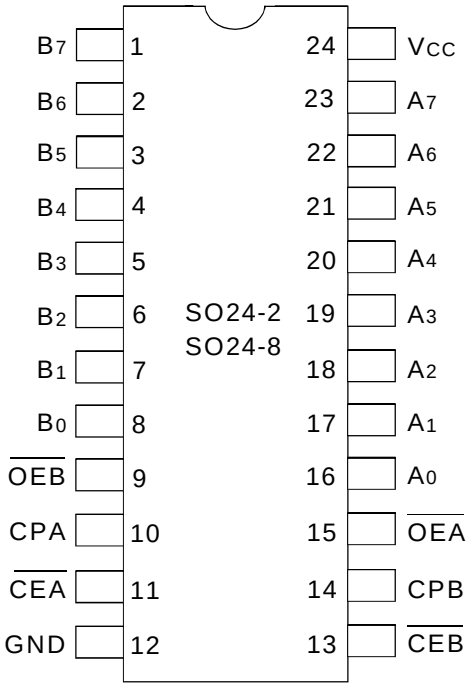
## DESCRIPTION:

The QS29FCT2052T is an 8-bit, high-speed, CMOS TTL-compatible, registered bus transceiver with 3-state outputs and a 25Ω resistor, useful for driving transmission lines and reducing system noise. The QS29FCT2052 series part can replace the FCT52 series to reduce noise in an existing design. All outputs have clamp diodes for undershoot noise suppression. All outputs have ground bounce suppression. Outputs will not load an active bus when Vcc is removed from the device.

## FUNCTIONAL BLOCK DIAGRAM



## PIN CONFIGURATION




**SOIC/ QSOP**
**TOP VIEW**

## PIN DESCRIPTION

| Name | I/O | Description |
|---|---|---|
| Ax | I/O | A Bus |
| Bx | I/O | B Bus |
| CPA | I | Register A Clock Input |
| CPB | I | Register B Clock Input |
| $\overline{CEA}$ | I | Register A Clock Enable |
| $\overline{CEB}$ | I | Register B Clock Enable |
| $\overline{OEA}$ | I | Output Enable, Reg. B to Bus A |
| $\overline{OEB}$ | I | Output Enable, Reg. A to Bus B |

## ABSOLUTE MAXIMUM RATINGS (1)

| Symbol | Description | Max. | Unit |
|---|---|---|---|
| $V_{TERM}$ | Terminal Voltage with Respect to GND | – 0.5 to +7 | V |
| $T_{STG}$ | Storage Temperature | – 65 to +150 | °C |
| $I_{OUT}$ | DC Output Current Max Sink Current/Pin | 120 | mA |
| $I_{IK}$ | Input Diode Current, $V_{IN}$ < 0 | – 20 | mA |
| $I_{OK}$ | Output Diode Current, $V_{OUT}$ < 0 | – 50 | mA |

FCTL

**NOTE:**
1. Stresses greater than those listed under ABSOLUTE MAXIMUM RATINGS may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect reliability.

## CAPACITANCE ($T_A$ = +25°C, f = 1.0MHz)

| Symbol | Parameter(1) | Conditions | Typ. | Max. | Unit |
|---|---|---|---|---|---|
| $C_{IN}$ | Input Capacitance | $V_{IN}$ = 0V | 8 | — | pF |
| $C_{OUT}$ | Output Capacitance | $V_{OUT}$ = 0V | 8 | — | pF |

FCT_1

**NOTE:**
1. This parameter is measured at characterization but not tested.

## FUNCTION TABLES (1)

| Inputs | | | | Outputs | |
|---|---|---|---|---|---|
| CPA | CPB | $\overline{CEA}$ | $\overline{CEB}$ | Ax | Bx |
| X | X | H | H | Hold | Hold |
| ↑ | X | L | H | Load | Hold |
| X | ↑ | H | L | Hold | Load |
| X | ↑ | L | L | X | Load |
| ↑ | X | L | L | Load | X |

| Inputs | | | | | | Outputs | |
|---|---|---|---|---|---|---|---|
| CPA | CPB | $\overline{CEA}$ | $\overline{CEB}$ | $\overline{OEA}$ | $\overline{OEB}$ | Ax | Bx |
| X | X | X | X | H | L | Z | Reg. A |
| X | X | X | X | L | H | Reg. B | Z |
| X | X | X | X | H | H | Z | Z |
| X | X | X | X | L | L | Reg. B | Reg. A |

**NOTE:**
1. H = HIGH Voltage Level
   L = LOW Voltage Level
   X = Don't Care
   Z = High-Impedence
   ↑ = LOW-to-HIGH Transition

# DC ELECTRICAL CHARACTERISTICS OVER OPERATING RANGE

**Following Conditions Apply Unless Otherwise Specified:**
**Industrial: $T_A$ = -40°C to +85°C, $V_{CC}$ = 5.0V ± 5%**

| Symbol | Parameter | Test Conditions | | Min. | Typ.(1) | Max. | Unit |
|---|---|---|---|---|---|---|---|
| $V_{IH}$ | Input HIGH Level | Guaranteed Logic HIGH Level | | 2 | — | — | V |
| $V_{IL}$ | Input LOW Level | Guaranteed Logic LOW Level | | — | — | 0.8 | V |
| $\Delta V_T$ | Input Hysteresis | $V_{TLH}$ - $V_{THL}$ for all inputs | | — | 0.2 | — | V |
| $I_{IH}$ | Input HIGH Current | $V_{CC}$ = Max. | 0 ≤ $V_{IN}$ < Vcc | — | — | ±5 | µA |
| $I_{IL}$ | Input LOW Current | | | | | | |
| $I_{OZ}$ | Off-State Output Current (Hi-Z) | $V_{CC}$ = Max. | 0 ≤ $V_{IN}$ ≤ Vcc | — | — | ±5 | µA |
| $I_{OR}$ | Current Drive | $V_{CC}$ = Max., $V_{OUT}$ = 2.0V(2) | | 50 | — | — | mA |
| $V_{IC}$ | Input Clamp Voltage | $V_{CC}$ = Min., $I_{IN}$ = –18mA, $T_A$ = 25°C(2) | | — | –0.7 | –1.2 | V |
| $V_{OH}$ | Output HIGH Voltage | $V_{CC}$ = Min. | $I_{OH}$ = -15mA | 2.4 | — | — | V |
| $V_{OL}$ | Output LOW Voltage | $V_{CC}$ = Min. | $I_{OL}$ = 12mA | — | — | 0.5 | V |
| $R_{OUT}$ | Output Resistance | $V_{CC}$ = Min. | $I_{OL}$ = 12mA | 20 | 28 | 40 | Ω |

**NOTES:**
1. Typical values are at $V_{CC}$ = 5.0V, $T_A$ = 25°C.
2. This parameter is guaranteed but not tested.

# POWER SUPPLY CHARACTERISTICS

**Following Conditions Apply Unless Otherwise Specified:**
**Industrial: $T_A$ = -40°C to +85°C, $V_{CC}$ = 5.0V ± 5%**

| Symbol | Parameter | Test Conditions(1) | Min. | Max. | Unit |
|---|---|---|---|---|---|
| $I_{CC}$ | Quiescent Power Supply Current | $V_{CC}$ = Max.<br>freq = 0<br>0V ≤ $V_{IN}$ ≤ 0.2V or<br>Vcc-0.2V ≤ $V_{IN}$ ≤ Vcc | — | 1.5 | mA |
| $\Delta I_{CC}$ | Supply Current per Input TTL Inputs HIGH | $V_{CC}$ = Max.<br>$V_{IN}$ = 3.4V(2)<br>freq = 0 | — | 2 | mA |
| $I_{CCD}$ | Supply Current per Input per MHz | $V_{CC}$ = Max.<br>Outputs Open and Enabled<br>One Bit Toggling<br>50% Duty Cycle<br>Other inputs at GND or Vcc(3,4) | — | 0.25 | mA/MHz |

FCTL

**NOTES:**
1. For conditions shown as Min. or Max., use the appropriate values specified under DC Electrical Characteristics.
2. Per TLL driven input ($V_{IN}$ = 3.4V).
3. For flip-flops, $I_{CCD}$ is measured by switching one of the data input pins so that the output changes every clock cycle. This is a measurement of device power consumption only and does not include power to drive load capacitance or tester capacitance.
4. $I_C = I_{QUIESCENT} + I_{INPUTS} + I_{DYNAMIC}$
   $I_C = I_{CC} + \Delta I_{CC} D_H N_T + I_{CCD} (f_{CP}/2 + f_i N_i)$
   $I_{CC}$ = Quiescent Current
   $\Delta I_{CC}$ = Power Supply Current for a TTL High Input ($V_{IN}$ = 3.4V)
   $D_H$ = Duty Cycle for TTL Inputs High
   $N_T$ = Number of TTL Inputs at $D_H$
   $I_{CCD}$ = Dynamic Current Caused by an Output Transition Pair (HLH or LHL)
   $f_{CP}$ = Clock Frequency for Register Devices (Zero for Non-Register Devices)
   $f_i$ = Input Frequency
   $N_i$ = Number of Inputs at $f_i$
   All currents are in milliamps and all frequencies are in megahertz.

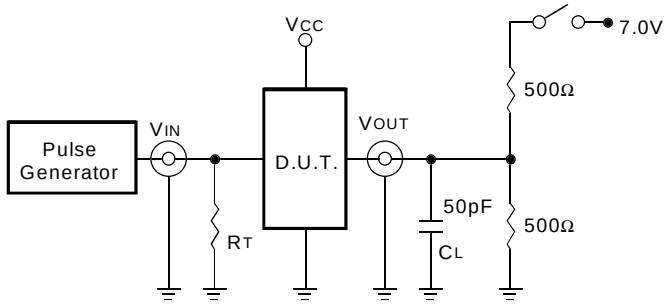
# SWITCHING CHARACTERISTICS OVER OPERATING RANGE(1)

| Symbol | Parameter | 29FCT2052AT | | 29FCT2052BT | | 29FCT2052CT | | Unit |
|---|---|---|---|---|---|---|---|---|
| | | Min. | Max. | Min. | Max. | Min. | Max. | |
| $t_{PHL}$<br>$t_{PLH}$ | Propagation Delay(2)<br>CP to Ax, Bx | 2 | 10 | 2 | 6.5 | 2 | 5.8 | ns |
| $t_{PZH}$<br>$t_{PZL}$ | Output Enable Time(2)<br>$\overline{OE}$ to Ax, Bx | 1.5 | 10.5 | 1.5 | 7 | 1.5 | 7 | ns |
| $t_{PHZ}$<br>$t_{PLZ}$ | Output Disable Time(2,3)<br>$\overline{OE}$ to Ax, Bx | 2 | 10 | 2 | 5.5 | 1.5 | 5.5 | ns |
| $t_S$ | Data Setup Time<br>Ax, Bx, to CP | 2 | — | 2 | — | 2 | — | ns |
| $t_H$ | Data Hold Time<br>Ax, Bx, to CP | 2 | — | 1.5 | — | 1.5 | — | ns |
| $t_{SCE}$ | Clock Enable Setup Time, $\overline{CE}$ to CP | 2 | — | 2 | — | 2 | — | ns |
| $t_{HCE}$ | Clock Enable Hold Time, $\overline{CE}$ to CP | 2 | — | 2 | — | 2 | — | ns |
| $t_W$ | Clock Pulse Width, HIGH or LOW(3) | 3 | — | 3 | — | 3 | — | ns |

**NOTES:**
1. $C_{LOAD}$ = 50pF, $R_{LOAD}$ = 500Ω unless otherwise noted.
2. Minimums guaranteed but not tested.
3. This parameter is guaranteed by design but not tested.

# TEST CIRCUITS AND WAVEFORMS

## TEST CIRCUITS FOR ALL OUTPUTS




FCTL link

## SWITCH POSITION

| Test | Switch |
|---|---|
| Open Drain<br>Disable Low<br>Enable Low | Closed |
| All Other Tests | Open |

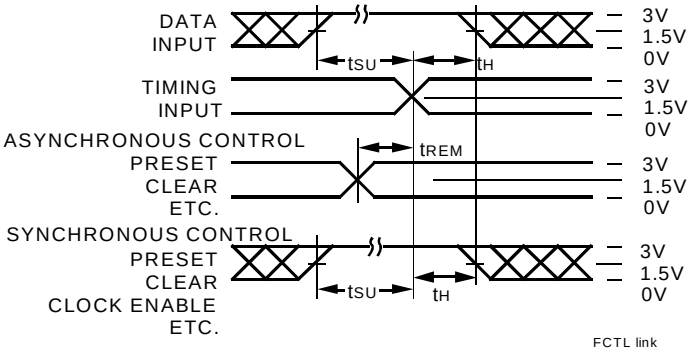
FCTL

**DEFINITIONS:**

$C_L$ = Load capacitance: includes jig and probe capacitance.

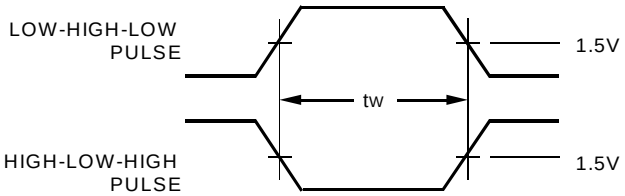
$R_T$ = Termination resistance: should be equal to $Z_{OUT}$ of the Pulse Generator.

## SET-UP, HOLD, AND RELEASE TIMES



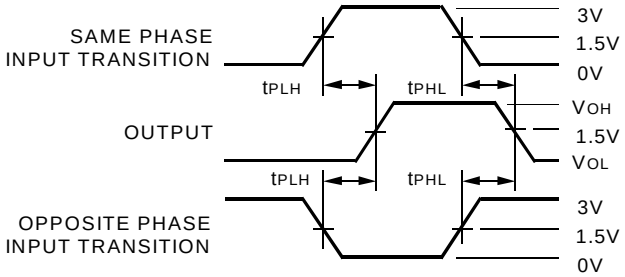

FCTL link

## PULSE WIDTH



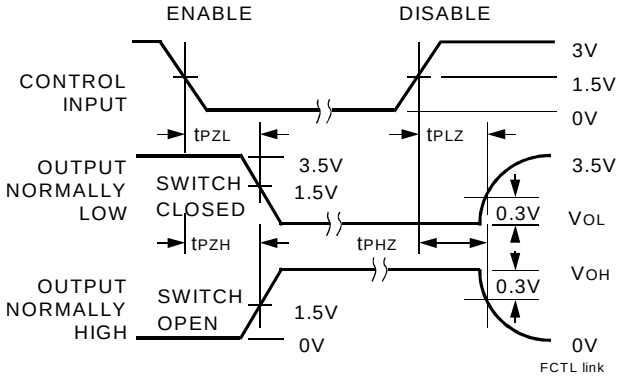

FCTL link

## PROPAGATION DELAY




FCTL link

## ENABLE AND DISABLE TIMES

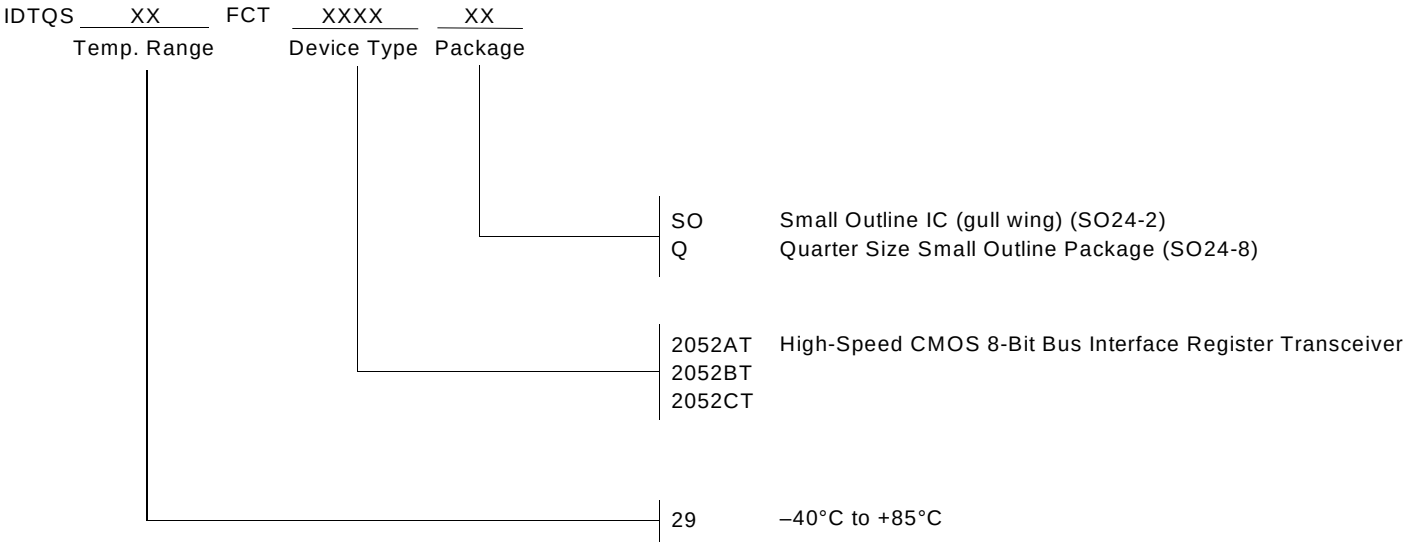



FCTL link

**NOTES:**

1. Diagram shown for input Control Enable-LOW and input Control Disable-HIGH.
2. Pulse Generator for All Pulses: Rate ≤ 10MHz; Zo ≤ 50Ω; $t_F$ ≤ 2.5ns; $t_R$ ≤ 2.5ns.

# ORDERING INFORMATION




*CORPORATE HEADQUARTERS*
2975 Stender Way
Santa Clara, CA 95054

*for SALES:*
800-345-7015 or 408-727-6116
fax: 408-492-8674
www.idt.com*

*To search for sales office near you, please click the sales button found on our home page or dial the 800# above and press 2.*