# 3.3V CMOS 18-BIT REGISTERED TRANSCEIVER WITH 5 VOLT TOLERANT I/O AND BUS-HOLD

**IDT74LVCH16501A**

## FEATURES:

- Typical $t_{SK(0)}$ (Output Skew) < 250ps
- ESD > 2000V per MIL-STD-883, Method 3015; > 200V using machine model (C = 200pF, R = 0)
- 0.635mm pitch SSOP, 0.50mm pitch TSSOP and 0.40mm pitch TVSOP packages
- Extended commercial range of -40°C to +85°C
- $V_{CC}$ = 3.3V ±0.3V, Normal Range
- $V_{CC}$ = 2.7V to 3.6V, Extended Range
- CMOS power levels (0.4µW typ. static)
- All inputs, outputs and I/O are 5 Volt tolerant
- Supports hot insertion

**Drive Features for LVCH16501A:**

- High Output Drivers: ±24mA
- Reduced system switching noise

## APPLICATIONS:

- 5V and 3.3V mixed voltage systems
- Data communication and telecommunication systems

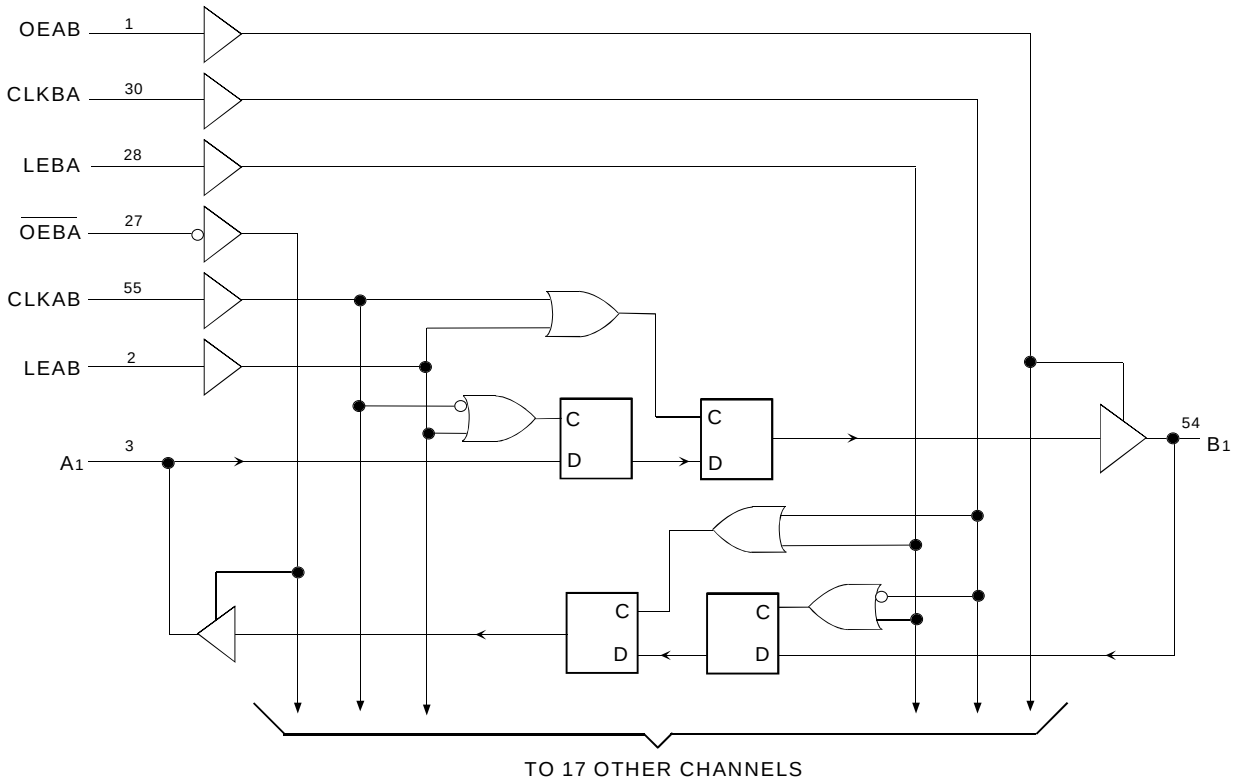
## DESCRIPTION

This 18-bit registered transceiver is built using advanced dual metal CMOS technology. This high-speed, low power 18-bit registered bus transceiver combines D-type latches and D-type flip-flops to allow data flow in transparent latched and clocked modes. Data flow in each direction is controlled by output-enable (OEAB and $\overline{OEBA}$), latch enable (LEAB and LEBA) and clock (CLKAB and CLKBA) inputs. For A-to-B data flow, the device operates in transparent mode when LEAB is high. When LEAB is low, the A data is latched if CLKAB is held at a high or low logic level. If LEAB is low, the A bus data is stored in the latch/flip-flop on the low-to-high transition of CLKAB. OEAB performs the output enable function on the B port. Data flow from B port to A port is similar but requires using $\overline{OEBA}$, LEBA and CLKBA. Flow-through organization of signal pins simplifies layout. All inputs are designed with hysteresis for improved noise margin.

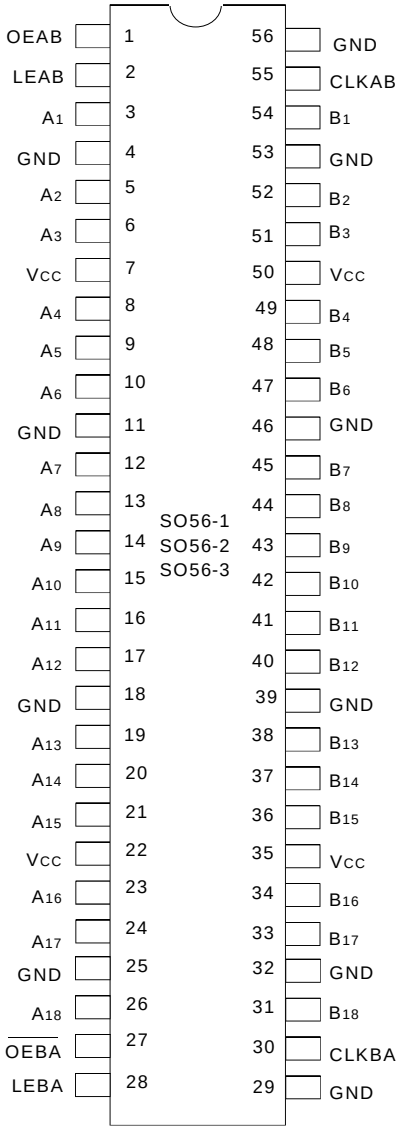
The LVCH16501A has been designed with a ±24mA output driver. This driver is capable of driving a moderate to heavy load while maintaining speed performance.

The LVCH16501A has "bus-hold" which retains the inputs' last state whenever the input goes to a high impedance. This prevents floating inputs and eliminates the need for pull-up/down resistors.

## Functional Block Diagram



## PIN CONFIGURATION




**SSOP/ TSSOP/ TVSOP**
**TOP VIEW**

## PIN DESCRIPTION

| Pin Names | Description |
|---|---|
| OEAB | A-to-B Output Enable Input |
| $\overline{OEBA}$ | B-to-A Output Enable Input (Active LOW) |
| LEAB | A-to-B Latch Enable Input |
| LEBA | B-to-A Latch Enable Input |
| CLKAB | A-to-B Clock Input |
| CLKBA | B-to-A Clock Input |
| Ax | A-to-B Data Inputs or B-to-A 3-State Outputs(1) |
| Bx | B-to-A Data Inputs or A-to-B 3-State Outputs(1) |

**NOTE:**
1. These pins have "Bus-hold". All other pins are standard inputs, outputs, or I/Os.

## ABSOLUTE MAXIMUM RATINGS (1)

| Symbol | Description | Max. | Unit |
|---|---|---|---|
| $V_{TERM}$(2) | Terminal Voltage with Respect to GND | – 0.5 to +6.5 | V |
| $V_{TERM}$(3) | Terminal Voltage with Respect to GND | – 0.5 to +6.5 | V |
| $T_{STG}$ | Storage Temperature | – 65 to +150 | °C |
| $I_{OUT}$ | DC Output Current | – 50 to +50 | mA |
| $I_{IK}$<br>$I_{OK}$ | Continuous Clamp Current,<br>$V_I$ < 0 or $V_O$ < 0 | – 50 | mA |
| $I_{CC}$<br>$I_{SS}$ | Continuous Current through<br>each $V_{CC}$ or GND | ±100 | mA |

LVC Link

**NOTES:**
1. Stresses greater than those listed under ABSOLUTE MAXIMUM RATINGS may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect reliability.
2. $V_{CC}$ terminals.
3. All terminals except $V_{CC}$.

## CAPACITANCE ($T_A$ = +25°C, f = 1.0MHz)

| Symbol | Parameter(1) | Conditions | Typ. | Max. | Unit |
|---|---|---|---|---|---|
| $C_{IN}$ | Input Capacitance | $V_{IN}$ = 0V | 4.5 | 6 | pF |
| $C_{OUT}$ | Output Capacitance | $V_{OUT}$ = 0V | 6.5 | 8 | pF |
| $C_{I/O}$ | I/O Port Capacitance | $V_{IN}$ = 0V | 6.5 | 8 | pF |

LVC Link

**NOTE:**
1. As applicable to the device type.

## FUNCTION TABLE (1, 2)

| Inputs | | | | Outputs |
|---|---|---|---|---|
| OEAB | LEAB | CLKAB | Ax | Bx |
| L | X | X | X | Z |
| H | H | X | L | L |
| H | H | X | H | H |
| H | L | ↑ | L | L |
| H | L | ↑ | H | H |
| H | L | L | X | B(3) |
| H | L | H | X | B(4) |

**NOTES:**
1. H = HIGH Voltage Level
   L = LOW Voltage Level
   X = Don't Care
   Z = High Impedance
   ↑ = LOW-to-HIGH Transition
2. A-to-B data flow is shown. B-to-A data flow is similar but uses $\overline{OEBA}$, LEBA, and CLKBA.
3. Output level before the indicated steady-state input conditions were established.
4. Output level before the indicated steady-state input conditions were established, provided that CLKAB was HIGH before LEAB went LOW.

# DC ELECTRICAL CHARACTERISTICS OVER OPERATING RANGE

**Following Conditions Apply Unless Otherwise Specified:**
**Operating Condition: $T_A$ = –40°C to +85°C**

| Symbol | Parameter | Test Conditions | | Min. | Typ.(1) | Max. | Unit |
|---|---|---|---|---|---|---|---|
| $V_{IH}$ | Input HIGH Voltage Level | $V_{CC}$ = 2.3V to 2.7V | | 1.7 | — | — | V |
| | | $V_{CC}$ = 2.7V to 3.6V | | 2 | — | — | |
| $V_{IL}$ | Input LOW Voltage Level | $V_{CC}$ = 2.3V to 2.7V | | — | — | 0.7 | V |
| | | $V_{CC}$ = 2.7V to 3.6V | | — | — | 0.8 | |
| $I_{IH}$<br>$I_{IL}$ | Input Leakage Current | $V_{CC}$ = 3.6V | $V_I$ = 0 to 5.5V | — | — | ±5 | µA |
| $I_{OZH}$<br>$I_{OZL}$ | High Impedance Output Current<br>(3-State Output pins) | $V_{CC}$ = 3.6V | $V_O$ = 0 to 5.5V | — | — | ±10 | µA |
| $I_{OFF}$ | Input/Output Power Off Leakage | $V_{CC}$ = 0V, $V_{IN}$ or $V_O \leq$ 5.5V | | — | — | ±50 | µA |
| $V_{IK}$ | Clamp Diode Voltage | $V_{CC}$ = 2.3V, $I_{IN}$ = – 18mA | | — | – 0.7 | – 1.2 | V |
| $V_H$ | Input Hysteresis | $V_{CC}$ = 3.3V | | — | 100 | — | mV |
| $I_{CCL}$<br>$I_{CCH}$ | Quiescent Power Supply Current | $V_{CC}$ = 3.6V | $V_{IN}$ = GND or $V_{CC}$ | — | — | 10 | µA |
| $I_{CCZ}$ | | | $3.6 \leq V_{IN} \leq 5.5V$(2) | — | — | 10 | |
| $\Delta I_{CC}$ | Quiescent Power Supply Current Variation | One input at $V_{CC}$ - 0.6V other inputs at $V_{CC}$ or GND | | — | — | 500 | µA |

LVC Link

**NOTES:**
1. Typical values are at $V_{CC}$ = 3.3V, +25°C ambient.
2. This applies in the disabled state only.

# BUS-HOLD CHARACTERISTICS

| Symbol | Parameter(1) | Test Conditions | | Min. | Typ.(2) | Max. | Unit |
|---|---|---|---|---|---|---|---|
| $I_{BHH}$ | Bus-Hold Input Sustain Current | $V_{CC}$ = 3.0V | $V_I$ = 2.0V | – 75 | — | — | µA |
| $I_{BHL}$ | | | $V_I$ = 0.8V | 75 | — | — | |
| $I_{BHH}$ | Bus-Hold Input Sustain Current | $V_{CC}$ = 2.3V | $V_I$ = 1.7V | — | — | — | µA |
| $I_{BHL}$ | | | $V_I$ = 0.7V | — | — | — | |
| $I_{BHHO}$ | Bus-Hold Input Overdrive Current | $V_{CC}$ = 3.6V | $V_I$ = 0 to 3.6V | — | — | ± 500 | µA |
| $I_{BHLO}$ | | | | | | | |

LVC Link

**NOTES:**
1. Pins with Bus-hold are identified in the pin description.
2. Typical values are at $V_{CC}$ = 3.3V, +25°C ambient.

# OUTPUT DRIVE CHARACTERISTICS

| Symbol | Parameter | Test Conditions[1] | | Min. | Max. | Unit |
|---|---|---|---|---|---|---|
| $V_{OH}$ | Output HIGH Voltage | $V_{CC}$ = 2.3V to 3.6V | $I_{OH}$ = – 0.1mA | $V_{CC}$ – 0.2 | — | V |
| | | $V_{CC}$ = 2.3V | $I_{OH}$ = – 6mA | 2 | — | |
| | | $V_{CC}$ = 2.3V | $I_{OH}$ = – 12mA | 1.7 | — | |
| | | $V_{CC}$ = 2.7V | | 2.2 | — | |
| | | $V_{CC}$ = 3.0V | | 2.4 | — | |
| | | $V_{CC}$ = 3.0V | $I_{OH}$ = – 24mA | 2.2 | — | |
| $V_{OL}$ | Output LOW Voltage | $V_{CC}$ = 2.3V to 3.6V | $I_{OL}$ = 0.1mA | — | 0.2 | V |
| | | $V_{CC}$ = 2.3V | $I_{OL}$ = 6mA | — | 0.4 | |
| | | | $I_{OL}$ = 12mA | — | 0.7 | |
| | | $V_{CC}$ = 2.7V | $I_{OL}$ = 12mA | — | 0.4 | |
| | | $V_{CC}$ = 3.0V | $I_{OL}$ = 24mA | — | 0.55 | |

LVC Link

**NOTE:**

1. $V_{IH}$ and $V_{IL}$ must be within the min. or max. range shown in the DC ELECTRICAL CHARACTERISTICS OVER OPERATING RANGE table for the appropriate $V_{CC}$ range. $T_A$ = – 40°C to +85°C.

# OPERATING CHARACTERISTICS, $V_{CC}$ = 3.3V ± 0.3V, $T_A$ = 25°C

| Symbol | Parameter | Test Conditions | Typical | Unit |
|---|---|---|---|---|
| $C_{PD}$ | Power Dissipation Capacitance per transceiver Outputs enabled | $C_L$ = 0pF, f = 10Mhz | | pF |
| $C_{PD}$ | Power Dissipation Capacitance per transceiver Outputs disabled | | | pF |

# SWITCHING CHARACTERISTICS (1)

| Symbol | Parameter | | Vcc = 2.7V | | Vcc = 3.3V±0.3V | | Unit |
|---|---|---|---|---|---|---|---|
| | | | Min. | Max. | Min. | Max. | |
| $t_{PLH}$<br>$t_{PHL}$ | Propagation Delay<br>Ax to Bx or Bx to Ax | | 1.5 | 5.2 | 1.5 | 4.6 | ns |
| $t_{PLH}$<br>$t_{PHL}$ | Propagation Delay<br>LEBA to Ax, LEAB to Bx | | 1.5 | 6 | 1.5 | 5.3 | ns |
| $t_{PLH}$<br>$t_{PHL}$ | Propagation Delay<br>CLKBA to Ax, CLKAB to Bx | | 1.5 | 6 | 1.5 | 5.3 | ns |
| $t_{PZH}$<br>$t_{PZL}$ | Output Enable Time<br>$\overline{OEBA}$ to Ax, OEAB to Bx | | 1.5 | 6 | 1.5 | 5.6 | ns |
| $t_{PHZ}$<br>$t_{PLZ}$ | Output Disable Time<br>$\overline{OEBA}$ to Ax, OEAB to Bx | | 1.5 | 6.5 | 1.5 | 5.8 | ns |
| $t_{SU}$ | Set-up Time, HIGH or LOW<br>Ax to CLKAB, Bx to CLKBA | | 3 | — | 3 | — | ns |
| $t_H$ | Hold Time, HIGH or LOW<br>Ax to CLKAB, Bx to CLKBA | | 0 | — | 0 | — | ns |
| $t_{SU}$ | Set-up Time<br>HIGH or LOW | Clock<br>LOW | 3 | — | 3 | — | ns |
| | Ax to LEAB,<br>Bx to LEBA | Clock<br>HIGH | 2 | — | 2 | — | ns |
| $t_H$ | Hold Time HIGH or LOW<br>Ax to LEAB, Bx to LEBA | | 1.5 | — | 1.5 | — | ns |
| $t_W$ | LEAB or LEBA Pulse Width HIGH | | 3 | — | 3 | — | ns |
| $t_W$ | CLKAB or CLKBA Pulse Width HIGH or LOW | | 3 | — | 3 | — | ns |
| $t_{SK}(o)$ | Output Skew(2) | | — | — | — | 500 | ps |

**NOTES:**
1. See test circuits and waveforms. $T_A$ = – 40°C to + 85°C.
2. Skew between any two outputs of the same package and switching in the same direction.

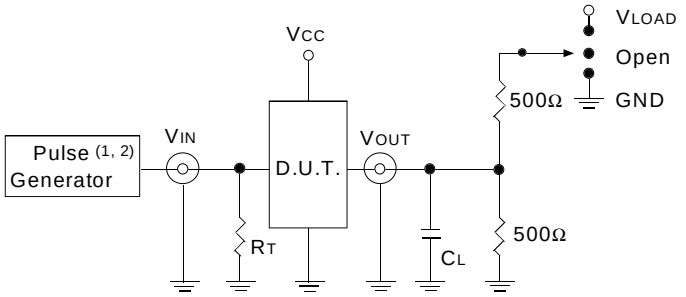
# TEST CIRCUITS AND WAVEFORMS

## TEST CONDITIONS

| Symbol | $V_{CC}^{(1)}$= 3.3V ±0.3V | $V_{CC}^{(1)}$ = 2.7V | $V_{CC}^{(2)}$= 2.5V ±0.2V | Unit |
|---|---|---|---|---|
| $V_{LOAD}$ | 6 | 6 | 2 x Vcc | V |
| $V_{IH}$ | 2.7 | 2.7 | Vcc | V |
| $V_T$ | 1.5 | 1.5 | Vcc / 2 | V |
| $V_{LZ}$ | 300 | 300 | 150 | mV |
| $V_{HZ}$ | 300 | 300 | 150 | mV |
| $C_L$ | 50 | 50 | 30 | pF |

LVC Link

## TEST CIRCUITS FOR ALL OUTPUTS




LVC Link

**DEFINITIONS:**
$C_L$ = Load capacitance: includes jig and probe capacitance.
$R_T$ = Termination resistance: should be equal to $Z_{OUT}$ of the Pulse Generator.

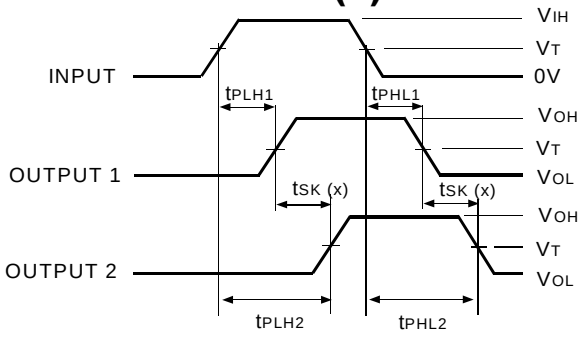
**NOTE:**
1. Pulse Generator for All Pulses: Rate ≤ 10MHz; $t_F$ ≤ 2.5ns; $t_R$ ≤ 2.5ns.
2. Pulse Generator for All Pulses: Rate ≤ 10MHz; $t_F$ ≤ 2ns; $t_R$ ≤ 2ns.

## SWITCH POSITION

| Test | Switch |
|---|---|
| Open Drain<br>Disable Low<br>Enable Low | $V_{LOAD}$ |
| Disable High<br>Enable High | GND |
| All Other tests | Open |

LVC Link

## OUTPUT SKEW - tsk (x)

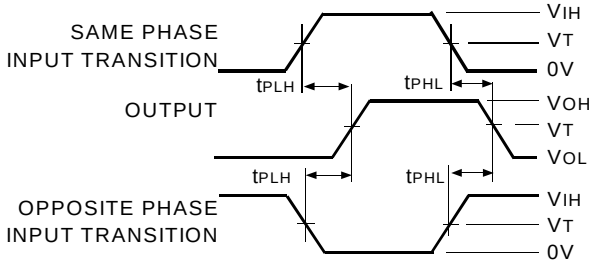



$t_{SK(x)} = |t_{PLH2} - t_{PLH1}|$ or $|t_{PHL2} - t_{PHL1}|$

LVC Link

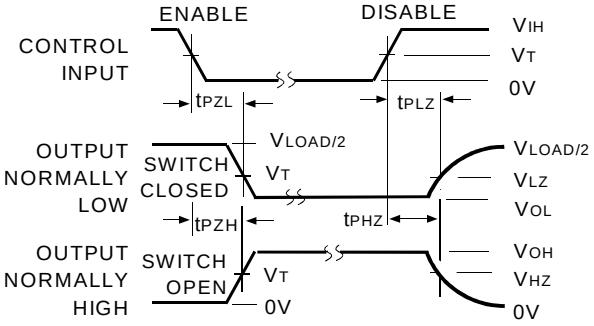
**NOTES:**
1. For $t_{SK}$(o) OUTPUT1 and OUTPUT2 are any two outputs.
2. For $t_{SK}$(b) OUTPUT1 and OUTPUT2 are in the same bank.

## PROPAGATION DELAY




LVC Link

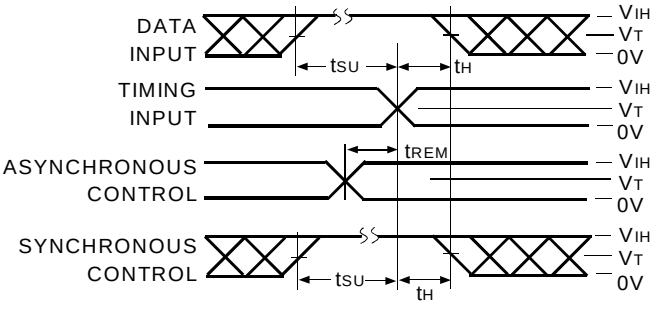
## ENABLE AND DISABLE TIMES




LVC Link

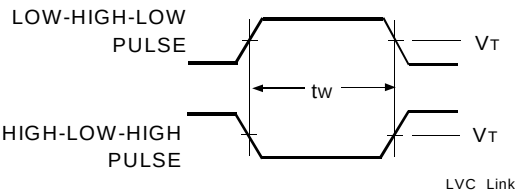
**NOTE:**
1. Diagram shown for input Control Enable-LOW and input Control Disable-HIGH.

## SET-UP, HOLD, AND RELEASE TIMES



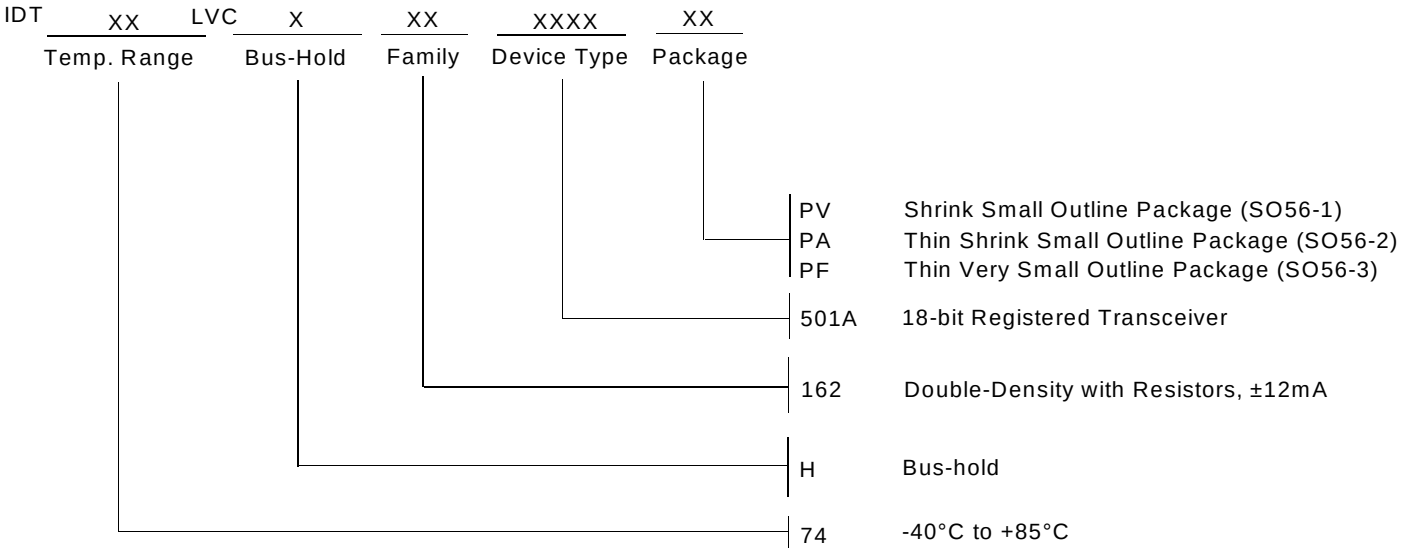

LVC Link

## PULSE WIDTH




LVC Link

# ORDERING INFORMATION




*CORPORATE HEADQUARTERS*
2975 Stender Way
Santa Clara, CA 95054

*for SALES:*
800-345-7015 or 408-727-6116
fax: 408-492-8674
www.idt.com*

*To search for sales office near you, please click the sales button found on our home page or dial the 800# above and press 2.*