



3.3V CMOS 18-BIT BUS INTERFACE REGISTER WITH 5 VOLT TOLERANT I/O AND BUS-HOLD

IDT74LVCH162823A

FEATURES:

- Typical $t_{sk(0)}$ (Output Skew) < 250ps
- ESD > 2000V per MIL-STD-883, Method 3015;
> 200V using machine model (C = 200pF, R = 0)
- 0.635mm pitch SSOP, 0.50mm pitch TSSOP
and 0.40mm pitch TVSOP packages
- Extended commercial range of -40°C to +85°C
- $V_{CC} = 3.3V \pm 0.3V$, Normal Range
- $V_{CC} = 2.7V$ to 3.6V, Extended Range
- CMOS power levels (0.4μW typ. static)
- All inputs, outputs and I/O are 5 Volt tolerant
- Supports hot insertion

Drive Features for LVCH162823A:

- Balanced Output Drivers: $\pm 12mA$
- Low Switching Noise

APPLICATIONS:

- 5V and 3.3V mixed voltage systems
- Data communication and telecommunication systems

DESCRIPTION:

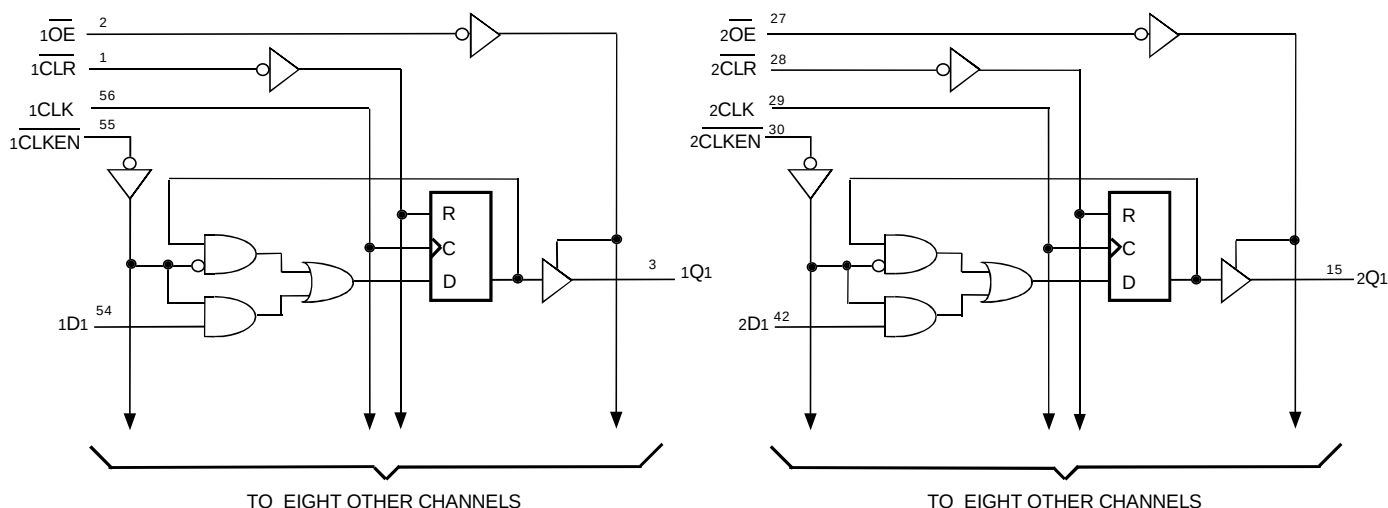
The LVCH162823A 18-bit bus interface register is built using advanced dual metal CMOS technology. This high-speed, low-power register with clock enable ($\overline{CLKEN}$) and clear ($\overline{CLR}$) controls is ideal for parity bus interfacing in high-performance synchronous systems. The control inputs are organized to operate the device as two 9-bit registers or one 18-bit register. Flow-through organization of signal pins simplifies layout. All inputs are designed with hysteresis for improved noise margin.

All pins of the LVCH162823A can be driven from either 3.3V or 5V devices. This feature allows the use of this device as a translator in a mixed 3.3V/5V supply system.

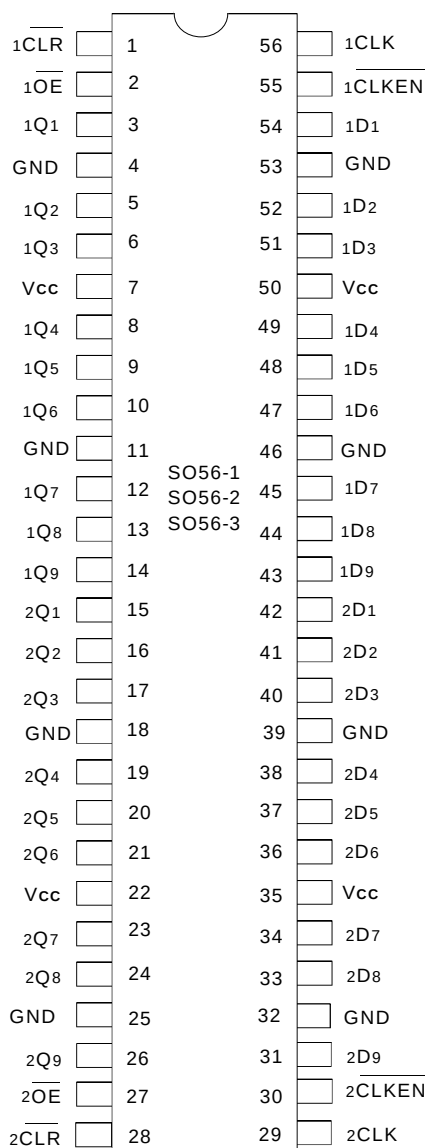
The LVCH162823A has series resistors in the device output structure which will significantly reduce line noise when used with light loads. This driver has been developed to drive $\pm 12mA$ at the designated threshold levels.

The LVCH162823A has “bus-hold” which retains the inputs' last state whenever the input goes to a high impedance. This prevents floating inputs and eliminates the need for pull-up/down resistors.

FUNCTIONAL BLOCK DIAGRAM



PIN CONFIGURATION



SSOP/ TSSOP/ TVSOP
TOP VIEW

PIN DESCRIPTION

Pin Names	Description
xDx	Data Inputs ⁽¹⁾
xCLK	Clock Inputs
$\overline{\text{xCLKEN}}$	Clock Enable Inputs (Active LOW)
$\overline{\text{xCLR}}$	Asynchronous Clear Inputs (Active LOW)
$\overline{\text{xOE}}$	Output Enable Inputs (Active LOW)
xQx	3-State Outputs

NOTE:

- These pins have "Bus-hold". All other pins are standard inputs, outputs, or I/Os.

ABSOLUTE MAXIMUM RATINGS ⁽¹⁾

Symbol	Description	Max.	Unit
VTERM	Terminal Voltage with Respect to GND	– 0.5 to +6.5	V
TSTG	Storage Temperature	– 65 to +150	°C
IOUT	DC Output Current	– 50 to +50	mA
IIK	Continuous Clamp Current, $V_i < 0$ or $V_o < 0$	– 50	mA
ICC	Continuous Current through each Vcc or GND	±100	mA

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NOTE:

- Stresses greater than those listed under ABSOLUTE MAXIMUM RATINGS may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect reliability.

CAPACITANCE ($T_A = +25^\circ\text{C}$, $f = 1.0\text{MHz}$)

Symbol	Parameter ⁽¹⁾	Conditions	Typ.	Max.	Unit
CIN	Input Capacitance	$V_{IN} = 0\text{V}$	4.5	6	pF
COUT	Output Capacitance	$V_{OUT} = 0\text{V}$	6.5	8	pF
C _{I/O}	I/O Port Capacitance	$V_{IN} = 0\text{V}$	6.5	8	pF

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NOTE:

- As applicable to the device type.

FUNCTION TABLE ⁽¹⁾

Inputs					Outputs	Function
$\overline{\text{xOE}}$	$\overline{\text{xCLR}}$	$\overline{\text{xCLKEN}}$	xCLK	xDx	xQx	
H	X	X	X	X	Z	High Z
H	L	X	X	X	Z	Clear
L	L	X	X	X	L	
H	H	H	X	X	Z	Hold
L	H	H	X	X	Q_0	
H	H	L	↑	L	Z	Load
H	H	L	↑	H	Z	
L	H	L	↑	L	L	
L	H	L	↑	H	H	

NOTE:

- H = HIGH Voltage Level
L = LOW Voltage Level
X = Don't Care
Z = High Impedance
↑ = LOW-to-HIGH Transition
 Q_0 = Level of Q before the indicated steady-state input conditions were established.

DC ELECTRICAL CHARACTERISTICS OVER OPERATING RANGE

Following Conditions Apply Unless Otherwise Specified:

Operating Condition: $T_A = -40^{\circ}\text{C}$ to $+85^{\circ}\text{C}$

Symbol	Parameter	Test Conditions		Min.	Typ. ⁽¹⁾	Max.	Unit
V_{IH}	Input HIGH Voltage Level	$V_{CC} = 2.3\text{V}$ to 2.7V		1.7	—	—	V
		$V_{CC} = 2.7\text{V}$ to 3.6V		2	—	—	
V_{IL}	Input LOW Voltage Level	$V_{CC} = 2.3\text{V}$ to 2.7V		—	—	0.7	V
		$V_{CC} = 2.7\text{V}$ to 3.6V		—	—	0.8	
I_{IH} I_{IL}	Input Leakage Current	$V_{CC} = 3.6\text{V}$	$V_I = 0$ to 5.5V	—	—	± 5	μA
I_{OZH} I_{OZL}	High Impedance Output Current (3-State Output pins)	$V_{CC} = 3.6\text{V}$	$V_O = 0$ to 5.5V	—	—	± 10	μA
I_{OFF}	Input/Output Power Off Leakage	$V_{CC} = 0\text{V}$, V_{IN} or $V_O \leq 5.5\text{V}$		—	—	± 50	μA
V_{IK}	Clamp Diode Voltage	$V_{CC} = 2.3\text{V}$, $I_{IN} = -18\text{mA}$		—	-0.7	-1.2	V
V_H	Input Hysteresis	$V_{CC} = 3.3\text{V}$		—	100	—	mV
I_{CCL} I_{CCH} I_{CCZ}	Quiescent Power Supply Current	$V_{CC} = 3.6\text{V}$	$V_{IN} = \text{GND}$ or V_{CC}	—	—	10	μA
			$3.6 \leq V_{IN} \leq 5.5\text{V}^{(2)}$	—	—	10	
ΔI_{CC}	Quiescent Power Supply Current Variation	One input at $V_{CC} - 0.6\text{V}$ other inputs at V_{CC} or GND		—	—	500	μA

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NOTES:

- Typical values are at $V_{CC} = 3.3\text{V}$, $+25^{\circ}\text{C}$ ambient.
- This applies in the disabled state only.

BUS-HOLD CHARACTERISTICS

Symbol	Parameter ⁽¹⁾	Test Conditions		Min.	Typ. ⁽²⁾	Max.	Unit
I_{BHH} I_{BHL}	Bus-Hold Input Sustain Current	$V_{CC} = 3.0\text{V}$	$V_I = 2.0\text{V}$	-75	—	—	μA
			$V_I = 0.8\text{V}$	75	—	—	
I_{BHH} I_{BHL}	Bus-Hold Input Sustain Current	$V_{CC} = 2.3\text{V}$	$V_I = 1.7\text{V}$	—	—	—	μA
			$V_I = 0.7\text{V}$	—	—	—	
I_{BHNO} I_{BHLO}	Bus-Hold Input Overdrive Current	$V_{CC} = 3.6\text{V}$	$V_I = 0$ to 3.6V	—	—	± 500	μA

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NOTES:

- Pins with Bus-hold are identified in the pin description.
- Typical values are at $V_{CC} = 3.3\text{V}$, $+25^{\circ}\text{C}$ ambient.

OUTPUT DRIVE CHARACTERISTICS

Symbol	Parameter	Test Conditions ⁽¹⁾		Min.	Max.	Unit
VOH	Output HIGH Voltage	VCC = 2.3V to 3.6V	IOH = - 0.1mA	VCC - 0.2	—	V
		VCC = 2.3V	IOH = - 4mA	1.9	—	
			IOH = - 6mA	1.7	—	
		VCC = 2.7V	IOH = - 4mA	2.2	—	
			IOH = - 8mA	2	—	
		VCC = 3.0V	IOH = - 6mA	2.4	—	
			IOH = - 12mA	2	—	
VOL	Output LOW Voltage	VCC = 2.3V to 3.6V	IOL = 0.1mA	—	0.2	V
		VCC = 2.3V	IOL = 4mA	—	0.4	
			IOL = 6mA	—	0.55	
		VCC = 2.7V	IOL = 4mA	—	0.4	
			IOL = 8mA	—	0.6	
		VCC = 3.0V	IOL = 6mA	—	0.55	
			IOL = 12mA	—	0.8	

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NOTE:

1. VIH and VIL must be within the min. or max. range shown in the DC ELECTRICAL CHARACTERISTICS OVER OPERATING RANGE table for the appropriate VCC range. TA = - 40°C to +85°C.

OPERATING CHARACTERISTICS, VCC = 3.3V ± 0.3V, TA = 25°C

Symbol	Parameter	Test Conditions	Typical	Unit
CPD	Power Dissipation Capacitance Outputs enabled	CL = 0pF, f = 10Mhz	—	pF
CPD	Power Dissipation Capacitance Outputs disabled		—	pF

SWITCHING CHARACTERISTICS (1)

Symbol	Parameter	V _{CC} = 2.7V		V _{CC} = 3.3V±0.3V		
		Min	Max	Min	Max	Unit
t _{PLH} t _{PHL}	Propagation Delay xCLK to xQx	1.5	10	1.5	6	ns
t _{PHL}	Propagation Delay xCLR to xQx	1.5	12	1.5	8	ns
t _{PZH} t _{PZL}	Output Enable Time xOE to xQx	1.5	11	1.5	7	ns
t _{PHZ} t _{PLZ}	Output Disable Time xOE to xQx	1.5	10	1.5	6.5	ns
t _{SU}	Set-up Time HIGH or LOW xDx to xCLK	3	—	3	—	ns
t _H	Hold Time HIGH or LOW xDx to xCLK	1.5	—	0	—	ns
t _{SU}	Set-up Time HIGH or LOW xCLKEN to xCLK	3.5	—	3.5	—	ns
t _H	Hold Time HIGH or LOW xCLKEN to xCLK	1.5	—	0	—	ns
t _w	xCLK Pulse Width HIGH or LOW	7	—	6	—	ns
t _w	xCLR Pulse Width LOW	6	—	6	—	ns
t _{REM}	Recovery Time xCLR to xCLK	6	—	6	—	ns
t _{SK(0)}	Output Skew ⁽²⁾	—	—	—	500	ps

NOTES:

1. See test circuits and waveforms. T_A = – 40°C to + 85°C.
2. Skew between any two outputs of the same package and switching in the same direction.

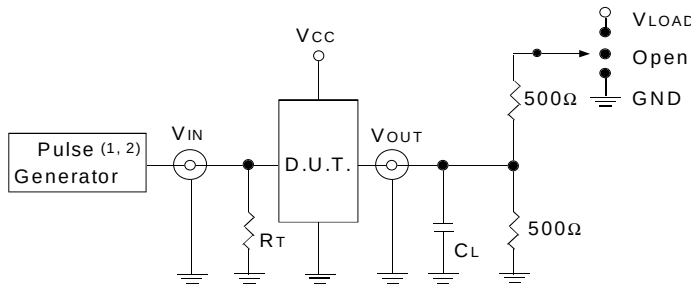
TEST CIRCUITS AND WAVEFORMS

TEST CONDITIONS

Symbol	V _{CC} (1)= 3.3V ±0.3V	V _{CC} (1)= 2.7V	V _{CC} (2)= 2.5V ±0.2V	Unit
V _{LOAD}	6	6	2 x V _{CC}	V
V _{IH}	2.7	2.7	V _{CC}	V
V _T	1.5	1.5	V _{CC} / 2	V
V _{LZ}	300	300	150	mV
V _{HZ}	300	300	150	mV
C _L	50	50	30	pF

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TEST CIRCUITS FOR ALL OUTPUTS



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DEFINITIONS:

C_L = Load capacitance: includes jig and probe capacitance.

R_T = Termination resistance: should be equal to Z_{OUT} of the Pulse Generator.

NOTES:

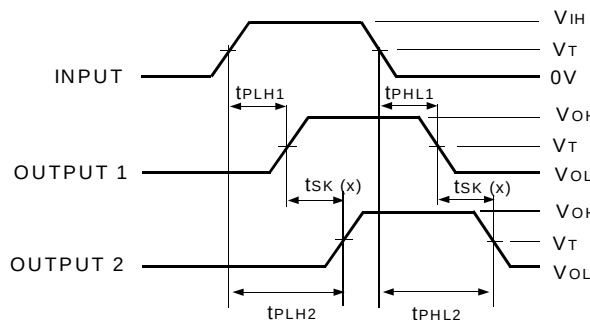
1. Pulse Generator for All Pulses: Rate ≤ 10MHz; t_F ≤ 2.5ns; t_R ≤ 2.5ns.
2. Pulse Generator for All Pulses: Rate ≤ 10MHz; t_F ≤ 2ns; t_R ≤ 2ns.

SWITCH POSITION

Test	Switch
Open Drain Disable Low Enable Low	V _{LOAD}
Disable High Enable High	GND
All Other tests	Open

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OUTPUT SKEW - t_{SK} (x)



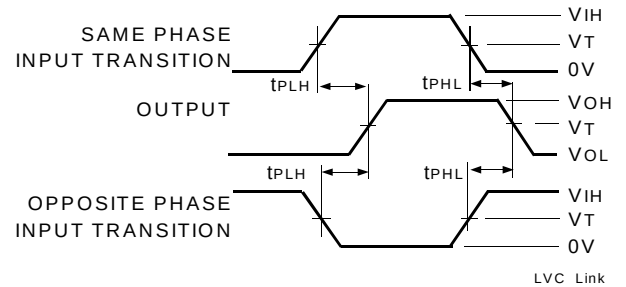
$$t_{SK}(x) = |t_{PLH2} - t_{PLH1}| \text{ or } |t_{PHL2} - t_{PHL1}|$$

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NOTES:

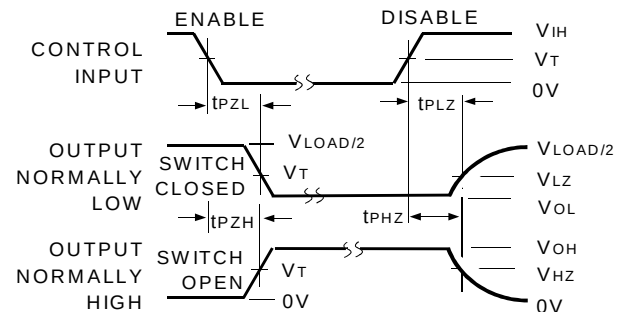
1. For t_{SK}(o) OUTPUT1 and OUTPUT2 are any two outputs.
2. For t_{SK}(b) OUTPUT1 and OUTPUT2 are in the same bank.

PROPAGATION DELAY



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ENABLE AND DISABLE TIMES

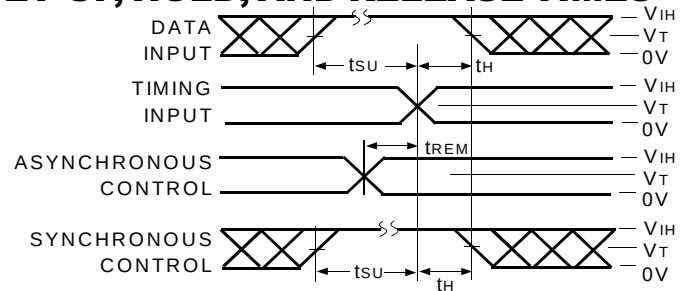


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NOTE:

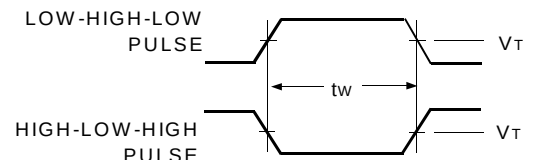
1. Diagram shown for input Control Enable-LOW and input Control Disable-HIGH.

SET-UP, HOLD, AND RELEASE TIMES



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PULSE WIDTH



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ORDERING INFORMATION

IDT	XX	LVC	X	XX	XXXX	XX	
	Temp. Range		Bus-Hold	Family	Device Type	Package	
						PV	Shrink Small Outline Package (SO56-1)
						PA	Thin Shrink Small Outline Package (SO56-2)
						PF	Thin Very Small Outline Package (SO56-3)
						823A	18-Bit Bus Interface Register
						162	Double-Density with Resistors, ±12mA
						H	Bus-hold
						74	-40°C to +85°C



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