3.3V CMOS 12-BIT SYNCHRONOUS BUS EXCHANGER WITH BUS-HOLD AND 5 VOLT TOLERANT I/O

IDT74LVCH16276A

FEATURES:

- Typical $t_{SK(0)}$ (Output Skew) < 250ps
- ESD > 2000V per MIL-STD-883, Method 3015; > 200V using machine model (C = 200pF, R = 0)
- 0.635mm pitch SSOP, 0.50mm pitch TSSOP and 0.40mm pitch TVSOP packages
- Extended commercial range of -40°C to +85°C
- V_{CC} = 3.3V ±0.3V, Normal Range
- V_{CC} = 2.7V to 3.6V, Extended Range
- CMOS power levels (0.4µW typ. static)
- All inputs, outputs and I/O are 5 Volt tolerant
- Supports hot insertion

Drive Features for LVCH16276A:

- High Output Drivers: ±24mA
- Reduced system switching noise

APPLICATIONS:

- 5V and 3.3V mixed voltage systems
- Data communication and telecommunication systems

DESCRIPTION

The LVCH16276A synchronous bus exchanger is built using advanced dual metal CMOS technology.The LVCH16276A is a high-speed, bidirectional, 12-bit, registered, bus multiplexer for use in synchronous memory interleaving applications. All registers have a common clock and use a clock enable ($\overline{CExxx}$) on each data register to control data sequencing. The output enables and mux select ($\overline{OEA}$, $\overline{OEB}$ and SEL) are also under synchronous control allowing direction changes to be edge triggered events.

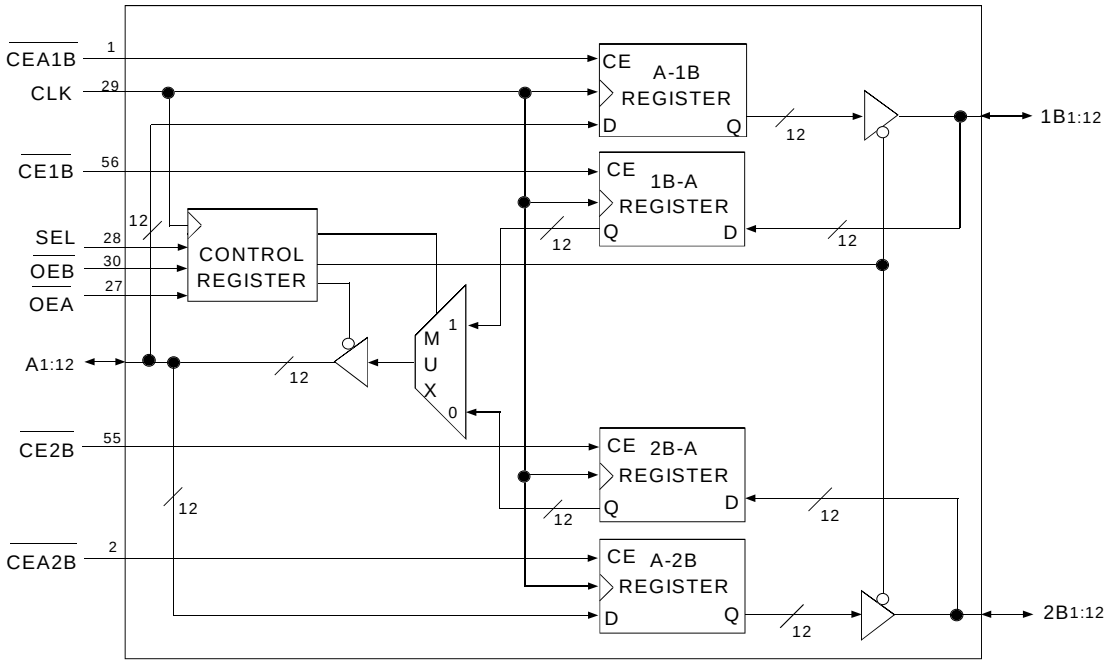
The tri-port bus exchanger has three 12-bit ports. Data may be transferred between the A port and either/both of the B ports. The clock enable ($\overline{CE1B}$, $\overline{CE2B}$, $\overline{CEA1B}$ and $\overline{CEA2B}$) inputs control the data storage. Both B ports have a common output enable ($\overline{OEB}$) to aid in synchronously loading the B registers from the B port.

All pins of the LVCH16276A can be driven from either 3.3V or 5V devices. This feature allows the use of this device as a translator in a mixed 3.3V/5V supply system.

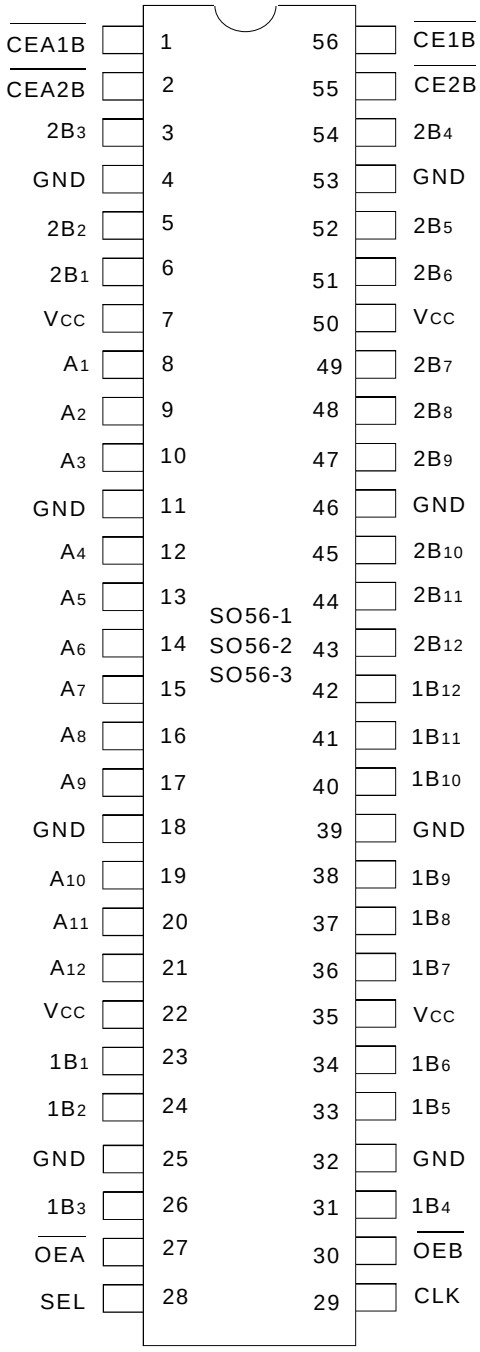
The LVCH16276A has been designed with a ±24mA output driver. This driver is capable of driving a moderate to heavy load while maintaining speed performance.

The LVCH16276A has "bus-hold" which retains the inputs' last state whenever the input goes to a high impedance. This prevents floating inputs and eliminates the need for pull-up/down resistors.

Functional Block Diagram



PIN CONFIGURATION



SSOP/ TSSOP/ TVSOP
TOP VIEW

ABSOLUTE MAXIMUM RATINGS (1)

Symbol	Description	Max.	Unit
V_{TERM}(2)	Terminal Voltage with Respect to GND	– 0.5 to +6.5	V
V_{TERM}(3)	Terminal Voltage with Respect to GND	– 0.5 to +6.5	V
T_{STG}	Storage Temperature	– 65 to +150	°C
I_{OUT}	DC Output Current	– 50 to +50	mA
I_{IK} I_{OK}	Continuous Clamp Current, $V_I < 0$ or $V_O < 0$	– 50	mA
I_{CC} I_{SS}	Continuous Current through each V_{CC} or GND	±100	mA

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NOTES:
1. Stresses greater than those listed under ABSOLUTE MAXIMUM RATINGS may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect reliability.
2. V_{CC} terminals.
3. All terminals except V_{CC}.

CAPACITANCE (T_A = +25°C, f = 1.0MHz)

Symbol	Parameter(1)	Conditions	Typ.	Max.	Unit
C_{IN}	Input Capacitance	V_{IN} = 0V	4.5	6	pF
C_{OUT}	Output Capacitance	V_{OUT} = 0V	6.5	8	pF
$C_{I/O}$	I/O Port Capacitance	V_{IN} = 0V	6.5	8	pF

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NOTE:
1. As applicable to the device type.

PIN DESCRIPTION

A(1:12)	I/O	Bidirectional Data Port A. Usually connected to the CPU's Address/Data bus.(1)
1B(1:12)	I/O	Bidirectional Data Port 1B. Usually connected to the even path or even bank of memory.(1)
2B(1:12)	I/O	Bidirectional Data Port 2B. Usually connected to the odd path or odd bank of memory.(1)
CLK	I	Clock Input.
$\overline{CEA1B}$	I	Clock Enable Input for the A-1B Register. If $\overline{CEA1B}$ is LOW during the rising edge of CLK, data will be clocked into register A-1B (Active LOW).
$\overline{CEA2B}$	I	Clock Enable Input for the A-2B Register. If $\overline{CEA2B}$ is LOW during the rising edge of CLK, data will be clocked into register A-2B (Active LOW).
$\overline{CE1B}$	I	Clock Enable Input for the 1B-A Register. If $\overline{CE1B}$ is LOW during the rising edge of CLK, data will be clocked into register 1B-A (Active LOW).
$\overline{CE2B}$	I	Clock Enable Input for the 2B-A Register. If $\overline{CE2B}$ is LOW during the rising edge of CLK, data will be clocked into register 2B-A (Active LOW).
SEL	I	1B or 2B Part Selection. When HIGH during the rising edge of CLK, SEL enables data transfer from 1B Port to A Port. When LOW during the rising edge of CLK, SEL enables data transfer from 2B Port to A Port.
$\overline{OEA}$	I	Synchronous Output Enable for A Port (Active LOW).
$\overline{OEB}$	I	Synchronous Output Enable for 1B Port and 2B Port (Active LOW).

NOTE:
1. These pins have "Bus-hold". All other pins have inputs, outputs, or I/Os.

FUNCTION TABLES (1)

Inputs							Outputs
1Bx	**2Bx**	**SEL**	**$\overline{CE1B}$**	**$\overline{CE2B}$**	**$\overline{OEA}$**	**CLK**	**Ax**
H	X	H	L	X	L	↑	H
L	X	H	L	X	L	↑	L
X	X	H	H	X	L	↑	A_0(2)
X	H	L	X	L	L	↑	H
X	L	L	X	L	L	↑	L
X	X	L	X	H	L	↑	A_0(2)
X	X	X	X	X	H	↑	Z

Inputs					Outputs	
Ax	**$\overline{CEA1B}$**	**$\overline{CEA2B}$**	**$\overline{OEB}$**	**CLK**	**1Bx**	**2Bx**
H	L	L	L	↑	H	H
L	L	L	L	↑	L	L
H	L	H	L	↑	H	B_0(2)
L	L	H	L	↑	L	B_0(2)
H	H	L	L	↑	B_0(2)	H
L	H	L	L	↑	B_0(2)	L
X	H	H	L	↑	B_0(2)	B_0(2)
X	X	X	H	↑	Z	Z
X	X	X	L	↑	Active	Active

NOTES:
1. H = HIGH Voltage Level
   L = LOW Voltage Level
   X = Don't Care
   Z = High-Impedance
   ↑ = LOW-to-HIGH Transition
2. A_0, B_0 = Output level before the indicated steady-state input conditions were established.

DC ELECTRICAL CHARACTERISTICS OVER OPERATING RANGE

Following Conditions Apply Unless Otherwise Specified:
Operating Condition: T_A = –40°C to +85°C

Symbol	Parameter	Test Conditions		Min.	Typ.(1)	Max.	Unit
V_{IH}	Input HIGH Voltage Level	V_{CC} = 2.3V to 2.7V		1.7	—	—	V
		V_{CC} = 2.7V to 3.6V		2	—	—	
V_{IL}	Input LOW Voltage Level	V_{CC} = 2.3V to 2.7V		—	—	0.7	V
		V_{CC} = 2.7V to 3.6V		—	—	0.8	
I_{IH} I_{IL}	Input Leakage Current	V_{CC} = 3.6V	V_I = 0 to 5.5V	—	—	±5	µA
I_{OZH} I_{OZL}	High Impedance Output Current (3-State Output pins)	V_{CC} = 3.6V	V_O = 0 to 5.5V	—	—	±10	µA
I_{OFF}	Input/Output Power Off Leakage	V_{CC} = 0V, V_{IN} or $V_O \leq$ 5.5V		—	—	±50	µA
V_{IK}	Clamp Diode Voltage	V_{CC} = 2.3V, I_{IN} = – 18mA		—	– 0.7	– 1.2	V
V_H	Input Hysteresis	V_{CC} = 3.3V		—	100	—	mV
I_{CCL} I_{CCH}	Quiescent Power Supply Current	V_{CC} = 3.6V	V_{IN} = GND or V_{CC}	—	—	10	µA
I_{CCZ}			$3.6 \leq V_{IN} \leq 5.5V$(2)	—	—	10	
ΔI_{CC}	Quiescent Power Supply Current Variation	One input at V_{CC} - 0.6V other inputs at V_{CC} or GND		—	—	500	µA

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NOTES:
1. Typical values are at V_{CC} = 3.3V, +25°C ambient.
2. This applies in the disabled state only.

BUS-HOLD CHARACTERISTICS

Symbol	Parameter(1)	Test Conditions		Min.	Typ.(2)	Max.	Unit
I_{BHH}	Bus-Hold Input Sustain Current	V_{CC} = 3.0V	V_I = 2.0V	– 75	—	—	µA
I_{BHL}			V_I = 0.8V	75	—	—	
I_{BHH}	Bus-Hold Input Sustain Current	V_{CC} = 2.3V	V_I = 1.7V	—	—	—	µA
I_{BHL}			V_I = 0.7V	—	—	—	
I_{BHHO}	Bus-Hold Input Overdrive Current	V_{CC} = 3.6V	V_I = 0 to 3.6V	—	—	± 500	µA
I_{BHLO}							

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NOTES:
1. Pins with Bus-hold are identified in the pin description.
2. Typical values are at V_{CC} = 3.3V, +25°C ambient.

OUTPUT DRIVE CHARACTERISTICS

Symbol	Parameter	Test Conditions[1]		Min.	Max.	Unit
V_{OH}	Output HIGH Voltage	V_{CC} = 2.3V to 3.6V	I_{OH} = – 0.1mA	V_{CC} – 0.2	—	V
		V_{CC} = 2.3V	I_{OH} = – 6mA	2	—	
		V_{CC} = 2.3V	I_{OH} = – 12mA	1.7	—	
		V_{CC} = 2.7V		2.2	—	
		V_{CC} = 3.0V		2.4	—	
		V_{CC} = 3.0V	I_{OH} = – 24mA	2.2	—	
V_{OL}	Output LOW Voltage	V_{CC} = 2.3V to 3.6V	I_{OL} = 0.1mA	—	0.2	V
		V_{CC} = 2.3V	I_{OL} = 6mA	—	0.4	
			I_{OL} = 12mA	—	0.7	
		V_{CC} = 2.7V	I_{OL} = 12mA	—	0.4	
		V_{CC} = 3.0V	I_{OL} = 24mA	—	0.55	

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NOTE:

1. V_{IH} and V_{IL} must be within the min. or max. range shown in the DC ELECTRICAL CHARACTERISTICS OVER OPERATING RANGE table for the appropriate V_{CC} range. T_A = – 40°C to +85°C.

OPERATING CHARACTERISTICS, V_{CC} = 3.3V ± 0.3V, T_A = 25°C

Symbol	Parameter	Test Conditions	Typical	Unit
C_{PD}	Power Dissipation Capacitance per bus exchanger Outputs enabled	C_L = 0pF, f = 10Mhz		pF
C_{PD}	Power Dissipation Capacitance per bus exchanger Outputs disabled			pF

SWITCHING CHARACTERISTICS (1)

Symbol	Parameter		Vcc = 2.7V		Vcc = 3.3V±0.3V		Unit
			Min.	Max.	Min.	Max.	
t_{PLH} t_{PHL}	Propagation Delay CLK to 1Bx or CLK to 2Bx		1.5	6.6	1.5	5.7	ns
t_{PLH} t_{PHL}	Propagation Delay CLK to Ax	SEL Stable $\overline{CExB}$ Enabled	1.5	7	1.5	5.8	ns
		SEL Changing $\overline{CExB}$ Disabled	1.5	7.5	1.5	6.5	ns
		SEL Changing $\overline{CExB}$ Enabled	1.5	7.6	1.5	6.6	ns
t_{PZH} t_{PZL}	Output Enable Time CLK to Ax, CLK to 1Bx, or CLK to 2Bx		1.5	6.8	1.5	5.8	ns
t_{PHZ} t_{PLZ}	Output Disable Time CLK to Ax, CLK to 1Bx, or CLK to 2Bx		1.5	6.6	1.5	6.6	ns
t_{SU}	Set-Up Time, HIGH or LOW Data to CLK		1.5	—	1.5	—	ns
t_{SU}	Set-Up Time, $\overline{OEA}$ to CLK, $\overline{OEB}$ to CLK		1.5	—	1.5	—	ns
t_{SU}	Set-Up Time, SEL to CLK		1.5	—	1.5	—	ns
t_{SU}	Set-Up Time, $\overline{CEA1B}$ to CLK, $\overline{CE1B}$ to CLK $\overline{CE2B}$ to CLK, or $\overline{CEA2B}$ to CLK		1.8	—	1.8	—	ns
t_H	Hold Time, CLK to Data		1	—	1	—	ns
t_H	Hold Time, CLK to $\overline{OEA}$, CLK to $\overline{OEB}$, CLK to SEL		1	—	1	—	ns
t_H	Hold Time, CLK to $\overline{CEA1B}$, CLK to $\overline{CE1B}$, CLK to $\overline{CE2B}$, CLK to $\overline{CEA2B}$		0.7	—	0.7	—	ns
t_W	Pulse Width, CLK HIGH		2.5	—	2.5	—	ns
$t_{SK(o)}$	Output Skew(2)		—	500	—	500	ps

NOTES:
1. See test circuits and waveforms. T_A = – 40°C to + 85°C.
2. Skew between any two outputs of the same package and switching in the same direction.

TEST CIRCUITS AND WAVEFORMS

TEST CONDITIONS

Symbol	$V_{CC}^{(1)}$= 3.3V ±0.3V	$V_{CC}^{(1)}$ = 2.7V	$V_{CC}^{(2)}$= 2.5V ±0.2V	Unit
V_{LOAD}	6	6	2 x Vcc	V
V_{IH}	2.7	2.7	Vcc	V
V_T	1.5	1.5	Vcc / 2	V
V_{LZ}	300	300	150	mV
V_{HZ}	300	300	150	mV
C_L	50	50	30	pF

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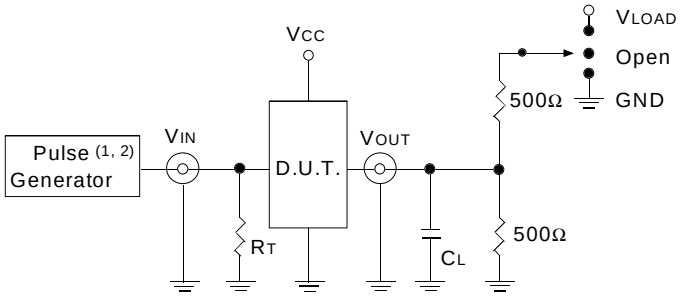
TEST CIRCUITS FOR ALL OUTPUTS



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DEFINITIONS:
C_L = Load capacitance: includes jig and probe capacitance.
R_T = Termination resistance: should be equal to Z_{OUT} of the Pulse Generator.

NOTE:
1. Pulse Generator for All Pulses: Rate ≤ 10MHz; t_F ≤ 2.5ns; t_R ≤ 2.5ns.
2. Pulse Generator for All Pulses: Rate ≤ 10MHz; t_F ≤ 2ns; t_R ≤ 2ns.

SWITCH POSITION

Test	Switch
Open Drain Disable Low Enable Low	V_{LOAD}
Disable High Enable High	GND
All Other tests	Open

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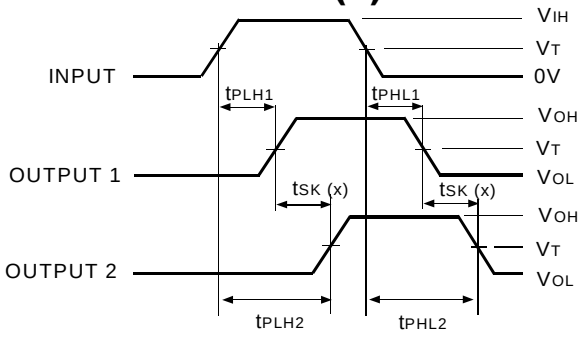
OUTPUT SKEW - tsk (x)



$t_{SK(x)} = |t_{PLH2} - t_{PLH1}|$ or $|t_{PHL2} - t_{PHL1}|$

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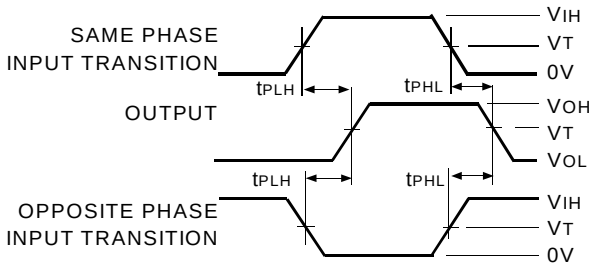
NOTES:
1. For t_{SK}(o) OUTPUT1 and OUTPUT2 are any two outputs.
2. For t_{SK}(b) OUTPUT1 and OUTPUT2 are in the same bank.

PROPAGATION DELAY



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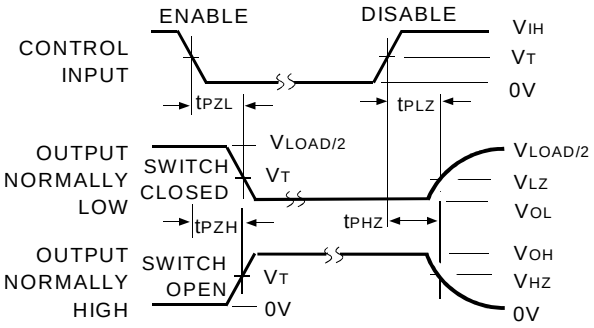
ENABLE AND DISABLE TIMES



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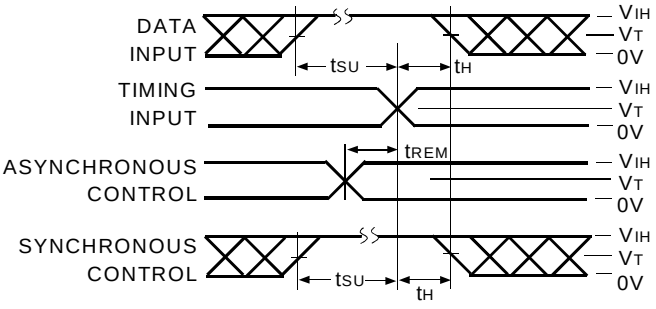
NOTE:
1. Diagram shown for input Control Enable-LOW and input Control Disable-HIGH.

SET-UP, HOLD, AND RELEASE TIMES



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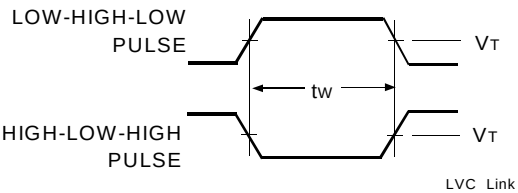
PULSE WIDTH



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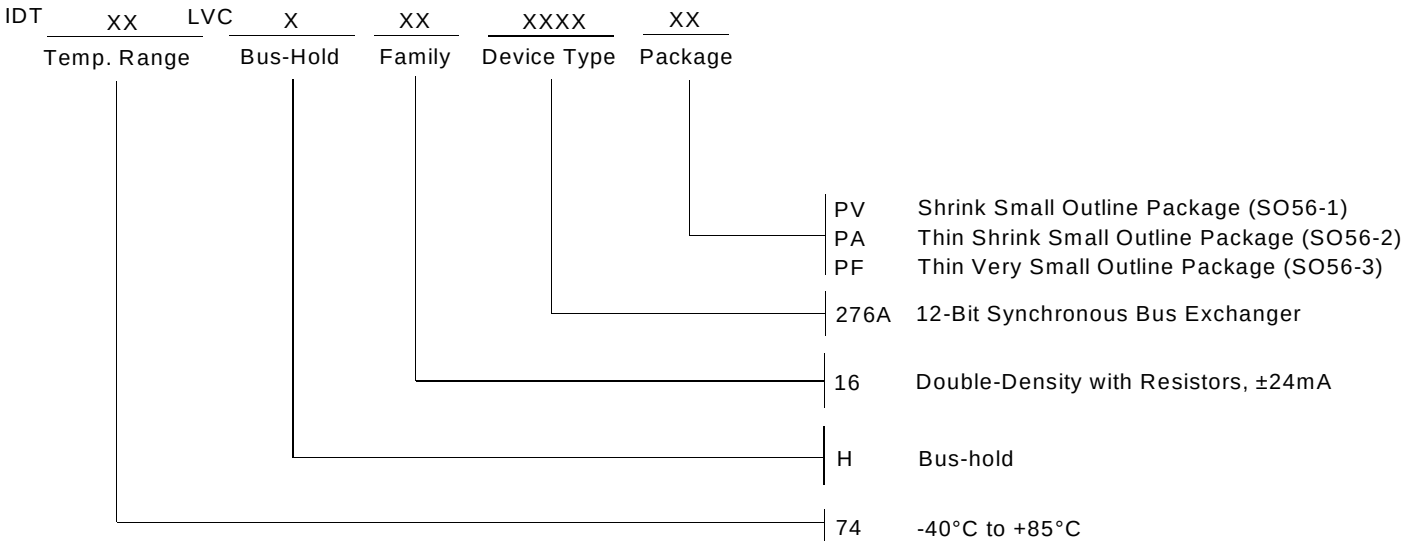
ORDERING INFORMATION



CORPORATE HEADQUARTERS
2975 Stender Way
Santa Clara, CA 95054

for SALES:
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