

3.3V CMOS OCTAL TRANSCEIVER WITH DUAL ENABLE, 3-STATE OUTPUTS, AND 5 VOLT TOLERANT I/O

FEATURES:

- 0.5 MICRON CMOS Technology
- ESD > 2000V per MIL-STD-883, Method 3015;
 > 200V using machine model (C = 200pF, R = 0)
- 1.27mm pitch SOIC, 0.65mm pitch SSOP, 0.635mm pitch QSOP, 0.65mm pitch TSSOP packages
- Extended commercial range of 40°C to +85°C
- VCC = 3.3V ±0.3V, Normal Range
- Vcc = 2.3V to 3.6V, Extended Range
- CMOS power levels (0.4µW typ. static)
- Rail-to-Rail output swing for increased noise margin
- All inputs, outputs and I/O are 5 Volt tolerant
- Supports hot insertion

Drive Features for LVC623A:

- High Output Drivers: ±24mA
- Reduced system switching noise

APPLICATIONS:

- 5V and 3.3V mixed voltage systems
- Data communication and telecommunication systems

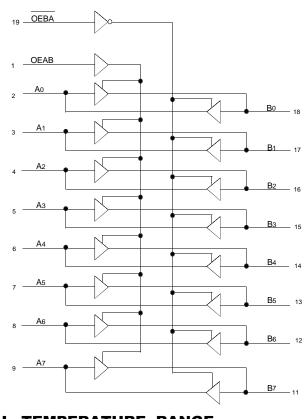
DESCRIPTION:

This octal transceiver is built using advanced dual metal CMOS technology. This high-speed, low power transceiver is ideal for asynchronous communication between two busses (A and B). The control function implementation allows maximum flexibility in timing. This device allows data transmission from the A bus to the B bus, or from the B bus to the A bus, depending upon the levels at the enable inputs (OEAB, OEBA). The enable inputs can be used to disable the device so that the buses are effectively isolated. The capability to store data by simultaneous enabling of OEAB and OEBA. Each output reinforces its input in this transceiver configuration. Thus, when both control inputs are enabled and all other data sources to the two sets of the bus lines are at high impedence OFF-state, both sets of bus lines will remain at their last states. The 8-bit codes appearing on the two sets of buses will be identical.

The LVC623A has been designed with a \pm 24mA output driver. This driver is capable of driving a moderate to heavy load while maintaining speed performance.

All pins can be driven from either 3.3V or 5V devices. This feature allows the use of this device as a translator in a mixed 3.3V/5V supply system.

FUNCTIONAL BLOCK DIAGRAM

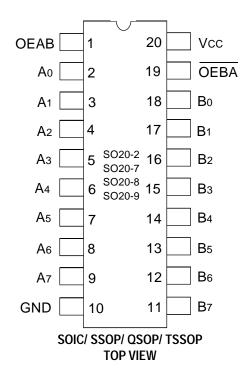


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EXTENDED COMMERCIAL TEMPERATURE RANGE

OCTOBER 1999

PIN CONFIGURATION



ABSOLUTE MAXIMUM RATINGS (1)

Symbol	Description	Max.	Unit
VTERM	Terminal Voltage with Respect to GND	– 0.5 to +6.5	V
Tstg	Storage Temperature	– 65 to +150	°C
Ιουτ	DC Output Current	– 50 to +50	mA
Ік	Continuous Clamp Current,	- 50	mA
Іок	$V_{I} < 0 \text{ or } V_{O} < 0$		
Icc	Continuous Current through	±100	mA
lss	each Vcc or GND		
			8LVC

NOTE:

 Stresses greater than those listed under ABSOLUTE MAXIMUM RATINGS may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect reliability.

CAPACITANCE (TA = +25°C, f = 1.0MHz)

Symbol	Parameter ⁽¹⁾	Conditions	Тур.	Max.	Unit
CIN	Input Capacitance	VIN = 0V	4.5	6	pF
Соит	Output Capacitance	Vout = 0V	5.5	8	pF
Сі/о	I/O Port Capacitance	VIN = 0V	6.5	8	pF

NOTE:

1. As applicable to the device type.

PIN DESCRIPTION

Pin Names	Description	
OEBA	Output Enable Input A Port (Active LOW)	
OEAB	Output Enable Input B Port	
Ах	Side A Inputs or 3-State Outputs	
Вх	Side B Inputs or 3-State Outputs	
GND	Ground (0V)	
Vcc	Positive Power Supply Voltage	

FUNCTION TABLE (1)

Inj	outs	Inputs/	Outputs
OEAB	OEBA	Ах	Вх
L	L	A = B	Inputs
Н	Н	Inputs	B = A
L	Н	Z	Z
Н	L	A = B	Inputs B = A
		Inputs	B = A

NOTE:

1. H = HIGH Voltage Level

L = LOW Voltage Level

X = Don't Care

Z = High-Impedance

DC ELECTRICAL CHARACTERISTICS OVER OPERATING RANGE

Following Conditions Apply Unless Otherwise Specified: Operating Condition: TA = -40° C To $+85^{\circ}$ C

Symbol	Parameter		Test Conditions	Min.	Typ. ⁽¹⁾	Max.	Unit
Vih	Input HIGH Voltage Level	Vcc = 2.3V to 2.7V		1.7	_	_	V
		Vcc = 2.7V to 3.6V		2	_	_	
VIL	Input LOW Voltage Level	Vcc = 2.3V to 2.7V		_	_	0.7	V
		Vcc = 2.7V to 3.6V		_	_	0.8	
lih lil	Input Leakage Current	Vcc = 3.6V	VI = 0 to 5.5V	_	_	±5	μA
Іоzн	High Impedance Output Current	Vcc = 3.6V	Vo = 0 to 5.5V	_	_	±10	μA
Iozl	(3-State Output pins)						
IOFF	Input/Output Power Off Leakage	$V_{CC} = 0V$, V_{IN} or $V_O \le 5.5V$		_	_	±50	μA
Vik	Clamp Diode Voltage	VCC = 2.3V, IIN = - 7	18mA	_	- 0.7	- 1.2	V
Vн	Input Hysteresis	Vcc = 3.3V		_	100		mV
ICCL ICCH	Quiescent Power Supply Current	Vcc = 3.6V	VIN = GND or Vcc	_	—	10	μA
lccz			$3.6 \le VIN \le 5.5V^{(2)}$	_	_	10	
Δlcc	Quiescent Power Supply Current Variation	One input at Vcc - 0.6V, other inputs at Vcc or GND Vcc = 3.0 - 3.6V		-	—	500	μA 8LVC Link

NOTES:

1. Typical values are at Vcc = 3.3V, +25°C ambient.

2. This applies in the disabled state only.

OUTPUT DRIVE CHARACTERISTICS

Symbol	Parameter	Test Conditions ⁽¹⁾		Min.	Max.	Unit
Vон	Output HIGH Voltage	Vcc = 2.3V to 3.6V	Iон = – 0.1mA	Vcc – 0.2	_	V
		Vcc = 2.3V	Iон = – 6mA	2	_	
		Vcc = 2.3V	Iон = – 12mA	1.7	_	
		Vcc = 2.7V		2.2	_	
		Vcc = 3.0V		2.4	_	
		Vcc = 3.0V	Iон = – 24mA	2.2	_	
Vol	Output LOW Voltage	Vcc = 2.3V to 3.6V	Iol = 0.1mA	_	0.2	V
		Vcc = 2.3V	Iol = 6mA	_	0.4	
			Iol = 12mA	_	0.7	
		Vcc = 2.7V	Iol = 12mA	_	0.4	
		Vcc = 3.0V	Iol = 24mA	—	0.55	
	•	•	•	•	•	8LVC Link

NOTE:

1. VIH and VIL must be within the min. or max. range shown in the DC ELECTRICAL CHARACTERISTICS OVER OPERATING RANGE table for the appropriate Vcc range. TA = − 40°C to +85°C.

OPERATING CHARACTERISTICS, $T_A = 25^{\circ}C$

			Vcc = 2.5V±0.2V	Vcc = 3.3V±0.3V	Unit
Symbol	Parameter	Test Conditions	Typical	Typical	
Cpd	Power dissipation capacitance per transceiver outputs enabled	CL = 0pF, f = 10Mhz	_	—	pF
Cpd	Power dissipation capacitance per transceiver outputs disabled		_	_	pF

SWITCHING CHARACTERISTICS (1)

		Vcc = 2.5V±0.2V		Vcc =	= 2.7V	Vcc = 3.	3V±0.3V	
Symbol	Parameter	Min.	Max.	Min.	Max.	Min.	Max.	Unit
tplh tphl	Propagation Delay Ax to Bx, Bx to Ax	—	—	1.5	7	1.5	6	ns
tpzh tpzl	Output Enable Time OEAB to Bx	—	—	1.5	8.6	1.5	7.6	ns
tphz tplz	Output Disable Time OEAB to Bx	_	—	1.5	7.5	1.5	6.5	ns
tPZH tPZL	Output Enable Time	_	—	1.5	8.9	1.5	7.9	ns
tphz tplz	Output Disable Time OEBA to Ax	_	_	1.5	7.5	1.5	6.5	ns
tsk(o)	Output Skew ⁽²⁾	_	—	—	_	_	500	ps

NOTES:

1. See test circuits and waveforms. TA = -40° C to $+85^{\circ}$ C.

2. Skew between any two outputs of the same package and switching in the same direction.

IDT74LVC623A 3.3V CMOS OCTAL TRANSCEIVER WITH DUAL ENABLE

EXTENDEDCOMMERCIALTEMPERATURERANGE

Vін

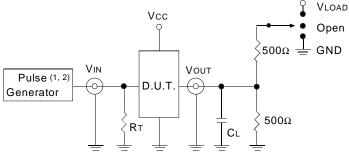
Vт

TEST CIRCUITS AND WAVEFORMS

TEST CONDITIONS

$V_{CC}^{(1)} = 3.3V \pm 0.3V$	$V_{CC}^{(1)} = 2.7V$	Vcc ⁽²⁾ = 2.5V ±0.2V	Unit
6	6	2 x Vcc	٧
2.7	2.7	Vcc	۷
1.5	1.5	Vcc/2	۷
300	300	150	mV
300	300	150	mV
50	50	30	pF
	6 2.7 1.5 300 300	6 6 2.7 2.7 1.5 1.5 300 300 300 300	6 6 2 x Vcc 2.7 2.7 Vcc 1.5 1.5 Vcc / 2 300 300 150 300 300 150

TEST CIRCUITS FOR ALL OUTPUTS



LVC Link

DEFINITIONS:

- CL= Load capacitance: includes jig and probe capacitance.
- RT = Termination resistance: should be equal to ZOUT of the Pulse Generator.

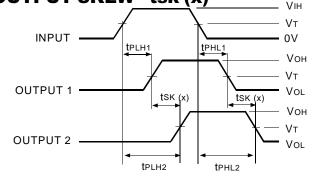
NOTES:

- 1. Pulse Generator for All Pulses: Rate \leq 10MHz: tF \leq 2.5ns: tR \leq 2.5ns.
- 2. Pulse Generator for All Pulses: Rate \leq 10MHz; tF \leq 2ns; tR \leq 2ns.

SWITCH POSITION

Test	Switch
Open Drain	Vload
Disable Low	
Enable Low	
Disable High	GND
Enable High	
All Other tests	Open 8LVC Link

OUTPUT SKEW - tsk (x)



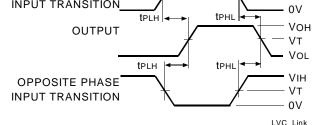
tSK(x) = |tPLH2 - tPLH1| or |tPHL2 - tPHL1|

NOTES:

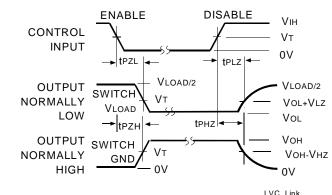
1. For tsk(o) OUTPUT1 and OUTPUT2 are any two outputs.

For tsk(b) OUTPUT1 and OUTPUT2 are in the same bank.





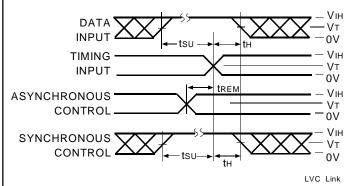
ENABLE AND DISABLE TIMES



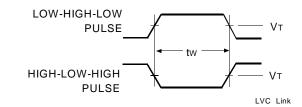
NOTE:

1. Diagram shown for input Control Enable-LOW and input Control Disable-HIGH.

SET-UP, HOLD, AND RELEASE TIMES

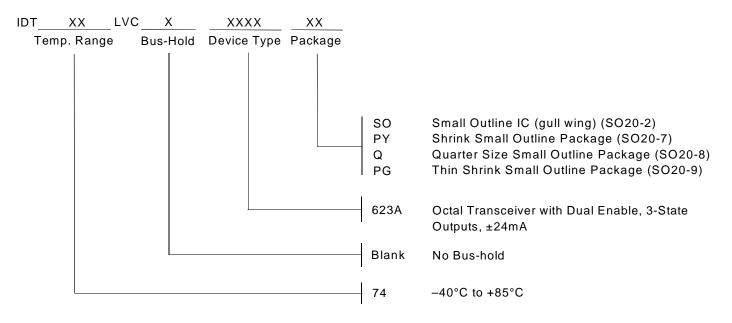


PULSEWIDTH



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ORDERING INFORMATION





CORPORATE HEADQUARTERS 2975 Stender Way Santa Clara, CA 95054 for SALES: 800-345-7015 or 408-727-6116 fax: 408-492-8674 www.idt.com*

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