



3.3V CMOS OCTAL BUS TRANSCIVER AND REGISTER WITH 3-STATE OUT- PUTS AND 5 VOLT TOLERANT I/O

IDT74LVC2952A

FEATURES:

- 0.5 MICRON CMOS Technology
- ESD > 2000V per MIL-STD-883, Method 3015;
> 200V using machine model (C = 200pF, R = 0)
- 1.27mm pitch SOIC, 0.65mm pitch SSOP,
0.635mm pitch QSOP, 0.65mm pitch TSSOP packages
- Extended commercial range of -40°C to $+85^{\circ}\text{C}$
- $V_{CC} = 3.3\text{V} \pm 0.3\text{V}$, Normal Range
- $V_{CC} = 2.3\text{V}$ to 3.6V , Extended Range
- CMOS power levels ($0.4\mu\text{W}$ typ. static)
- Rail-to-Rail output swing for increased noise margin
- All inputs, outputs and I/O are 5 Volt tolerant
- Supports hot insertion

Drive Feature for LVC2952A:

- Balanced Output Drivers: $\pm 24\text{mA}$

APPLICATIONS:

- 5V and 3.3V mixed voltage systems
- Data communication and telecommunication systems

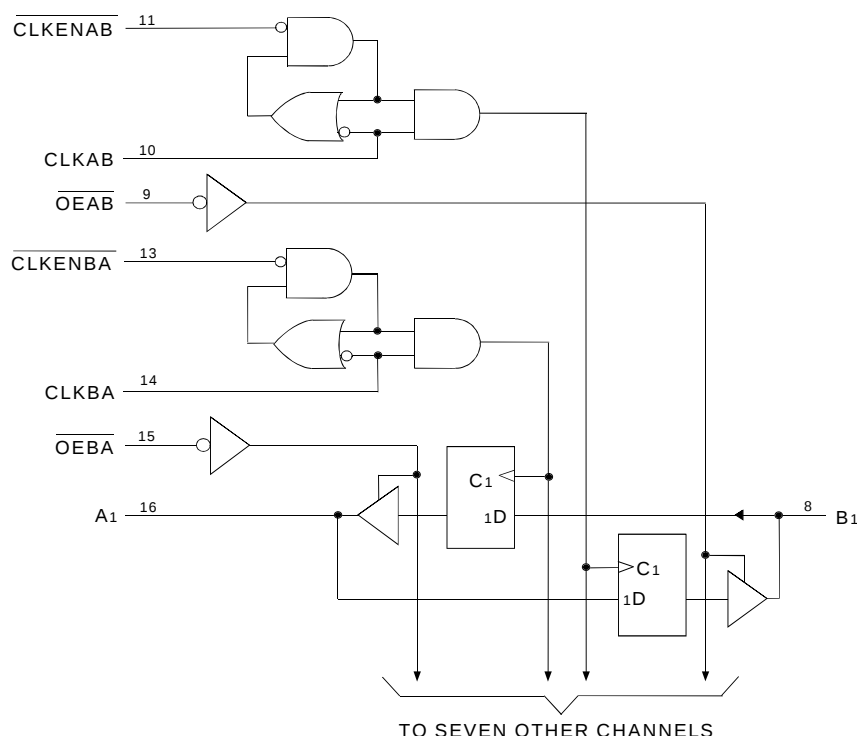
DESCRIPTION:

The LVC2952A octal bus transceiver and register is built using advanced dual metal CMOS technology. This high speed low power device is organized as 8-bit back-to-back registers with separate input and output control for independent control of data flow in either direction. Data on the A or B bus is stored in the registers on the low-to-high transition of the clock (CLKAB or CLKBA) input, provided that the clock-enable ($\overline{\text{CLKENAB}}$ or $\overline{\text{CLKENBA}}$) input is low. Taking the output-enable ($\overline{\text{OEAB}}$ or $\overline{\text{OEBA}}$) input low accesses the data of either port.

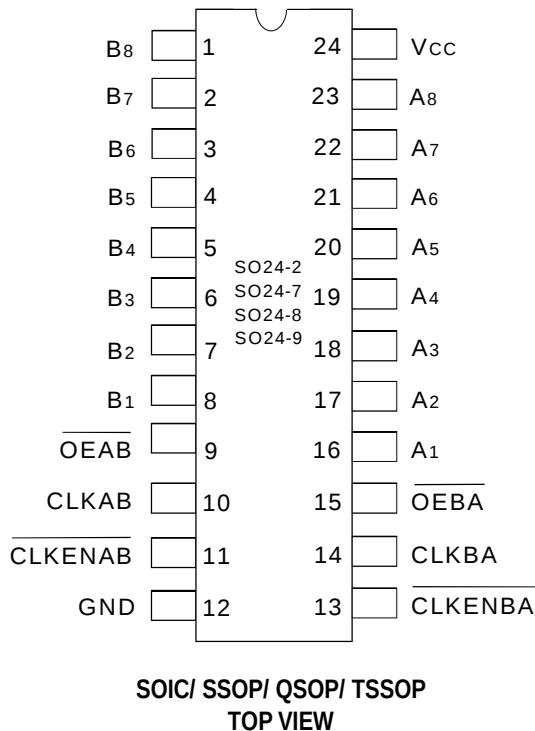
All pins can be driven from either 3.3V or 5V devices. This feature allows the use of this device as a translator in a mixed 3.3V/5V system environment.

The LVC2952A has been designed with a $\pm 24\text{mA}$ output driver. This driver is capable of driving a moderate to heavy load while maintaining speed performance.

FUNCTIONAL BLOCK DIAGRAM



PIN CONFIGURATION



FUNCTION TABLE (1, 2)

Inputs				Outputs
CLKENAB	CLKAB	OEAB	Ax	Bx
H	X	L	X	B ₀ ⁽³⁾
X	H or L	L	X	B ₀ ⁽³⁾
L	↑	L	L	L
L	↑	L	H	H
X	X	H	X	Z

NOTES:

- H = HIGH Voltage Level
L = LOW Voltage Level
X = Don't Care
Z = High-Impedance
↑ = LOW-to-HIGH Transition
- A-to-B data flow is shown; B-to-A flow control is similar but uses CLKENBA, CLKBA, and OEBA.
- B₀ = Level of B before the indicated steady-state input conditions were established.

ABSOLUTE MAXIMUM RATINGS ⁽¹⁾

Symbol	Description	Max.	Unit
VTERM ⁽²⁾	Terminal Voltage with Respect to GND	– 0.5 to +6.5	V
VTERM ⁽³⁾	Terminal Voltage with Respect to GND	– 0.5 to +6.5	V
TSTG	Storage Temperature	– 65 to +150	°C
I _{OUT}	DC Output Current	– 50 to +50	mA
I _{IK} I _{OK}	Continuous Clamp Current, V _I < 0 or V _O < 0	– 50	mA
I _{CC} I _{SS}	Continuous Current through each V _{CC} or GND	±100	mA

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NOTES:

- Stresses greater than those listed under ABSOLUTE MAXIMUM RATINGS may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect reliability.
- V_{CC} terminals.
- All terminals except V_{CC}.

CAPACITANCE (T_A = +25°C, f = 1.0MHz)

Symbol	Parameter ⁽¹⁾	Conditions	Typ.	Max.	Unit
C _{IN}	Input Capacitance	V _{IN} = 0V	4.5	6	pF
C _{OUT}	Output Capacitance	V _{OUT} = 0V	5.5	8	pF
C _{I/O}	I/O Port Capacitance	V _{IN} = 0V	6.5	8	pF

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NOTE:

- As applicable to the device type.

PIN DESCRIPTION

Pin Names	Description
OEAB	A-to-B Output Enable Input (Active LOW)
OEBA	B-to-A Output Enable Input (Active LOW)
CLKENAB	A-to-B Clock Enable Input (Active LOW)
CLKENBA	B-to-A Clock Enable Input (Active LOW)
CLKAB	A-to-B Clock Input
CLKBA	B-to-A Clock Input
Ax	A-to-B Data Inputs or B-to-A 3-State Outputs
Bx	B-to-A Data Inputs or A-to-B 3-State Outputs

DC ELECTRICAL CHARACTERISTICS OVER OPERATING RANGE

Following Conditions Apply Unless Otherwise Specified:

Operating Condition: $T_A = -40^{\circ}\text{C}$ To $+85^{\circ}\text{C}$

Symbol	Parameter	Test Conditions		Min.	Typ. ⁽¹⁾	Max.	Unit
V_{IH}	Input HIGH Voltage Level	$V_{CC} = 2.3\text{V}$ to 2.7V		1.7	—	—	V
		$V_{CC} = 2.7\text{V}$ to 3.6V		2	—	—	
V_{IL}	Input LOW Voltage Level	$V_{CC} = 2.3\text{V}$ to 2.7V		—	—	0.7	V
		$V_{CC} = 2.7\text{V}$ to 3.6V		—	—	0.8	
I_{IH} I_{IL}	Input Leakage Current	$V_{CC} = 3.6\text{V}$	$V_I = 0$ to 5.5V	—	—	± 5	μA
I_{OZH} I_{OZL}	High Impedance Output Current (3-State Output pins)	$V_{CC} = 3.6\text{V}$	$V_O = 0$ to 5.5V	—	—	± 10	μA
I_{OFF}	Input/Output Power Off Leakage	$V_{CC} = 0\text{V}$, V_{IN} or $V_O \leq 5.5\text{V}$		—	—	± 50	μA
V_{IK}	Clamp Diode Voltage	$V_{CC} = 2.3\text{V}$, $I_{IN} = -18\text{mA}$		—	-0.7	-1.2	V
V_H	Input Hysteresis	$V_{CC} = 3.3\text{V}$		—	100	—	mV
I_{CCL} I_{CCH} I_{CCZ}	Quiescent Power Supply Current	$V_{CC} = 3.6\text{V}$	$V_{IN} = \text{GND}$ or V_{CC}	—	—	10	μA
			$3.6 \leq V_{IN} \leq 5.5\text{V}^{(2)}$	—	—	10	
ΔI_{CC}	Quiescent Power Supply Current Variation	One input at $V_{CC} - 0.6\text{V}$, other inputs at V_{CC} or GND		—	—	500	μA

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NOTES:

- Typical values are at $V_{CC} = 3.3\text{V}$, $+25^{\circ}\text{C}$ ambient.
- This applies in the disabled state only.

OUTPUT DRIVE CHARACTERISTICS

Symbol	Parameter	Test Conditions ⁽¹⁾		Min.	Max.	Unit
V_{OH}	Output HIGH Voltage	$V_{CC} = 2.3\text{V}$ to 3.6V	$I_{OH} = -0.1\text{mA}$	$V_{CC} - 0.2$	—	V
		$V_{CC} = 2.3\text{V}$	$I_{OH} = -6\text{mA}$	2	—	
		$V_{CC} = 2.3\text{V}$	$I_{OH} = -12\text{mA}$	1.7	—	
		$V_{CC} = 2.7\text{V}$		2.2	—	
		$V_{CC} = 3.0\text{V}$		2.4	—	
		$V_{CC} = 3.0\text{V}$	$I_{OH} = -24\text{mA}$	2.2	—	
V_{OL}	Output LOW Voltage	$V_{CC} = 2.3\text{V}$ to 3.6V	$I_{OL} = 0.1\text{mA}$	—	0.2	V
		$V_{CC} = 2.3\text{V}$	$I_{OL} = 6\text{mA}$	—	0.4	
			$I_{OL} = 12\text{mA}$	—	0.7	
		$V_{CC} = 2.7\text{V}$	$I_{OL} = 12\text{mA}$	—	0.4	
		$V_{CC} = 3.0\text{V}$	$I_{OL} = 24\text{mA}$	—	0.55	

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NOTE:

- V_{IH} and V_{IL} must be within the min. or max. range shown in the DC ELECTRICAL CHARACTERISTICS OVER OPERATING RANGE table for the appropriate V_{CC} range. $T_A = -40^{\circ}\text{C}$ to $+85^{\circ}\text{C}$.

OPERATING CHARACTERISTICS, $V_{CC} = 3.3V \pm 0.3V$, $T_A = 25^\circ C$

Symbol	Parameter	Test Conditions	Typical	Unit
CPD	Power Dissipation Capacitance per Transceiver Outputs enabled	$C_L = 0$, $f = 10\text{MHz}$	79	pF
CPD	Power Dissipation Capacitance per Transceiver Outputs disabled		41	pF

SWITCHING CHARACTERISTICS ⁽¹⁾

Symbol	Parameter	$V_{CC} = 2.5V \pm 0.2V$		$V_{CC} = 2.7V$		$V_{CC} = 3.3V \pm 0.3V$		Unit
		Min.	Max.	Min.	Max.	Min.	Max.	
f_{MAX}		—	—	150	—	150	—	MHz
t_{PLH} t_{PHL}	Propagation Delay CLKAB or CLKBA to Bx or Ax	—	—	—	8.8	1	8.2	ns
t_{PZH} t_{PZL}	Output Enable Time $\overline{OEBA}$ or $\overline{OEAB}$ to Ax or Bx	—	—	—	9	1	7.8	ns
t_{PHZ} t_{PLZ}	Output Disable Time $\overline{OEBA}$ or $\overline{OEAB}$ to Ax or Bx	—	—	—	8.8	1	7.8	ns
t_{SU}	Set-up Time, Data Before CLK $\uparrow$ HIGH	—	—	1.7	—	1.3	—	ns
t_H	Hold Time, Data After CLK $\uparrow$ HIGH	—	—	1.8	—	1.1	—	ns
t_{SU}	Set-up Time, $\overline{CLKEN}$ Before CLK $\uparrow$ HIGH	—	—	1.3	—	1.1	—	ns
t_H	Hold Time, $\overline{CLKEN}$ After CLK $\uparrow$ HIGH	—	—	1.4	—	1.1	—	ns
t_W	Pulse Duration, CLK HIGH or LOW	—	—	3.3	—	3.3	—	ns
$t_{SK(0)}$	Output Skew ⁽²⁾	—	—	—	—	—	1	ns

NOTES:

1. See test circuits and waveforms. $T_A = -40^\circ C$ to $+85^\circ C$.
2. Skew between any two outputs of the same package and switching in the same direction.

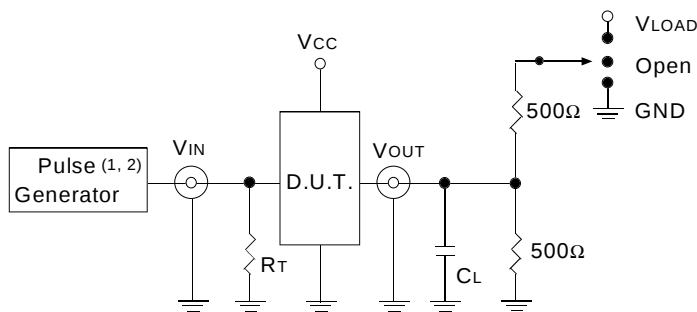
TEST CIRCUITS AND WAVEFORMS

TEST CONDITIONS

Symbol	V _{CC} (1) = 3.3V ± 0.3V	V _{CC} (1) = 2.7V	V _{CC} (2) = 2.5V ± 0.2V	Unit
V _{LOAD}	6	6	2 x V _{CC}	V
V _{IH}	2.7	2.7	V _{CC}	V
V _T	1.5	1.5	V _{CC} / 2	V
V _{LZ}	300	300	150	mV
V _{HZ}	300	300	150	mV
C _L	50	50	30	pF

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TEST CIRCUITS FOR ALL OUTPUTS



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DEFINITIONS:

C_L = Load capacitance: includes jig and probe capacitance.

R_T = Termination resistance: should be equal to Z_{OUT} of the Pulse Generator.

NOTES:

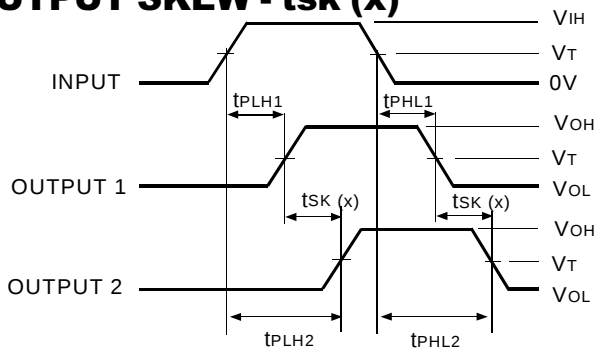
1. Pulse Generator for All Pulses: Rate ≤ 10MHz; t_F ≤ 2.5ns; t_R ≤ 2.5ns.
2. Pulse Generator for All Pulses: Rate ≤ 10MHz; t_F ≤ 2ns; t_R ≤ 2ns.

SWITCH POSITION

Test	Switch
Open Drain Disable Low Enable Low	V _{LOAD}
Disable High Enable High	GND
All Other tests	Open

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OUTPUT SKEW - t_{SK}(x)



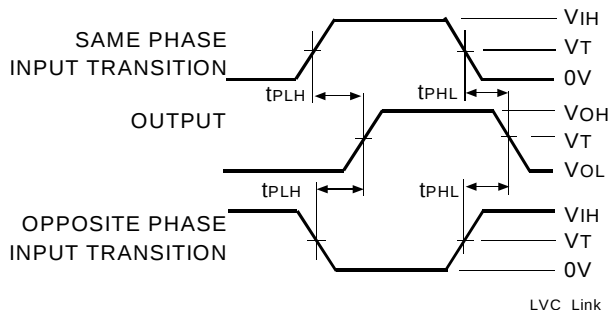
$$t_{SK}(x) = |t_{PLH2} - t_{PLH1}| \text{ or } |t_{PHL2} - t_{PHL1}|$$

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NOTES:

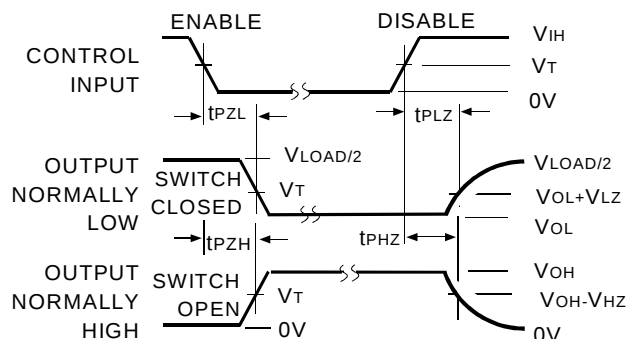
1. For t_{SK}(o) OUTPUT1 and OUTPUT2 are any two outputs.
2. For t_{SK}(b) OUTPUT1 and OUTPUT2 are in the same bank.

PROPAGATION DELAY



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ENABLE AND DISABLE TIMES

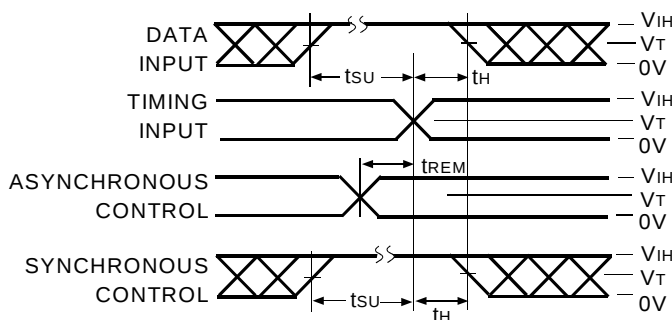


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NOTE:

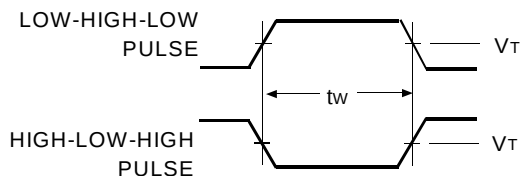
1. Diagram shown for input Control Enable-LOW and input Control Disable-HIGH.

SET-UP, HOLD, AND RELEASE TIMES



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PULSE WIDTH



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ORDERING INFORMATION

IDT	XX	LVC	X	XXXX	XX	
Temp. Range		Bus-Hold	Device Type		Package	
					SO	Small Outline IC (gull wing) (SO24-2)
					PY	Shrink Small Outline Package (SO24-7)
					Q	Quarter Size Small Outline Package (SO24-8)
					PG	Thin Shrink Small Outline Package (SO24-9)
				2952A		Octal Bus Transceiver and Register with 3-State Outputs, $\pm 24\text{mA}$
				Blank		No Bus-hold
				74		-40°C to $+85^{\circ}\text{C}$



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