



3.3V CMOS OCTAL D-TYPE FLIP-FLOP WITH RESET, POSITIVE EDGE TRIGGER, AND 5 VOLT TOLERANT I/O

IDT74LVC273A

FEATURES:

- 0.5 MICRON CMOS Technology
- ESD > 2000V per MIL-STD-883, Method 3015;
> 200V using machine model (C = 200pF, R = 0)
- 1.27mm pitch SOIC, 0.65mm pitch SSOP,
0.635mm pitch QSOP, 0.65mm pitch TSSOP packages
- Extended commercial range of – 40°C to +85°C
- Vcc = 3.3V ±0.3V, Normal Range
- Vcc = 2.3V to 3.6V, Extended Range
- CMOS power levels (0.4μW typ. static)
- Rail-to-Rail output swing for increased noise margin
- All inputs, outputs and I/O are 5 Volt tolerant
- Supports hot insertion

Drive Features for LVC273A:

- High Drive Output: ±24mA
- Reduced system switching noise

DESCRIPTION:

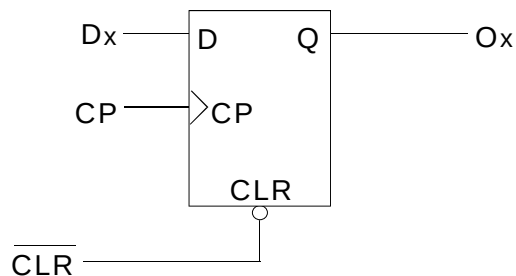
The octal D-type flip-flop with reset, positive edge trigger is built using advanced dual metal CMOS technology. This high-speed, low power device is ideal for driving high capacitance loads such as memory address and data buses.

All pins can be driven from either 3.3V or 5V devices. This feature allows the use of these devices as translators in a mixed 3.3V/5V supply system.

APPLICATIONS:

- 5V and 3.3V mixed voltage systems
- Data communication and telecommunication systems

FUNCTIONAL BLOCK DIAGRAM



PIN DESCRIPTION

Pin Names	Description
CLR	Clear Input
CP	Clock Input
Ox	Data Outputs
Dx	Data Inputs

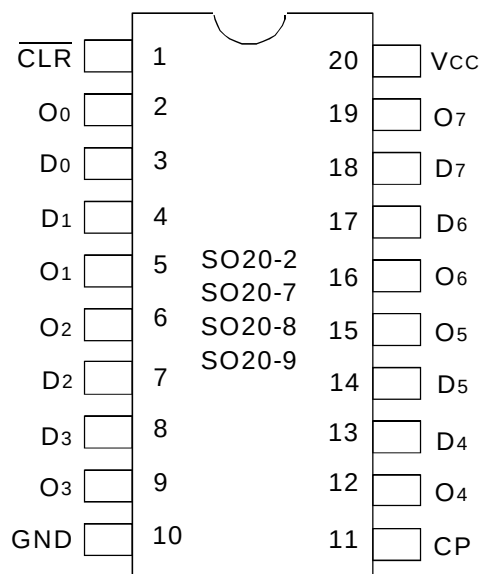
FUNCTION TABLE (1)

Inputs			Internal Q Value	Outputs Ox	Function
CLR	CP	Dx			
L	X	X	L	L	Clear Register
H	↑	L	L	L	Load Input Data
H	↑	H	H	H	Load Input Data

NOTE:

1. H = HIGH Voltage Level
L = LOW Voltage Level
X = Don't Care
↑ = LOW-to-HIGH Transition

PIN CONFIGURATION



SOIC/ SSOP/ QSOP/ TSSOP
TOP VIEW

ABSOLUTE MAXIMUM RATINGS ⁽¹⁾

Symbol	Description	Max.	Unit
V _{TERM} ⁽²⁾	Terminal Voltage with Respect to GND	– 0.5 to +6.5	V
V _{TERM} ⁽³⁾	Terminal Voltage with Respect to GND	– 0.5 to +6.5	V
T _{STG}	Storage Temperature	– 65 to +150	°C
I _{OUT}	DC Output Current	– 50 to +50	mA
I _{IK} I _{OK}	Continuous Clamp Current, V _I < 0 or V _O < 0	– 50	mA
I _{CC} I _{SS}	Continuous Current through each V _{CC} or GND	±100	mA

8LVC

NOTES:

- Stresses greater than those listed under ABSOLUTE MAXIMUM RATINGS may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect reliability.
- V_{CC} terminals.
- All terminals except V_{CC}.

CAPACITANCE (T_A = +25°C, f = 1.0MHz)

Symbol	Parameter ⁽¹⁾	Conditions	Typ.	Max.	Unit
C _{IN}	Input Capacitance	V _{IN} = 0V	4.5	6	pF
C _{OUT}	Output Capacitance	V _{OUT} = 0V	5.5	8	pF
C _{I/O}	I/O Port Capacitance	V _{IN} = 0V	6.5	8	pF

8LVC Link

NOTE:

- As applicable to the device type.

DC ELECTRICAL CHARACTERISTICS OVER OPERATING RANGE

Following Conditions Apply Unless Otherwise Specified:

Operating Condition: T_A = – 40°C To +85°C

Symbol	Parameter	Test Conditions		Min.	Typ. ⁽¹⁾	Max.	Unit
V _{IH}	Input HIGH Voltage Level	V _{CC} = 2.3V to 2.7V		1.7	—	—	V
		V _{CC} = 2.7V to 3.6V		2	—	—	
V _{IL}	Input LOW Voltage Level	V _{CC} = 2.3V to 2.7V		—	—	0.7	V
		V _{CC} = 2.7V to 3.6V		—	—	0.8	
I _{IH} I _{IL}	Input Leakage Current	V _{CC} = 3.6V	V _I = 0 to 5.5V	—	—	±5	μA
I _{OZH} I _{OZL}	High Impedance Output Current (3-State Output pins)	V _{CC} = 3.6V	V _O = 0 to 5.5V	—	—	±10	μA
I _{OFF}	Input/Output Power Off Leakage	V _{CC} = 0V, V _{IN} or V _O ≤ 5.5V		—	—	±50	μA
V _{IK}	Clamp Diode Voltage	V _{CC} = 2.3V, I _{IN} = – 18mA		—	– 0.7	– 1.2	V
V _H	Input Hysteresis	V _{CC} = 3.3V		—	100	—	mV
I _{CCL} I _{CCH} I _{CCZ}	Quiescent Power Supply Current	V _{CC} = 3.6V	V _{IN} = GND or V _{CC}	—	—	10	μA
			3.6 ≤ V _{IN} ≤ 5.5V ⁽²⁾	—	—	10	
ΔI _{CC}	Quiescent Power Supply Current Variation	One input at V _{CC} - 0.6V, other inputs at V _{CC} or GND		—	—	500	μA

8LVC Link

NOTES:

- Typical values are at V_{CC} = 3.3V, +25°C ambient.
- This applies in the disabled state only.

OUTPUT DRIVE CHARACTERISTICS

Symbol	Parameter	Test Conditions ⁽¹⁾		Min.	Max.	Unit
VOH	Output HIGH Voltage	VCC = 2.3V to 3.6V	IOH = – 0.1mA	VCC – 0.2	—	V
		VCC = 2.3V	IOH = – 6mA	2	—	
		VCC = 2.3V	IOH = – 12mA	1.7	—	
		VCC = 2.7V		2.2	—	
		VCC = 3.0V		2.4	—	
		VCC = 3.0V	IOH = – 24mA	2.2	—	
VOL	Output LOW Voltage	VCC = 2.3V to 3.6V	IOL = 0.1mA	—	0.2	V
		VCC = 2.3V	IOL = 6mA	—	0.4	
			IOL = 12mA	—	0.7	
		VCC = 2.7V	IOL = 12mA	—	0.4	
		VCC = 3.0V	IOL = 24mA	—	0.55	

8LVC Link

NOTE:

1. VIH and VIL must be within the min. or max. range shown in the DC ELECTRICAL CHARACTERISTICS OVER OPERATING RANGE table for the appropriate VCC range. TA = – 40°C to +85°C.

OPERATING CHARACTERISTICS, VCC = 3.3V ± 0.3V, TA = 25°C

Symbol	Parameter	Test Conditions	Typical	Unit
CPD	Power Dissipation Capacitance per transceiver Outputs enabled	CL = 0pF, f = 10Mhz	—	pF
CPD	Power Dissipation Capacitance per transceiver Outputs disabled		—	pF

SWITCHING CHARACTERISTICS ⁽¹⁾

Symbol	Parameter	VCC = 2.7V		VCC = 3.3V±0.3V		Unit
		Min.	Max.	Min.	Max.	
tPLH	Propagation Delay, CP to Ox	1.5	9.5	1.5	8.5	ns
tPHL	Propagation Delay, $\overline{\text{CLR}}$ to Ox	1.5	9.5	1.5	8.5	ns
ts	Data Setup Time, Dx to CP	2.5	—	2.5	—	ns
th	Data Hold Time, Dx to CP	1.5	—	1.5	—	ns
tREC	$\overline{\text{CLR}}$ Recovery Time, $\overline{\text{CLR}}$ to CP	2	—	2	—	ns
twCLR	$\overline{\text{CLR}}$ Pulse Width, LOW	3.3	—	3.3	—	ns
twCP	CLK Pulse Width, HIGH or LOW	3.3	—	3.3	—	ns
tsk(o)	Output Skew ⁽²⁾	—	—	—	500	ps

NOTES:

1. See test circuits and waveforms. TA = – 40°C to + 85°C.
2. Skew between any two outputs of the same package and switching in the same direction.

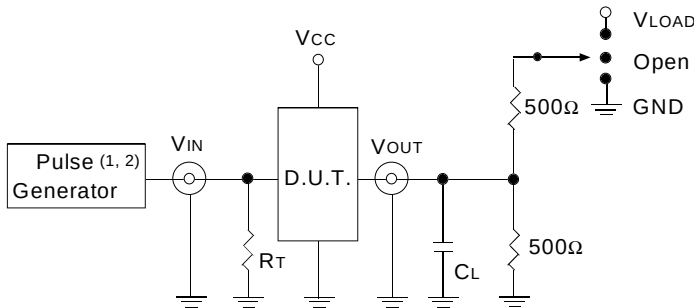
TEST CIRCUITS AND WAVEFORMS

TEST CONDITIONS

Symbol	V _{CC} (1) = 3.3V ± 0.3V	V _{CC} (1) = 2.7V	V _{CC} (2) = 2.5V ± 0.2V	Unit
V _{LOAD}	6	6	2 x V _{CC}	V
V _{IH}	2.7	2.7	V _{CC}	V
V _T	1.5	1.5	V _{CC} / 2	V
V _{LZ}	300	300	150	mV
V _{HZ}	300	300	150	mV
C _L	50	50	30	pF

8LVC Link

TEST CIRCUITS FOR ALL OUTPUTS



LVC Link

DEFINITIONS:

C_L = Load capacitance: includes jig and probe capacitance.

R_T = Termination resistance: should be equal to Z_{OUT} of the Pulse Generator.

NOTES:

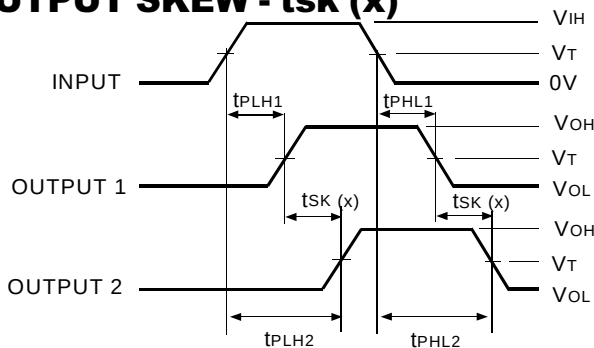
1. Pulse Generator for All Pulses: Rate ≤ 10MHz; t_F ≤ 2.5ns; t_R ≤ 2.5ns.
2. Pulse Generator for All Pulses: Rate ≤ 10MHz; t_F ≤ 2ns; t_R ≤ 2ns.

SWITCH POSITION

Test	Switch
Open Drain	V _{LOAD}
Disable Low	
Enable Low	
Disable High	GND
Enable High	
All Other tests	Open

8LVC Link

OUTPUT SKEW - t_{SK}(x)



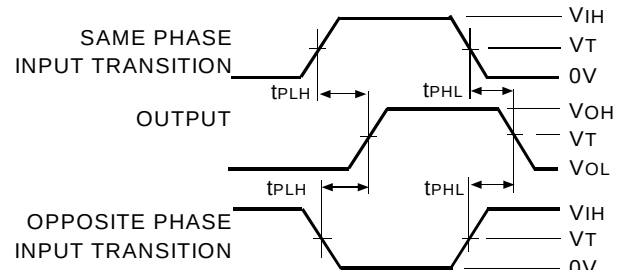
$$t_{SK}(x) = |t_{PLH2} - t_{PLH1}| \text{ or } |t_{PHL2} - t_{PHL1}|$$

LVC Link

NOTES:

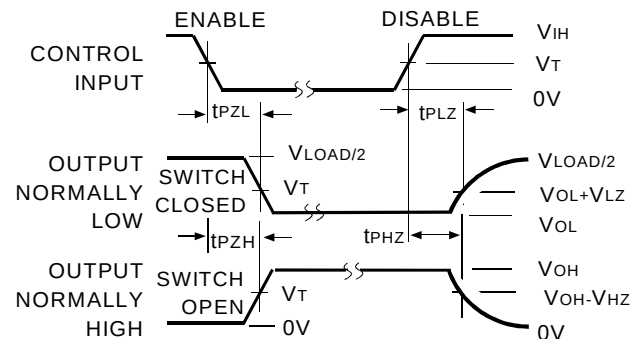
1. For t_{SK}(o) OUTPUT1 and OUTPUT2 are any two outputs.
2. For t_{SK}(b) OUTPUT1 and OUTPUT2 are in the same bank.

PROPAGATION DELAY



LVC Link

ENABLE AND DISABLE TIMES

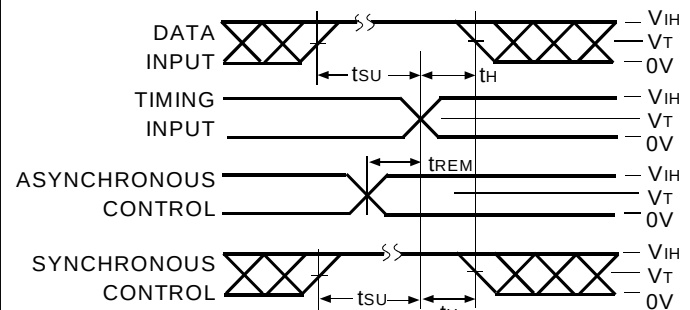


LVC Link

NOTE:

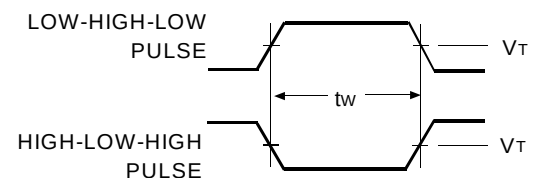
1. Diagram shown for input Control Enable-LOW and input Control Disable-HIGH.

SET-UP, HOLD, AND RELEASE TIMES



LVC Link

PULSE WIDTH



LVC Link

ORDERING INFORMATION

IDT	XX	LVC	X	XXXX	XX	
	Temp. Range		Bus-Hold	Device Type	Package	
					SO	Small Outline IC (gull wing) (SO20-2)
					PY	Shrink Small Outline Package (SO20-7)
					Q	Quarter Size Small Outline Package (SO20-8)
					PG	Thin Shrink Small Outline Package (SO20-9)
				273A		Octal D-Type Flip-Flop with Reset, Positive Edge Trigger, 5V Tolerant I/O
					Blank	No Bus-hold
					74	-40°C to +85°C



CORPORATE HEADQUARTERS
 2975 Stender Way
 Santa Clara, CA 95054

for SALES:
 800-345-7015 or 408-727-6116
 fax: 408-492-8674
www.idt.com*

*To search for sales office near you, please click the sales button found on our home page or dial the 800# above and press 2.
 The IDT logo is a registered trademark of Integrated Device Technology, Inc.