

# 3.3V CMOS OCTAL BUFFER/DRIVER WITH 3STATE OUTPUTS AND 5 VOLT TOLERANT I/O

### IDT74LVC2244A

### **FEATURES:**

- 0.5 MICRON CMOS Technology
- ESD > 2000V per MIL-STD-883, Method 3015;
  - > 200V using machine model (C = 200pF, R = 0)
- 1.27mm pitch SOIC, 0.65mm pitch SSOP, 0.635mm pitch QSOP, 0.65mm pitch TSSOP packages
- Extended commercial range of 40°C to +85°C
- $VCC = 3.3V \pm 0.3V$ , Normal Range
- Vcc = 2.3V to 3.6V, Extended Range
- CMOS power levels (0.4µW typ. static)
- Rail-to-Rail output swing for increased noise margin
- All inputs, outputs and I/O are 5 Volt tolerant
- Supports hot insertion

### **Drive Features for LVC2244A:**

- Balanced Output Drivers: ±12mA
- Low Switching Noise

# **APPLICATIONS:**

- 5V and 3.3V mixed voltage systems
- Data communication and telecommunication systems

### **DESCRIPTION:**

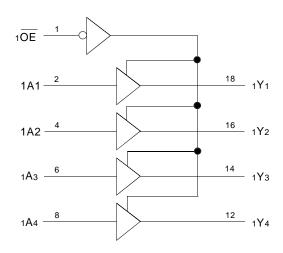
This octal buffer/driver is built using advanced dual metal CMOS technology. The LVC2244A device is organized as two 4-bit line drivers with separate output-enable ( $\overline{OE}$ ) inputs. When  $\overline{OE}$  is low, the device passes data from the A inputs to the Y outputs. When  $\overline{OE}$  is high, the outputs are in the high-impedance state.

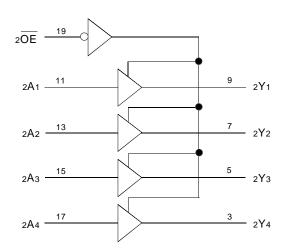
To ensure the high-impedance state during power up or power down,  $\overline{OE}$  should be tied to Vcc through a pullup resistor; the minimum value of the resistor is determined by the current-sinking capability of the driver.

The LVC2244A has series resistors in the device output structure which will significantly reduce line noise when used with light loads. This driver has been designed to drive  $\pm 12$ mA at the designated threshold levels.

Inputs can be driven from either 3.3V or 5V devices. This feature allows the use of this device as a translator in a mixed 3.3V/5V system environment.

# **FUNCTIONAL BLOCK DIAGRAM**

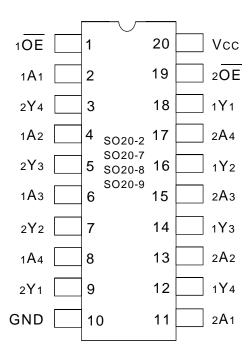




**EXTENDED COMMERCIAL TEMPERATURE RANGE** 

**FEBRUARY 2000** 

### **PIN CONFIGURATION**



SOIC/ SSOP/ QSOP/ TSSOP TOP VIEW

# **ABSOLUTE MAXIMUM RATINGS (1)**

Symbol	Description	Max.	Unit
VTERM	Terminal Voltage with Respect to GND	- 0.5 to +6.5	V
Tstg	Storage Temperature	- 65 to +150	°C
Іоит	DC Output Current	- 50 to +50	mA
lıĸ	Continuous Clamp Current,	- 50	mA
Іок	VI < 0 or Vo < 0		
Icc	Continuous Current through	±100	mA
Iss	each Vcc or GND		

### NOTE:

 Stresses greater than those listed under ABSOLUTE MAXIMUM RATINGS may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect reliability.

# **CAPACITANCE** (TA = +25°C, f = 1.0MHz)

Symbol	Parameter <sup>(1)</sup>	Conditions	Тур.	Max.	Unit
CIN	Input Capacitance	VIN = 0V	4.5	6	pF
Соит	Output Capacitance	Vout = 0V	5.5	8	pF
Ci/o	I/O Port Capacitance	VIN = 0V	6.5	8	pF
					8LVC Link

### NOTE:

1. As applicable to the device type.

### **PIN DESCRIPTION**

Pin Names	Description
xŌĒ	Output-enable Inputs
xAx	Data Inputs
хҮх	3-State Outputs

# FUNCTION TABLE (each buffer) (1)

ln	outs	Outputs
хŌЕ	хАх	хҮх
L	Н	Н
L	L	L
Н	Х	Z

### NOTE

1. H = HIGH Voltage Level

L = LOW Voltage Level

X = Don't Care

Z = High-Impedance

# DC ELECTRICAL CHARACTERISTICS OVER OPERATING RANGE

Following Conditions Apply Unless Otherwise Specified:

Operating Condition: TA = - 40°C To +85°C

Symbol	Parameter	7	Test Conditions	Min.	Typ. <sup>(1)</sup>	Max.	Unit
VIH	Input HIGH Voltage Level	Vcc = 2.3V to 2.7V		1.7	_	_	٧
		Vcc = 2.7V to 3.6V		2	_		
VIL	Input LOW Voltage Level	Vcc = 2.3V to 2.7V		_	_	0.7	٧
		Vcc = 2.7V to 3.6V		_	_	0.8	
lih lil	Input Leakage Current	Vcc = 3.6V	VI = 0 to 5.5V	_	_	±5	μA
lozн	High Impedance Output Current	Vcc = 3.6V	Vo = 0 to 5.5V	_	_	±10	μA
lozL	(3-State Output pins)						
loff	Input/Output Power Off Leakage	$V_{CC} = 0V$ , $V_{IN}$ or $V_{O} \le 5.5V$		_	_	±50	μA
VIK	Clamp Diode Voltage	Vcc = 2.3V, lin = -1	8mA	_	- 0.7	- 1.2	٧
VH	Input Hysteresis	Vcc = 3.3V		_	100	_	mV
ICCL ICCH	Quiescent Power Supply Current	Vcc = 3.6V	VIN = GND or Vcc	_	_	10	μA
Iccz			$3.6 \le VIN \le 5.5V^{(2)}$	_	_	10	1
Δlcc	Quiescent Power Supply Current Variation	One input at Vcc - 0.6V, other inputs at Vcc or GND		_	_	500	µA

#### NOTES

1. Typical values are at Vcc = 3.3V, +25°C ambient.

2. This applies in the disabled state only.

### **OUTPUT DRIVE CHARACTERISTICS**

Symbol	Parameter	Test Conditions <sup>(1)</sup>		Min.	Max.	Unit
Vон	Output HIGH Voltage	Vcc = 2.3V to 3.6V	IOH = - 0.1mA	Vcc - 0.2	_	V
		Vcc = 2.3V	IOH = -4mA	1.9	_	
			IOH = -6mA	1.7	_	
		Vcc = 2.7V	IOH = -4mA	2.2	_	
			I <sub>OH</sub> = -8mA	2	_	
		Vcc = 3.0V	IOH = -6mA	2.4	_	
			IOH = - 12mA	2	_	
VoL	Output LOW Voltage	Vcc = 2.3V to 3.6V	I <sub>OL</sub> = 0.1mA	_	0.2	V
		Vcc = 2.3V	IoL = 4mA	_	0.4	
			IoL = 6mA	_	0.55	
		Vcc = 2.7V	I <sub>OL</sub> = 4mA	_	0.4	
			IoL = 8mA	_	0.6	
		Vcc = 3.0V	IoL = 6mA	_	0.55	
			IOL = 12mA	_	0.8	8LVC Link

### NOTE:

1. VIH and VIL must be within the min. or max. range shown in the DC ELECTRICAL CHARACTERISTICS OVER OPERATING RANGE table for the appropriate Vcc range. TA = − 40°C to +85°C.

# OPERATING CHARACTERISTICS, $V_{CC}$ = 3.3V $\pm$ 0.3V, $T_{A}$ = 25°C

Symbol	Parameter	Test Conditions	Typical	Unit
CPD	Power dissipation capacitance per buffer/driver Outputs enabled	CL = 0, $f = 10Mhz$	46	pF
CPD	Power dissipation capacitance per buffer/driver Outputs enabled		2	pF

# **SWITCHING CHARACTERISTICS (1)**

		Vcc = 2.7V		$Vcc = 3.3V \pm 0.3V$		
Symbol	Parameter	Min.	Max.	Min.	Max.	Unit
tPLH	Propagation Delay	-	6.4	1.5	5.5	ns
tphl	xAx to xYx					
tpzh	Output Enable Time	_	8.1	1	7.1	ns
tpzl	x <del>OE</del> to xYx					
tphz	Output Disable Time	_	7.3	1.5	6.8	ns
tplz	x <del>OE</del> to xYx					
tsk(0)	Output Skew <sup>(2)</sup>	_	_	_	500	ps

### NOTES:

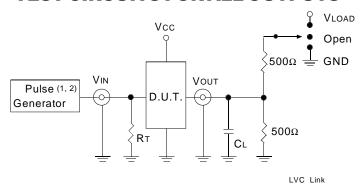
- 1. See test circuits and waveforms. TA = -40°C to + 85°C.
- 2. Skew between any two outputs of the same package and switching in the same direction.

## **TEST CIRCUITS AND WAVEFORMS**

### **TEST CONDITIONS**

Symbol	$V_{CC}^{(1)} = 3.3V \pm 0.3V$	$V_{CC}^{(1)} = 2.7V$	$V_{CC}^{(2)} = 2.5V \pm 0.2V$	Unit		
VLOAD	6	6	2 x Vcc	٧		
VIH	2.7	2.7	Vcc	٧		
VT	1.5	1.5	Vcc/2	٧		
VLZ	300	300	150	mV		
VHZ	300	300	150	mV		
CL	50	50	30	pF		
			8	LVC Link		

# **TEST CIRCUITS FOR ALL OUTPUTS**



#### **DEFINITIONS:**

CL= Load capacitance: includes jig and probe capacitance.

 $\mathsf{RT} = \mathsf{Termination}$  resistance: should be equal to  $\mathsf{ZouT}$  of the Pulse Generator.

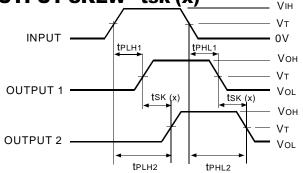
### NOTES:

- 1. Pulse Generator for All Pulses: Rate ≤ 10MHz: tF ≤ 2.5ns: tR ≤ 2.5ns.
- 2. Pulse Generator for All Pulses: Rate  $\leq$  10MHz; tF  $\leq$  2ns; tR  $\leq$  2ns.

### **SWITCH POSITION**

Test	Switch
Open Drain	Vload
Disable Low	
Enable Low	
Disable High	GND
Enable High	
All Other tests	Open

OUTPUT SKEW - tsk (x)

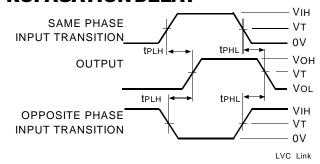


tsk(x) = |tPLH2 - tPLH1| or |tPHL2 - tPHL1|

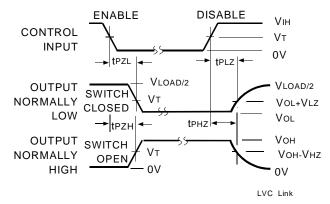
# NOTES: 1. For tsk(o) OUTPUT1 and OUTPUT2 are any two outputs.

2. For tsk(b) OUTPUT1 and OUTPUT2 are in the same bank.

# PROPAGATION DELAY



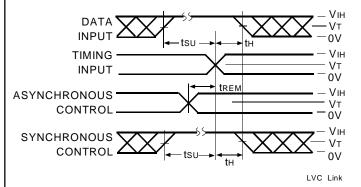
### **ENABLE AND DISABLE TIMES**



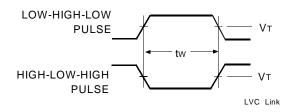
### NOTE:

 Diagram shown for input Control Enable-LOW and input Control Disable-HIGH.

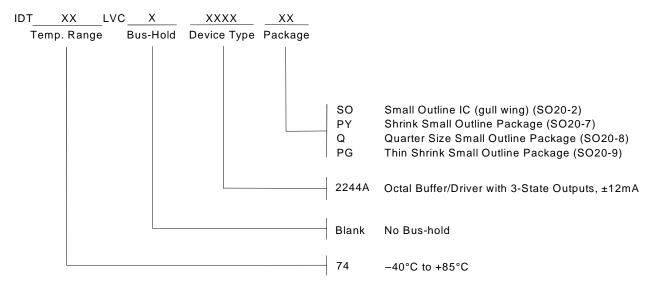
# **SET-UP, HOLD, AND RELEASE TIMES**



### **PULSE WIDTH**



### ORDERING INFORMATION





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