



3.3V CMOS SINGLE BUS BUFFER GATE WITH 3-STATE OUTPUT AND 5 VOLT TOLERANT I/O

IDT74LVC1G125A

FEATURES:

- 0.5 MICRON CMOS Technology
- ESD > 2000V per MIL-STD-883, Method 3015;
> 200V using machine model (C = 200pF, R = 0)
- 0.65mm pitch PSOP package
- Extended commercial range of – 40°C to +85°C
- $V_{CC} = 3.3V \pm 0.3V$, Normal Range
- $V_{CC} = 1.65V$ to 3.6V, Extended Range
- $V_{CC} = 2.5V \pm 0.2V$
- CMOS power levels (0.4μW typ. static)
- Rail-to-Rail output swing for increased noise margin
- All inputs, outputs and I/O are 5 Volt tolerant
- Supports hot insertion

Drive Features for LVC1G125A:

- High Output Drivers: $\pm 24mA$
- Reduced system switching noise

APPLICATIONS:

- 3.3V mixed voltage systems
- 3.3V and lower computing systems

DESCRIPTION:

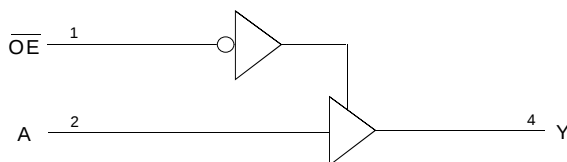
The LVC1G125A single bus buffer gate is built using advanced dual metal CMOS technology. The LVC1G125A is designed for 1.65V to 3.6V V_{CC} operation and features independent line drivers with 3-state outputs. Each output is disabled when the associated output-enable ($\overline{OE}$) input is high.

To ensure the high-impedance state during power up or power down, $\overline{OE}$ should be tied to V_{CC} through a pullup resistor; the minimum value of the resistor is determined by the current sourcing capability of the driver.

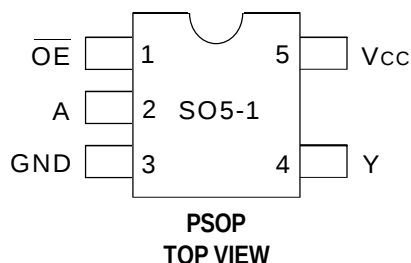
The LVC1G125A has been designed with a $\pm 24mA$ output driver. This driver is capable of driving a moderate to heavy load while maintaining speed performance.

Inputs can be driven from either 3.3V or 5V devices. This feature allows the use of this device as a translator in a mixed 3.3V/5V system environment.

FUNCTIONAL BLOCK DIAGRAM



PIN CONFIGURATION



PIN DESCRIPTION

Pin Names	Description
$\overline{OE}$	Output Enable input
A	Data Input
Y	3-State Output

FUNCTION TABLE⁽¹⁾

Inputs		Output
$\overline{OE}$	A	Y
L	H	H
L	L	L
H	X	Z

NOTE:

1. H = HIGH Voltage Level
L = LOW Voltage Level
X = Don't Care
Z = High-Impedance

ABSOLUTE MAXIMUM RATINGS ⁽¹⁾

Symbol	Description	Max.	Unit
V _{TERM}	Terminal Voltage with Respect to GND	−0.5 to +6.5	V
T _{STG}	Storage Temperature	− 65 to +150	°C
I _{OUT}	DC Output Current	− 50 to +50	mA
I _{IK} I _{OK}	Continuous Clamp Current, V _I < 0 or V _O < 0	− 50	mA
I _{CC} I _{SS}	Continuous Current through each V _{CC} or GND	±100	mA

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NOTE:

- Stresses greater than those listed under ABSOLUTE MAXIMUM RATINGS may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect reliability.

CAPACITANCE (T_A = +25°C, f = 1.0MHz)

Symbol	Parameter ⁽¹⁾	Conditions	Typ.	Max.	Unit
C _{IN}	Input Capacitance	V _{IN} = 0V	4.5	6	pF
C _{OUT}	Output Capacitance	V _{OUT} = 0V	5.5	8	pF
C _{I/O}	I/O Port Capacitance	V _{IN} = 0V	6.5	8	pF

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NOTE:

- As applicable to the device type.

DC ELECTRICAL CHARACTERISTICS OVER OPERATING RANGE

Following Conditions Apply Unless Otherwise Specified:

Operating Condition: T_A = − 40°C To +85°C

Symbol	Parameter	Test Conditions		Min.	Typ. ⁽¹⁾	Max.	Unit
V _{IH}	Input HIGH Voltage Level	V _{CC} = 1.65V to 1.95V		0.65 x V _{CC}	—	—	V
		V _{CC} = 2.3V to 2.7V		1.7	—	—	V
		V _{CC} = 2.7V to 3.6V		2	—	—	V
V _{IL}	Input LOW Voltage Level	V _{CC} = 1.65V to 1.95V		—	—	0.35 x V _{CC}	V
		V _{CC} = 2.3V to 2.7V		—	—	0.7	V
		V _{CC} = 2.7V to 3.6V		—	—	0.8	V
I _{IH} I _{IL}	Input Leakage Current	V _{CC} = 3.6V	V _I = 0 to 5.5V	—	—	±5	μA
I _{OZH} I _{OZL}	High Impedance Output Current (3-State Output pins)	V _{CC} = 3.6V	V _I = 0 to 5.5V	—	—	±10	μA
I _{OFF}	Input/Output Power Off Leakage	V _{CC} = 0V, V _{IN} or V _O ≤ 5.5V		—	—	±50	μA
V _{IK}	Clamp Diode Voltage	V _{CC} = 2.3V, I _{IN} = − 18mA		—	− 0.7	− 1.2	V
V _H	Input Hysteresis	V _{CC} = 3.3V		—	100	—	mV
I _{CC1} I _{CC2} I _{CC3}	Quiescent Power Supply Current	V _{CC} = 3.6V	V _{IN} = GND or V _{CC}	—	—	10	μA
			3.6 ≤ V _{IN} ≤ 5.5V ⁽²⁾	—	—	10	μA
ΔI _{CC}	Quiescent Power Supply Current Variation	One input at V _{CC} − 0.6V, other inputs at V _{CC} or GND		—	—	500	μA

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NOTE:

- Typical values are at V_{CC} = 3.3V, +25°C ambient.
- This applies to 3-state outputs in the disabled state only.

OUTPUT DRIVE CHARACTERISTICS

Symbol	Parameter	Test Conditions ⁽¹⁾		Min.	Max.	Unit
VOH	Output HIGH Voltage	VCC = 1.65V to 3.6V	IOH = -0.1mA	VCC - 0.2	—	V
		VCC = 1.65V	IOH = -4mA	1.2	—	
		VCC = 2.3V	IOH = -8mA	1.7	—	
		VCC = 2.7V	IOH = -12mA	2.2	—	
		VCC = 3.0V		2.4	—	
		VCC = 3.0V	IOH = -24mA	2.2	—	
VOL	Output LOW Voltage	VCC = 1.65V to 3.6V	IOL = 0.1mA	—	0.2	V
		VCC = 1.65V	IOL = 4mA	—	0.45	
		VCC = 2.3V	IOL = 8mA	—	0.7	
		VCC = 2.7V	IOL = 12mA	—	0.4	
		VCC = 3.0V	IOL = 24mA	—	0.55	

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NOTE:

1. VIH and VIL must be within the min. or max. range shown in the DC ELECTRICAL CHARACTERISTICS OVER OPERATING RANGE table for the appropriate VCC range. TA = -40°C to +85°C.

OPERATING CHARACTERISTICS, TA = 25°C

Symbol	Parameter	Test Conditions	VCC = 1.8V±0.15V	VCC = 2.5V±0.2V	VCC = 3.3V±0.3V	Unit
			Typical	Typical	Typical	
CPD	Power Dissipation Capacitance Outputs enabled	CL = 0pF, f = 10Mhz	—	—	—	pF
CPD	Power Dissipation Capacitance Outputs disabled		—	—	—	pF

SWITCHING CHARACTERISTICS ⁽¹⁾

Symbol	Parameter	VCC = 1.8V±0.15V		VCC = 2.5V±0.2V		VCC = 2.7V		VCC = 3.3V±0.3V		Unit
		Min.	Max.	Min.	Max.	Min.	Max.	Min.	Max.	
tPLH tPHL	Propagation Delay A to Y	—	12.3	1	6.3	—	5.5	1	4.8	ns
tPZH tPZL	Output Enable Time OE to Y	—	14	1	7.4	—	6.6	1	5.4	ns
tPHZ tPLZ	Output Disable Time OE to Y	—	12	1	5.6	—	5	1	4.6	ns

NOTE:

1. See test circuits and waveforms. TA = -40°C to +85°C.

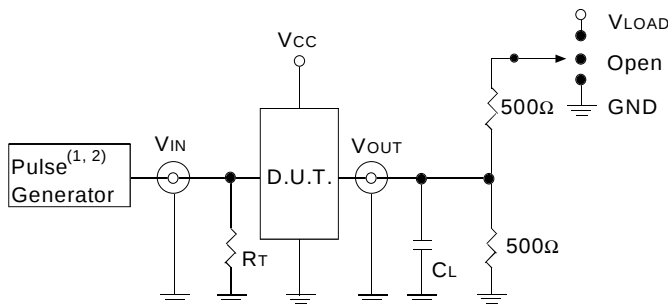
TEST CIRCUITS AND WAVEFORMS

TEST CONDITIONS

Symbol	V _{CC} (1)= 3.3V±0.3V	V _{CC} (1)= 2.7V	V _{CC} (2)= 2.5V±0.2V	Unit
V _{LOAD}	6	6	2 x V _{CC}	V
V _{IH}	2.7	2.7	V _{CC}	V
V _T	1.5	1.5	V _{CC} / 2	V
V _{LZ}	300	300	150	mV
V _{HZ}	300	300	150	mV
C _L	50	50	30	pF

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TEST CIRCUITS FOR ALL OUTPUTS



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DEFINITIONS:

C_L = Load capacitance: includes jig and probe capacitance.

R_T = Termination resistance: should be equal to Z_{OUT} of the Pulse Generator.

NOTES:

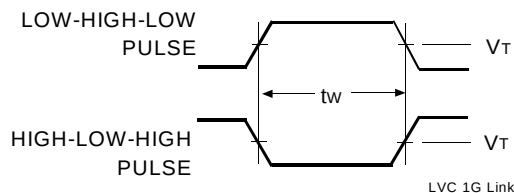
1. Pulse Generator for All Pulses: Rate ≤ 10MHz; t_r ≤ 2.5ns; t_r ≤ 2.5ns.
2. Pulse Generator for All Pulses: Rate ≤ 10MHz; t_r ≤ 2ns; t_r ≤ 2ns.

SWITCH POSITION

Test	Switch
Open Drain Disable Low Enable Low	V _{LOAD}
Disable High Enable High	GND
All Other tests	Open

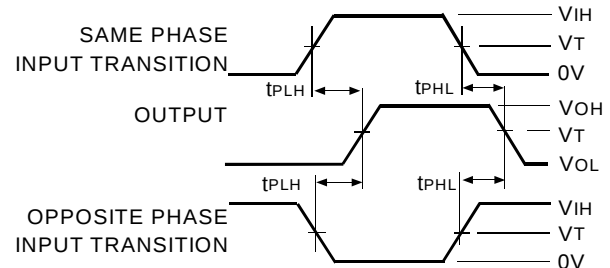
LVC 1G Link

PULSE WIDTH



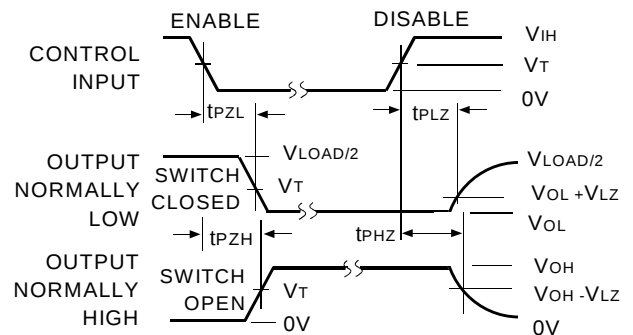
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PROPAGATION DELAY



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ENABLE AND DISABLE TIMES

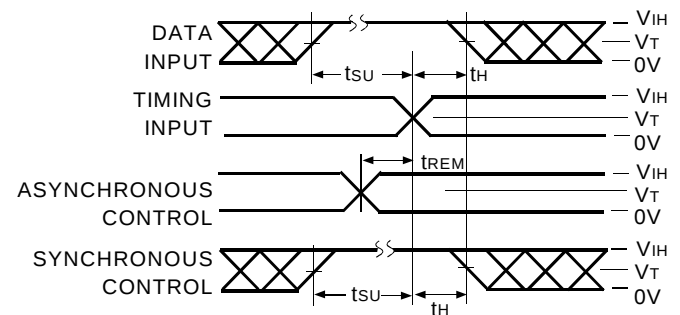


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NOTE:

1. Diagram shown for input Control Enable-LOW and input Control Disable-HIGH.

SET-UP, HOLD, AND RELEASE TIMES



LVC 1G Link

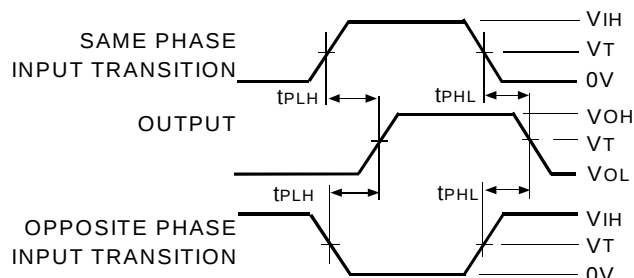
1.8V ± 0.15V TEST CIRCUITS AND WAVEFORMS

TEST CONDITIONS

Symbol	$V_{CC}^{(1)} = 1.8V \pm 0.15V$	Unit
V_{LOAD}	$2 \times V_{CC}$	V
V_{IH}	V_{CC}	V
V_T	$V_{CC} / 2$	V
V_{LZ}	150	mV
V_{HZ}	150	mV
C_L	30	pF

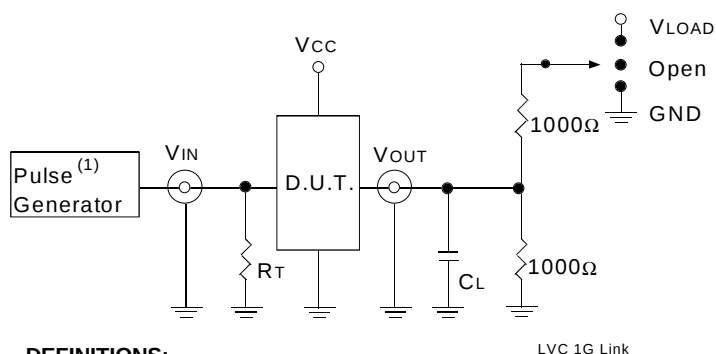
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PROPAGATION DELAY



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TEST CIRCUITS FOR ALL OUTPUTS



LVC 1G Link

DEFINITIONS:

C_L = Load capacitance: includes jig and probe capacitance.
 R_T = Termination resistance: should be equal to Z_{OUT} of the Pulse Generator.

NOTE:

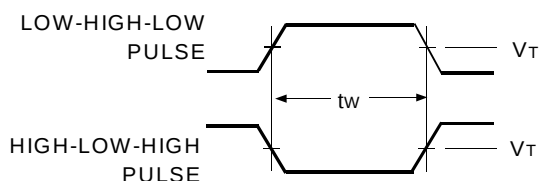
1. Pulse Generator for All Pulses: Rate $\leq 10\text{MHz}$; $t_f \leq 2\text{ns}$; $t_r \leq 2\text{ns}$.

SWITCH POSITION

Test	Switch
Open Drain Disable Low Enable Low	V_{LOAD}
Disable High Enable High	GND
All Other tests	Open

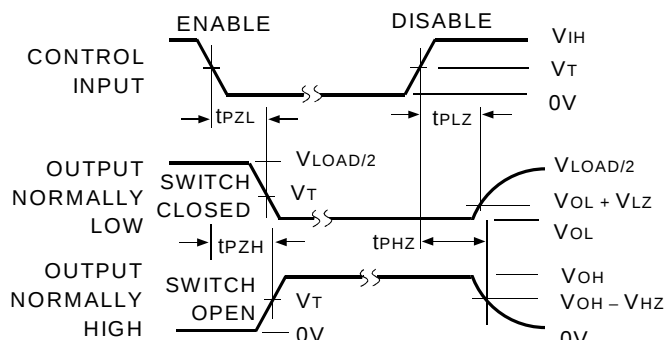
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PULSE WIDTH



LVC 1G Link

ENABLE AND DISABLE TIMES

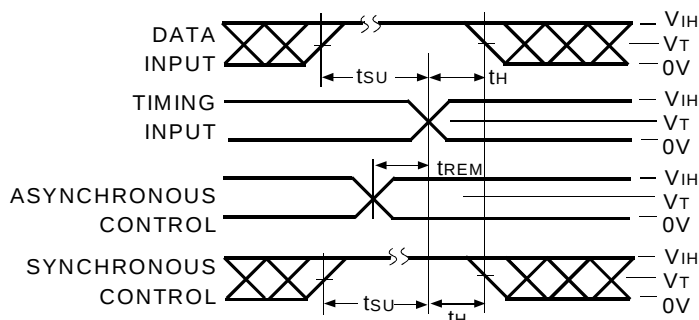


NOTE:

1. Diagram shown for input Control Enable-LOW and input Control Disable-HIGH.

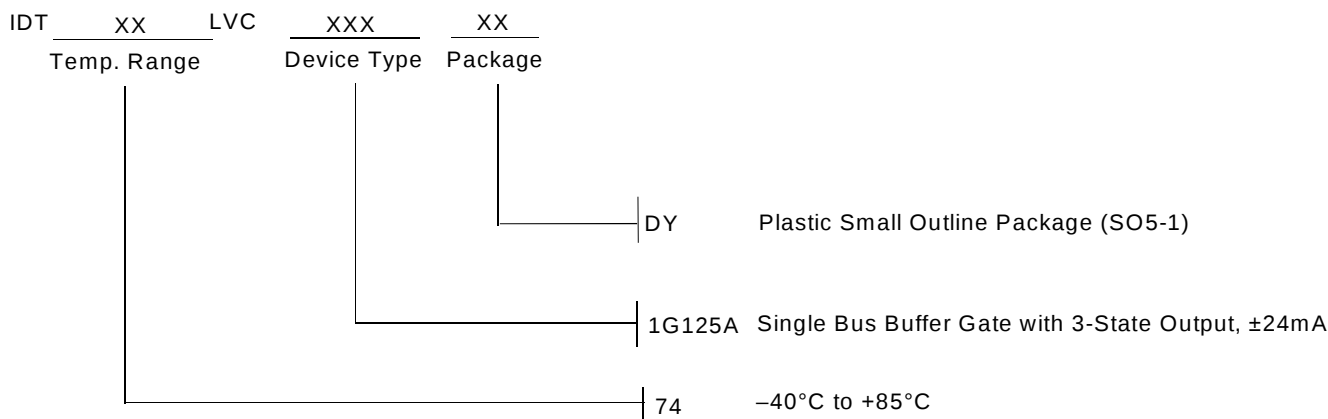
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SET-UP, HOLD, AND RELEASE TIMES



LVC 1G Link

ORDERING INFORMATION



PICOGATE-LOGIC (DY) PACKAGES

Due to their small size, PicoGate-Logic packages require more complex symbolization guidelines. IDT's 5-pin PSOP (DY) packaged devices utilize a three-symbol name rule. The first symbol denotes device technology, the second symbol denotes device function, and the third symbol denotes a wafer fab/assembly site code for internal tracking.

EXAMPLES:

1. A PicoGate-Logic device with package code LR* is an IDT74LVC1G79A.
2. A PicoGate-Logic device with package code GC* is an IDT74ALVC1G04.

PICOGATE-LOGIC (DY) PACKAGE SYMBOLIZATION GUIDELINES

TECHNOLOGY	CODE	FUNCTION	CODE
ALVC	G	00	A
ALVCH	J	02	B
LVC	L	04	C
LVCH ⁽¹⁾		U04	D
		06	T
		07	V
		08	E
		14	F
		32	G
		79	R
		86	H
		125	M
		126	N
		132	Y

NOTE:

1. Code to be determined.



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