



3.3V CMOS 16-BIT REGISTERED TRANSCEIVER WITH 3-STATE OUTPUTS, 5 VOLT TOLERANT I/O

IDT74LVC16543A

FEATURES:

- Typical $t_{SK(0)}$ (Output Skew) < 250ps
- ESD > 2000V per MIL-STD-883, Method 3015;
> 200V using machine model (C = 200pF, R = 0)
- 0.635mm pitch SSOP, 0.50mm pitch TSSOP
and 0.40mm pitch TVSOP packages
- Extended commercial range of -40°C to +85°C
- $V_{CC} = 3.3V \pm 0.3V$, Normal Range
- $V_{CC} = 2.7V$ to 3.6V, Extended Range
- CMOS power levels (0.4μW typ. static)
- All inputs, outputs and I/O are 5 Volt tolerant
- Supports hot insertion

Drive Features for LVC16543A:

- High Output Drivers: $\pm 24mA$
- Reduced system switching noise

APPLICATIONS:

- 5V and 3.3V mixed voltage systems
- Data communication and telecommunication systems

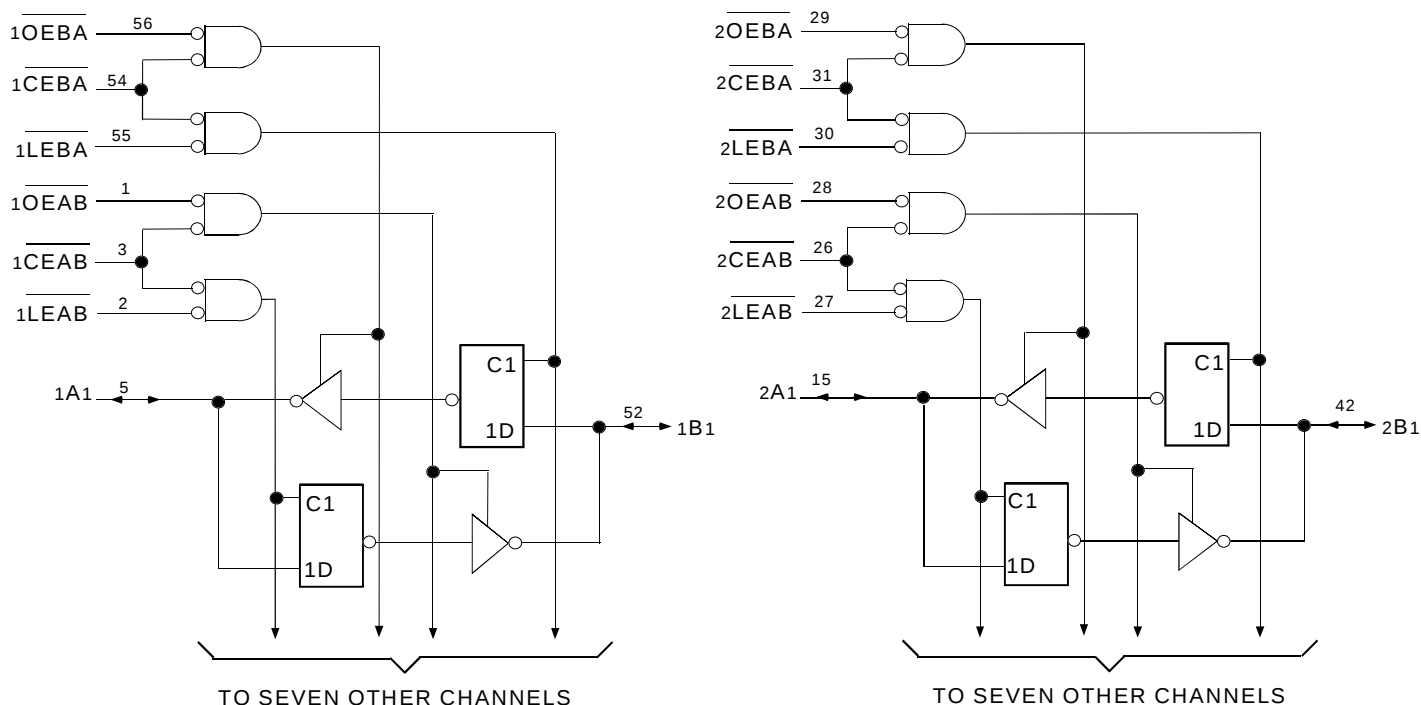
DESCRIPTION:

The LVC16543A 16-bit registered transceiver is built using advanced dual metal CMOS technology. This high-speed, low-power device can be used as two 8-bit transceivers or one 16-bit transceiver. Separate latch-enable ($\overline{LEAB}$ or $\overline{LEBA}$) and output-enable ($\overline{OEAB}$ or $\overline{OEBA}$) inputs are provided for each register to permit independent control in either direction of data flow. For example, the A-to-B enable ($\overline{CEAB}$) must be low to enter data from the A port or to output data from the B port. $\overline{LEAB}$ controls the latch function. When $\overline{LEAB}$ is low, the latches are transparent. A subsequent low-to-high transition of $\overline{LEAB}$ signal puts the A latches in the storage mode. $\overline{OEAB}$ performs the output enable function on the B port. Data flow from the B port to the A port is similar but requires using $\overline{CEBA}$, $\overline{LEBA}$, and $\overline{OEBA}$ inputs. Flow-through organization of signal pins simplifies layout. All inputs are designed with hysteresis for improved noise margin.

All pins of this 16-bit latched transceiver can be driven from either 3.3V or 5V devices. This feature allows the use of this device as a translator in a mixed 3.3V/5V supply system.

The LVC16543A has been designed with a $\pm 24mA$ output driver. This driver is capable of driving a moderate to heavy load while maintaining speed performance.

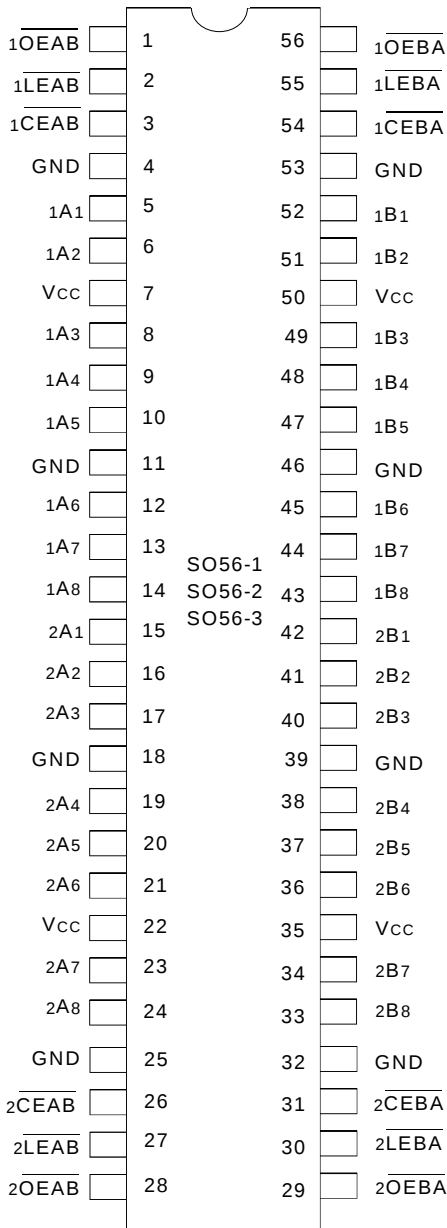
Functional Block Diagram



EXTENDED COMMERCIAL TEMPERATURE RANGE

JULY 1999

PIN CONFIGURATION



SSOP/ TSSOP/ TVSOP
TOP VIEW

CAPACITANCE (T_A = +25°C, f = 1.0MHz)

Symbol	Parameter ⁽¹⁾	Conditions	Typ.	Max.	Unit
C _{IN}	Input Capacitance	V _{IN} = 0V	4.5	6	pF
C _{OUT}	Output Capacitance	V _{OUT} = 0V	6.5	8	pF
C _{I/O}	I/O Port Capacitance	V _{IN} = 0V	6.5	8	pF

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NOTE:

- As applicable to the device type.

ABSOLUTE MAXIMUM RATINGS (1)

Symbol	Description	Max.	Unit
V _{TERM} ⁽²⁾	Terminal Voltage with Respect to GND	– 0.5 to +6.5	V
V _{TERM} ⁽³⁾	Terminal Voltage with Respect to GND	– 0.5 to +6.5	V
T _{STG}	Storage Temperature	– 65 to +150	°C
I _{OUT}	DC Output Current	– 50 to +50	mA
I _{IK} I _{OK}	Continuous Clamp Current, V _I < 0 or V _O < 0	– 50	mA
I _{CC} I _{SS}	Continuous Current through each V _{CC} or GND	±100	mA

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NOTES:

- Stresses greater than those listed under ABSOLUTE MAXIMUM RATINGS may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect reliability.
- V_{CC} terminals.
- All terminals except V_{CC}.

PIN DESCRIPTION

Pin Names	Description
xOEAB	A-to-B Output Enable Input (Active LOW)
xOEBA	B-to-A Output Enable Input (Active LOW)
xCEAB	A-to-B Enable Input (Active LOW)
xCEBA	B-to-A Enable Input (Active LOW)
xLEAB	A-to-B Latch Enable Input (Active LOW)
xLEBA	B-to-A Latch Enable Input (Active LOW)
xAx	A-to-B Data Inputs or B-to-A 3-State Outputs
xBx	B-to-A Data Inputs or A-to-B 3-State Outputs

FUNCTION TABLE (each 8-bit section) (1, 2)

Inputs				Outputs
xCEAB	xLEAB	xOEAB	xAx	xBx
H	X	X	X	Z
X	X	H	X	Z
L	H	L	X	B ₀ ⁽³⁾
L	L	L	L	L
L	L	L	H	H

NOTES:

- H = HIGH Voltage Level
L = LOW Voltage Level
X = Don't Care
Z = High-Impedance
- A-to-B data flow is shown; B-to-A flow control is the same except using CEBA, LEBA, and OEBA.
- B₀ = Output level before the indicated steady-state input conditions were established.

DC ELECTRICAL CHARACTERISTICS OVER OPERATING RANGE

Following Conditions Apply Unless Otherwise Specified:

Operating Condition: TA = -40°C to +85°C

Symbol	Parameter	Test Conditions		Min.	Typ. ⁽¹⁾	Max.	Unit
VIH	Input HIGH Voltage Level	VCC = 2.3V to 2.7V		1.7	—	—	V
		VCC = 2.7V to 3.6V		2	—	—	
VIL	Input LOW Voltage Level	VCC = 2.3V to 2.7V		—	—	0.7	V
		VCC = 2.7V to 3.6V		—	—	0.8	
IIH IIL	Input Leakage Current	VCC = 3.6V	VI = 0 to 5.5V	—	—	±5	μA
IOZH IOZL	High Impedance Output Current (3-State Output pins)	VCC = 3.6V	VO = 0 to 5.5V	—	—	±10	μA
IOFF	Input/Output Power Off Leakage	VCC = 0V, VIN or VO ≤ 5.5V		—	—	±50	μA
VIK	Clamp Diode Voltage	VCC = 2.3V, IIN = -18mA		—	-0.7	-1.2	V
VH	Input Hysteresis	VCC = 3.3V		—	100	—	mV
ICCL ICCH IC CZ	Quiescent Power Supply Current	VCC = 3.6V	VIN = GND or VCC	—	—	10	μA
			3.6 ≤ VIN ≤ 5.5V ⁽²⁾	—	—	10	
ΔICC	Quiescent Power Supply Current Variation	One input at VCC - 0.6V other inputs at VCC or GND		—	—	500	μA

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NOTES:

- Typical values are at VCC = 3.3V, +25°C ambient.
- This applies in the disabled state only.

OUTPUT DRIVE CHARACTERISTICS

Symbol	Parameter	Test Conditions ⁽¹⁾		Min.	Max.	Unit
VOH	Output HIGH Voltage	VCC = 2.3V to 3.6V	IOH = -0.1mA	VCC - 0.2	—	V
		VCC = 2.3V	IOH = -6mA	2	—	
		VCC = 2.3V	IOH = -12mA	1.7	—	
		VCC = 2.7V		2.2	—	
		VCC = 3.0V		2.4	—	
		VCC = 3.0V	IOH = -24mA	2.2	—	
VOL	Output LOW Voltage	VCC = 2.3V to 3.6V	IOL = 0.1mA	—	0.2	V
		VCC = 2.3V	IOL = 6mA	—	0.4	
			IOL = 12mA	—	0.7	
		VCC = 2.7V	IOL = 12mA	—	0.4	
		VCC = 3.0V	IOL = 24mA	—	0.55	

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NOTE:

- VIH and VIL must be within the min. or max. range shown in the DC ELECTRICAL CHARACTERISTICS OVER OPERATING RANGE table for the appropriate VCC range. TA = -40°C to +85°C.

OPERATING CHARACTERISTICS, $V_{CC} = 3.3V \pm 0.3V$, $T_A = 25^\circ C$

Symbol	Parameter	Test Conditions	Typical	Unit
C_{PD}	Power Dissipation Capacitance per transceiver Outputs enabled	$C_L = 0pF$, $f = 10MHz$	44	pF
C_{PD}	Power Dissipation Capacitance per transceiver Outputs disabled		4	pF

SWITCHING CHARACTERISTICS ⁽¹⁾

Symbol	Parameter	$V_{CC} = 2.7V$		$V_{CC} = 3.3V \pm 0.3V$		Unit
		Min.	Max.	Min.	Max.	
t_{PLH} t_{PHL}	Propagation Delay xAx to xBx or xBx to xAx	—	6.1	1.2	5.4	ns
t_{PLH} t_{PHL}	Propagation Delay xLEBA or xLEAB to xAx or xBx	—	7.4	1.5	6.1	ns
t_{PZH} t_{PZL}	Output Enable Time xCEBA or xCEAB to xAx or xBx	—	7.9	1.2	6.6	ns
t_{PZH} t_{PZL}	Output Enable Time xOEBA or xOEAB to xAx or xBx	—	7.6	1	6.3	ns
t_{PHZ} t_{PLZ}	Output Disable Time xCEBA or xCEAB to xAx or xBx	—	7.1	1.5	6.6	ns
t_{PHZ} t_{PLZ}	Output Disable Time xOEBA or xOEAB to xAx or xBx	—	6.9	1.5	6.3	ns
t_{SU}	Set-up Time, data before $\overline{CE} \uparrow$	1.1	—	1.1	—	ns
t_{SU}	Set-up Time, data before $\overline{LE} \uparrow$, $\overline{CE}$ LOW	1.1	—	1.1	—	ns
t_H	Hold Time, data after $\overline{CE} \uparrow$	1.9	—	1.9	—	ns
t_H	Hold Time, data after $\overline{LE} \uparrow$, $\overline{CE}$ LOW	1.9	—	1.9	—	ns
t_W	Pulse Duration, xLEAB or xLEBA, xCEAB or xCEBA LOW	3.3	—	3.3	—	ns
$t_{SK(0)}$	Output Skew ⁽²⁾	—	—	—	500	ps

NOTES:

- See test circuits and waveforms. $T_A = -40^\circ C$ to $+85^\circ C$.
- Skew between any two outputs of the same package and switching in the same direction.

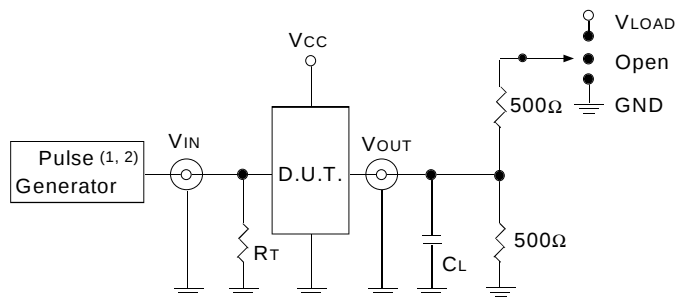
TEST CIRCUITS AND WAVEFORMS:

TEST CONDITIONS

Symbol	V _{CC} (1) = 3.3V ±0.3V	V _{CC} (1) = 2.7V	V _{CC} (2) = 2.5V ±0.2V	Unit
V _{LOAD}	6	6	2 x V _{CC}	V
V _{IH}	2.7	2.7	V _{CC}	V
V _T	1.5	1.5	V _{CC} / 2	V
V _{LZ}	300	300	150	mV
V _{HZ}	300	300	150	mV
C _L	50	50	30	pF

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TEST CIRCUITS FOR ALL OUTPUTS



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DEFINITIONS:

C_L = Load capacitance: includes jig and probe capacitance.
R_T = Termination resistance: should be equal to Z_{OUT} of the Pulse Generator.

NOTES:

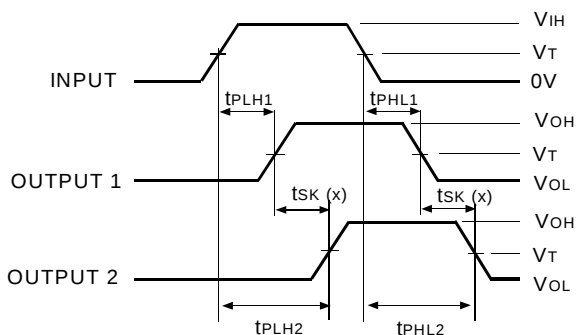
1. Pulse Generator for All Pulses: Rate ≤ 10MHz; t_r ≤ 2.5ns; t_r ≤ 2.5ns.
2. Pulse Generator for All Pulses: Rate ≤ 10MHz; t_r ≤ 2ns; t_r ≤ 2ns.

SWITCH POSITION

Test	Switch
Open Drain Disable Low Enable Low	V _{LOAD}
Disable High Enable High	GND
All Other tests	Open

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OUTPUT SKEW - t_{SK} (x)



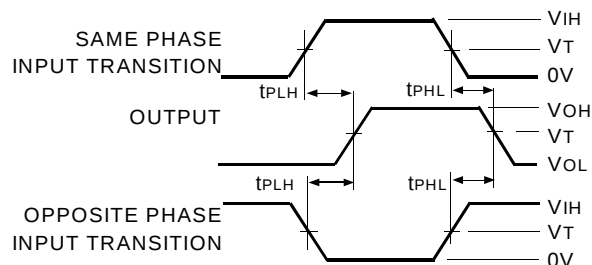
$$t_{SK}(x) = |t_{PLH2} - t_{PLH1}| \text{ or } |t_{PHL2} - t_{PHL1}|$$

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NOTES:

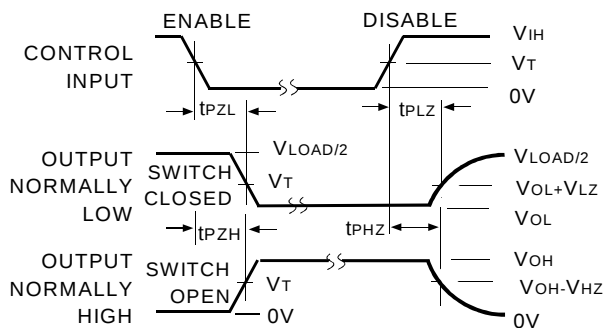
1. For t_{SK}(o) OUTPUT1 and OUTPUT2 are any two outputs.
2. For t_{SK}(b) OUTPUT1 and OUTPUT2 are in the same bank.

PROPAGATION DELAY



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ENABLE AND DISABLE TIMES

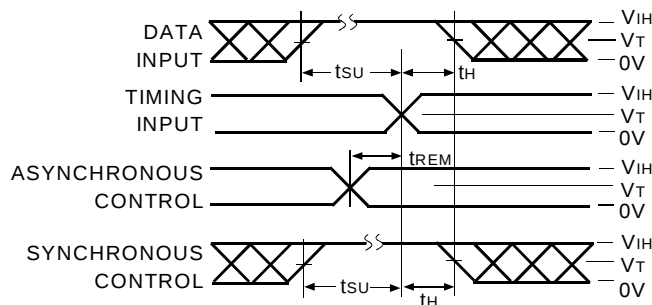


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NOTE:

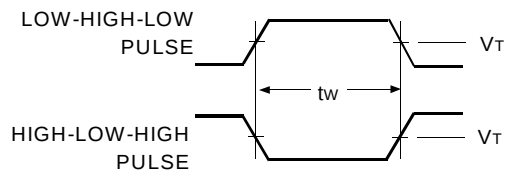
1. Diagram shown for input Control Enable-LOW and input Control Disable-HIGH.

SET-UP, HOLD, AND RELEASE TIMES



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PULSE WIDTH



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ORDERING INFORMATION

IDT	XX	LVC	X	XX	XXXX	XX	
Temp. Range	Bus-Hold	Family	Device Type	Package			
						PV	Shrink Small Outline Package (SO56-1)
						PA	Thin Shrink Small Outline Package (SO56-2)
						PF	Thin Very Small Outline Package (SO56-3)
					543A		16-Bit Registered Transceiver with 3-State Outputs, 5 Volt Tolerant I/O
					16		Double-Density with Resistors, $\pm 24\text{mA}$
					Blank		No Bus-hold
					74		-40°C to $+85^{\circ}\text{C}$



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