



HIGH PERFORMANCE CMOS BUS INTERFACE REGISTER

IDT54/74FCT823A/B/C

FEATURES:

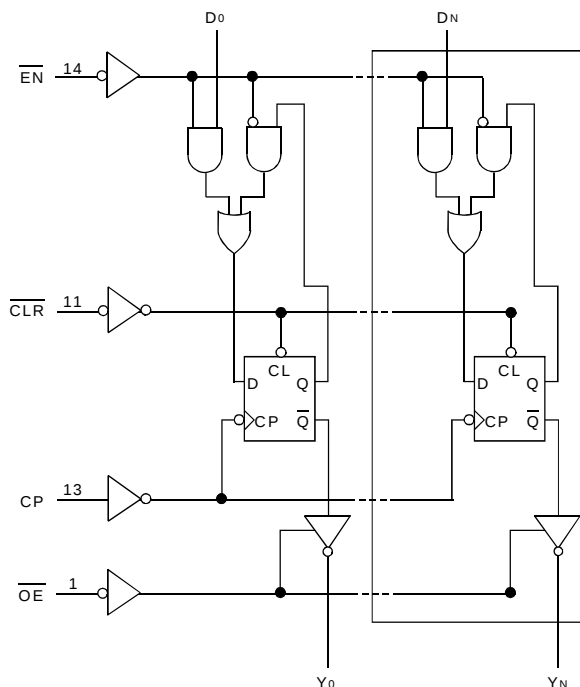
- Equivalent to AMD's Am29823 bipolar registers in pinout/function, speed and output drive over full temperature and voltage supply extremes
- IDT54/74FCT823A equivalent to FAST™ speed
- IDT54/74FCT823B 25% faster than FAST
- IDT54/74FCT823C 40% faster than FAST
- Buffered common Clock Enable ($\overline{EN}$) and asynchronous Clear input ($\overline{CLR}$)
- $I_{OL} = 48\text{mA}$ (commercial) and 32mA (military)
- Clamp diodes on all inputs for ringing suppression
- CMOS power levels (1mW typ. static)
- TTL input and output compatibility
- CMOS output level compatible
- Substantially lower input current levels than AMD's bipolar Am29800 series ($5\mu\text{A max.}$)
- Military product compliant to MIL-STD-883, Class B
- Available in the following packages:
 - Commercial: SOIC
 - Military: CERDIP, LCC, CERPACK

DESCRIPTION:

The FCT823 series is built using an advanced dual metal CMOS technology. The FCT823 bus interface registers are designed to eliminate the extra packages required to buffer existing registers and provide extra data width for wider address/data paths or buses carrying parity. The FCT823 is a 9-bit wide buffered register with Clock Enable ($\overline{EN}$) and Clear ($\overline{CLR}$) – ideal for parity bus interfacing in high-performance microprogrammed systems.

The FCT823 high-performance interface family is designed for high-capacitance load drive capability, while providing low-capacitance bus loading at both inputs and outputs. All inputs have clamp diodes and all outputs are designed for low-capacitance bus loading in high-impedance state.

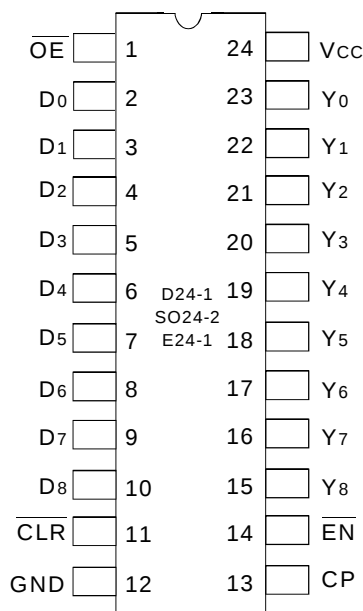
FUNCTIONAL BLOCK DIAGRAM



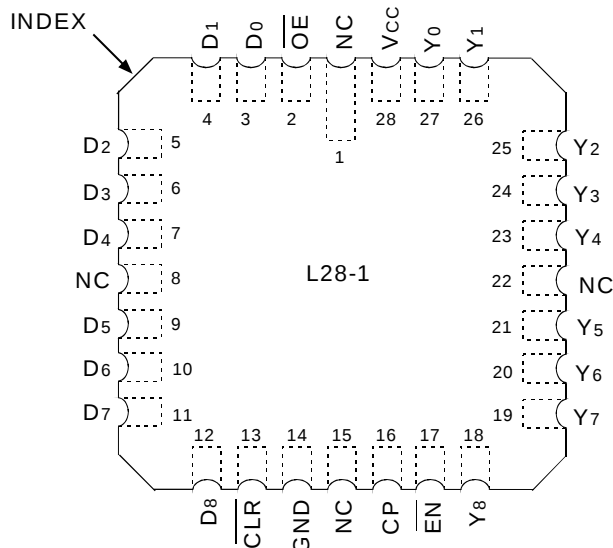
MILITARY AND COMMERCIAL TEMPERATURE RANGES

AUGUST 2001

PIN CONFIGURATION



CERDIP/ SOIC/ CERPACK
TOP VIEW



LCC
TOP VIEW

ABSOLUTE MAXIMUM RATINGS⁽¹⁾

Symbol	Rating	Commercial	Military	Unit
V _{TERM} ⁽²⁾	Terminal Voltage with Respect to GND	−0.5 to +7	−0.5 to +7	V
V _{TERM} ⁽³⁾	Terminal Voltage with Respect to GND	−0.5 to V _{CC}	−0.5 to V _{CC}	V
T _A	Operating Temperature	0 to +70	−55 to +125	°C
T _{BIAS}	Temperature Under Bias	−55 to +125	−65 to +135	°C
T _{STG}	Storage Temperature	−55 to +125	−65 to +150	°C
P _T	Power Dissipation	0.5	0.5	W
I _{OUT}	DC Output Current	120	120	mA

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NOTES:

1. Stresses greater than those listed under ABSOLUTE MAXIMUM RATINGS may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect reliability. No terminal voltage may exceed V_{CC} by +.5V unless otherwise noted.
2. Input and V_{CC} terminals only.
3. Outputs and I/O terminals only.

CAPACITANCE ($T_A = +25^{\circ}\text{C}$, $f = 1.0\text{MHz}$)

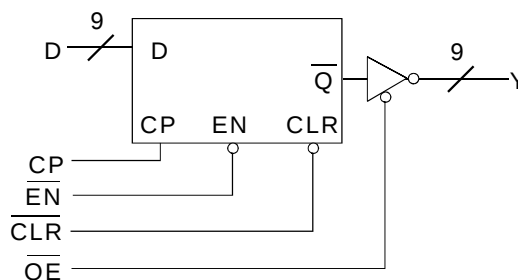
Symbol	Parameter ⁽¹⁾	Conditions	Typ.	Max.	Unit
C _{IN}	Input Capacitance	V _{IN} = 0V	6	10	pF
C _{OUT}	Output Capacitance	V _{OUT} = 0V	8	12	pF

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NOTE:

1. This parameter is measured at characterization but not tested.

LOGIC SYMBOL



PIN DESCRIPTION

Name	I/O	Description
D_I	I	The D flip-flop data inputs.
$\overline{CLR}$	I	For both inverting and non-inverting registers, when the clear input is LOW and $\overline{OE}$ is LOW, the Q_I outputs are LOW. When the clear input is HIGH, data can be entered into the register.
CP	I	Clock Pulse for the Register; enters data into the register on the LOW-to-HIGH transition.
Y_I	O	The register three-state outputs.
$\overline{EN}$	I	Clock Enable. When the clock enable is LOW, data on the D_I input is transferred to the Q_I output on the LOW-to-HIGH clock transition. When the clock enable is HIGH, the Q_I outputs do not change state, regardless of the data or clock input transitions.
$\overline{OE}$	I	Output Control. When the $\overline{OE}$ input is HIGH, the Y_I outputs are in the high impedance state. When the $\overline{OE}$ input is LOW, the TRUE register data is present at the Y_I outputs.

FUNCTION TABLE (1)

Inputs					Internal/ Outputs		Function
OE	CLR	EN	Di	CP	Qi	Yi	
H	H	L	L	↑	L	Z	High Z
H	H	L	H	↑	H	Z	
H	L	X	X	X	L	Z	Clear
L	L	X	X	X	L	L	
H	H	H	X	X	NC	Z	Hold
L	H	H	X	X	NC	NC	
H	H	L	L	↑	L	Z	Load
H	H	L	H	↑	H	Z	
L	H	L	L	↑	L	L	
L	H	L	H	↑	H	H	

NOTE:

1. H = HIGH
L = LOW
X = Don't Care
NC = No Change
↑ = LOW-to-HIGH Transition
Z = High Impedance

DC ELECTRICAL CHARACTERISTICS OVER OPERATING RANGE

Following Conditions Apply Unless Otherwise Specified: $V_{LC} = 0.2V$; $V_{HC} = V_{CC} - 0.2V$

Commercial: $T_A = 0^{\circ}C$ to $+70^{\circ}C$, $V_{CC} = 5.0V \pm 5\%$; Military: $T_A = -55^{\circ}C$ to $+125^{\circ}C$, $V_{CC} = 5.0V \pm 10\%$

Symbol	Parameter	Test Conditions ⁽¹⁾		Min.	Typ. ⁽²⁾	Max.	Unit	
V _{IH}	Input HIGH Level	Guaranteed Logic HIGH Level		2	—	—	V	
V _{IL}	Input LOW Level	Guaranteed Logic LOW Level		—	—	0.8	V	
I _{IH}	Input HIGH Current	V _{CC} = Max.	V _I = V _{CC}	—	—	5	μA	
			V _I = 2.7V	—	—	5 ⁽⁴⁾		
I _{IL}	Input LOW Current		V _I = 0.5V	—	—	−5 ⁽⁴⁾		
			V _I = GND	—	—	−5		
I _{OZH}	Off State (High Impedance) Output Current	V _{CC} = Max.	V _O = V _{CC}	—	—	10	μA	
			V _O = 2.7V	—	—	10 ⁽⁴⁾		
I _{OZL}				V _O = 0.5V	—	—		−10 ⁽⁴⁾
				V _O = GND	—	—		−10
V _{IK}	Clamp Diode Voltage	V _{CC} = Min., I _N = −18mA		—	−0.7	−1.2	V	
I _{OS}	Short Circuit Current	V _{CC} = Max. ⁽³⁾ , V _O = GND		−75	−120	—	mA	
V _{OH}	Output HIGH Voltage	V _{CC} = 3V, V _{IN} = V _{LC} or V _{HC} , I _{OH} = −32μA		V _{HC}	V _{CC}	—	V	
		V _{CC} = Min. V _{IN} = V _{IH} or V _{IL}	I _{OH} = −300μA	V _{HC}	V _{CC}	—		
			I _{OH} = −15mA MIL.	2.4	4.3	—		
			I _{OH} = −24mA COM'L.	2.4	4.3	—		
V _{OL}	Output LOW Voltage	V _{CC} = 3V, V _{IN} = V _{LC} or V _{HC} , I _{OL} = 300μA		—	GND	V _{LC}	V	
		V _{CC} = Min. V _{IN} = V _{IH} or V _{IL}	I _{OL} = 300μA	—	GND	V _{LC} ⁽⁴⁾		
			I _{OL} = 32mA MIL.	—	0.3	0.5		
			I _{OL} = 48mA COM'L.	—	0.3	0.5		

NOTES:

1. For conditions shown as max. or min., use appropriate value specified under Electrical Characteristics for the applicable device type.
2. Typical values are at $V_{CC} = 5.0V$, $+25^{\circ}C$ ambient and maximum loading.
3. Not more than one output should be shorted at one time. Duration of the short circuit test should not exceed one second.
4. This parameter is guaranteed but not tested.

POWER SUPPLY CHARACTERISTICS

 $V_{LC} = 0.2V$; $V_{HC} = V_{CC} - 0.2V$

Symbol	Parameter	Test Conditions ⁽¹⁾		Min.	Typ. ⁽²⁾	Max.	Unit
I _{CC}	Quiescent Power Supply Current	V _{CC} = Max. V _{IN} ≥ V _{HC} ; V _{IN} ≤ V _{LC}		—	0.2	1.5	mA
ΔI _{CC}	Quiescent Power Supply Current TTL Inputs HIGH	V _{CC} = Max. V _{IN} = 3.4V ⁽³⁾		—	0.5	2	mA
I _{CCD}	Dynamic Power Supply Current ⁽⁴⁾	V _{CC} = Max. Outputs Open $\overline{OE} = \overline{EN} = GND$ One Input Toggling 50% Duty Cycle	V _{IN} ≥ V _{HC} V _{IN} ≤ V _{LC}	—	0.15	0.25	mA/ MHz
I _C	Total Power Supply Current ⁽⁶⁾	V _{CC} = Max. Outputs Open f _{CP} = 10MHz 50% Duty Cycle $\overline{OE} = \overline{EN} = GND$ One Bit Toggling at f _i = 5MHz 50% Duty Cycle	V _{IN} ≥ V _{HC} V _{IN} ≤ V _{LC} (FCT)	—	1.7	4	mA
			V _{IN} = 3.4V V _{IN} = GND	—	2.2	6	
		V _{CC} = Max. Outputs Open f _{CP} = 10MHz 50% Duty Cycle $\overline{OE} = \overline{EN} = GND$ Eight Bits Toggling at f _i = 2.5MHz 50% Duty Cycle	V _{IN} ≥ V _{HC} V _{IN} ≤ V _{LC} (FCT)	—	4	7.8 ⁽⁵⁾	
			V _{IN} = 3.4V V _{IN} = GND	—	6.2	16.8 ⁽⁵⁾	

NOTES:

- For conditions shown as Max. or Min., use appropriate value specified under Electrical Characteristics for the applicable device type.
- Typical values are at V_{CC} = 5.0V, +25°C ambient.
- Per TTL driven input (V_{IN} = 3.4V); all other inputs at V_{CC} or GND.
- This parameter is not directly testable, but is derived for use in Total Power Supply calculations.
- Values for these conditions are examples of the I_{CC} formula. These limits are guaranteed but not tested.
- I_C = I_{QUIESCENT} + I_{INPUTS} + I_{DYNAMIC}
 $I_C = I_{CC} + \Delta I_{CC} D_{HNT} + I_{CCD} (f_{CP}/2 + f_i N_i)$
I_{CC} = Quiescent Current
ΔI_{CC} = Power Supply Current for a TTL High Input (V_{IN} = 3.4V)
D_H = Duty Cycle for TTL Inputs High
N_T = Number of TTL Inputs at D_H
I_{CCD} = Dynamic Current Caused by an Input Transition Pair (HLH or LHL)
f_{CP} = Clock Frequency for Register Devices (Zero for Non-Register Devices)
f_i = Input Frequency
N_i = Number of Inputs at f_i
All currents are in milliamps and all frequencies are in megahertz.

SWITCHING CHARACTERISTICS OVER OPERATING RANGE

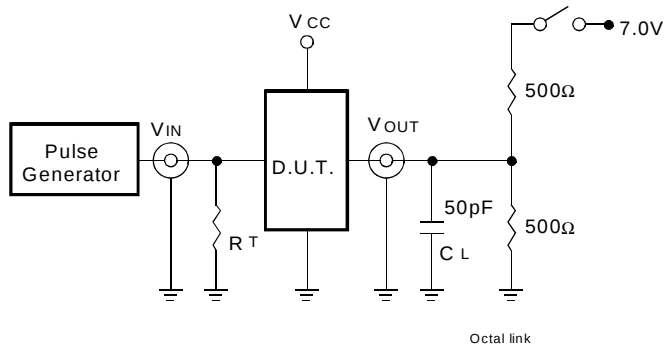
Parameter	Description	Test Conditions ⁽¹⁾	IDT54/74FCT823A				IDT54/74FCT823B				IDT54/74FCT823C				Unit
			Com'l.		Mil.		Com'l.		Mil.		Com'l.		Mil.		
			Min. ⁽²⁾	Max.	Min. ⁽²⁾	Max.	Min. ⁽²⁾	Max.	Min. ⁽²⁾	Max.	Min. ⁽²⁾	Max.	Min. ⁽²⁾	Max.	
t _{PLH} t _{PHL}	Propagation Delay CP to Y _I ($\overline{OE}$ = LOW)	CL = 50pF RL = 500Ω	—	10	—	11.5	—	7.5	—	8.5	—	6	—	7	ns
		CL = 300pF ⁽³⁾ RL = 500Ω	—	20	—	20	—	15	—	16	—	12.5	—	13.5	
t _{SU}	Set-up Time HIGH or LOW DI to CP	CL = 50pF RL = 500Ω	4	—	4	—	3	—	3	—	3	—	3	—	ns
t _H	Hold Time HIGH or LOW DI to CP		2	—	2	—	1.5	—	1.5	—	1.5	—	1.5	—	ns
t _{SU}	Set-up Time HIGH or LOW $\overline{EN}$ to CP		4	—	4	—	3	—	3	—	3	—	3	—	ns
t _H	Hold Time HIGH or LOW $\overline{EN}$ to CP		2	—	2	—	0	—	0	—	0	—	0	—	ns
t _{PHL}	Propagation Delay $\overline{CLR}$ to Y _I		—	14	—	15	—	9	—	9.5	—	8	—	8.5	ns
t _{REM}	Recovery Time $\overline{CLR}$ to CP		6	—	7	—	6	—	6	—	6	—	6	—	ns
t _W	CP Pulse Width HIGH or LOW		7	—	7	—	6	—	6	—	6	—	6	—	ns
t _W	$\overline{CLR}$ Pulse Width LOW		6	—	7	—	6	—	6	—	6	—	6	—	ns
t _{PZH} t _{PZL}	Output Enable Time $\overline{OE}$ to Y _I	CL = 50pF RL = 500Ω	—	12	—	13	—	8	—	9	—	7	—	8	ns
		CL = 300pF ⁽³⁾ RL = 500Ω	—	23	—	25	—	15	—	16	—	12.5	—	13.5	
t _{PHZ} t _{PLZ}	Output Disable Time $\overline{OE}$ to Y _I	CL = 5pF ⁽³⁾ RL = 500Ω	—	7	—	8	—	6.5	—	7	—	6.2	—	6.2	ns
		CL = 50pF RL = 500Ω	—	8	—	9	—	7.5	—	8	—	6.5	—	6.5	

NOTES:

1. See test circuit and waveforms.
2. Minimum limits are guaranteed but not tested on Propagation Delays.
3. These parameters are guaranteed but not tested.

TEST CIRCUITS AND WAVEFORMS

TEST CIRCUITS FOR ALL OUTPUTS



SWITCH POSITION

Test	Switch
Open Drain Disable Low Enable Low	Closed
All Other Tests	Open

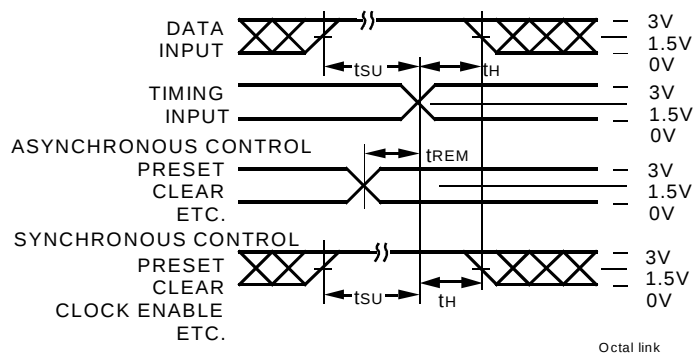
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DEFINITIONS:

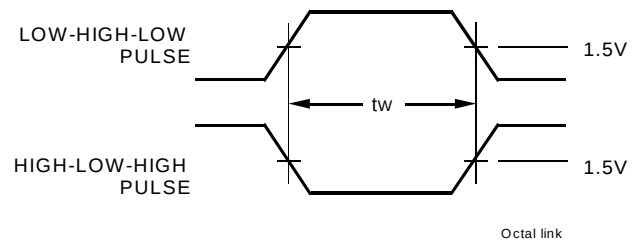
C_L = Load capacitance: includes jig and probe capacitance.

R_T = Termination resistance: should be equal to Z_{OUT} of the Pulse Generator.

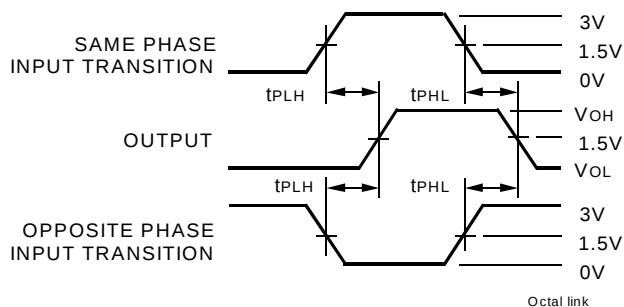
SET-UP, HOLD, AND RELEASE TIMES



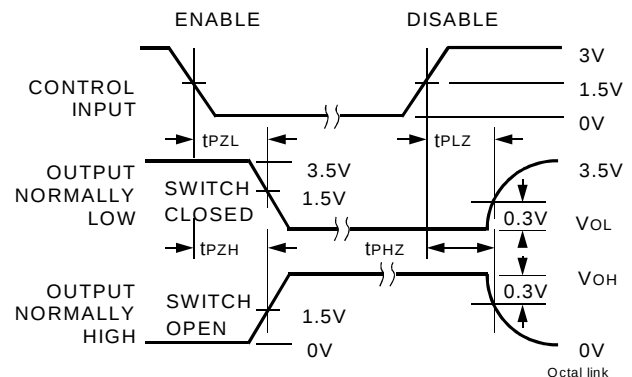
PULSE WIDTH



PROPAGATION DELAY



ENABLE AND DISABLE TIMES



NOTES:

- Diagram shown for input Control Enable-LOW and input Control Disable-HIGH.
- Pulse Generator for All Pulses: Rate $\leq 1.0\text{MHz}$; $Z_o \leq 50\Omega$; $t_f \leq 2.5\text{ns}$; $t_r \leq 2.5\text{ns}$.

ORDERING INFORMATION

IDT	XX	FCT	XXXX	XX	X		
Temp. Range	Device Type	Package	Process				
				Blank	Commercial		
				B	MIL-STD-883, Class B		
				SO	<u>Commercial Options</u>		
					Small Outline IC (SO24-2)		
				D	<u>Military Options</u>		
				E	CERDIP (D24-1)		
				L	CERPACK (E24-1)		
					Leadless Chip Carrier (L28-2)		
				823A	High Performance CMOS Bus Interface		
				823B	Register, 9-Bit		
				823C			
				54	– 55°C to +125°C		
				74	– 40°C to +85°C		



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