3.3V CMOS 20-BIT REGISTER WITH CLOCK ENABLE

IDT74FCT16V721

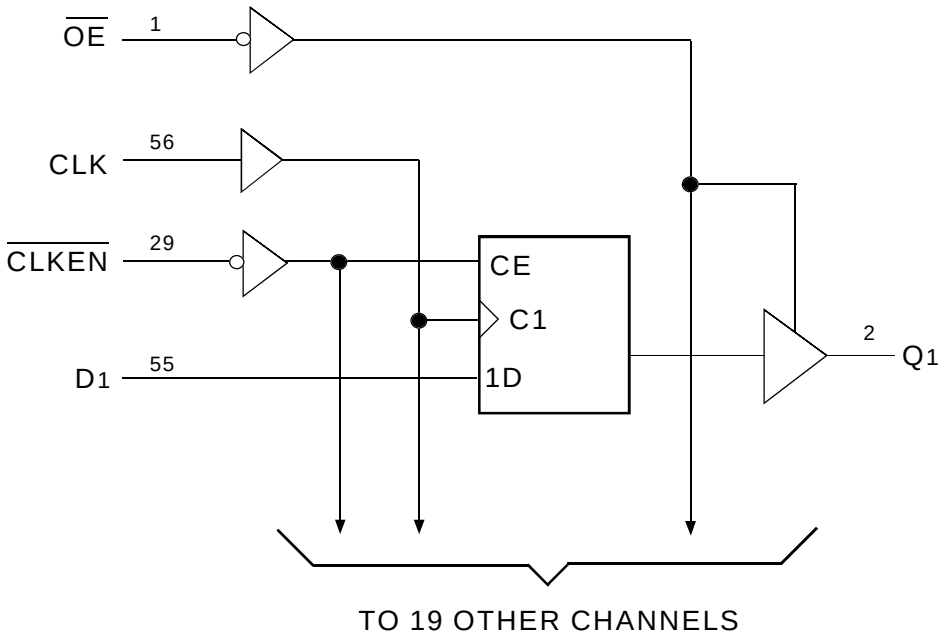
FEATURES:

- 0.5 MICRON CMOS Technology
- Typical $t_{SK(o)}$ (Output Skew) < 250ps
- ESD > 2000V per MIL-STD-883, Method 3015; > 200V using machine model (C = 200pF, R = 0)
- V_{CC} = 3.3V ±0.3V, Normal Range or
  V_{CC} = 2.7V to 3.6V, Extended Range
  V_{CC} = 2.5V ±0.2V
- CMOS power levels (0.4µW typ. static)
- Rail-to-Rail output swing for increased noise margin
- Available in SSOP and TSSOP Packages

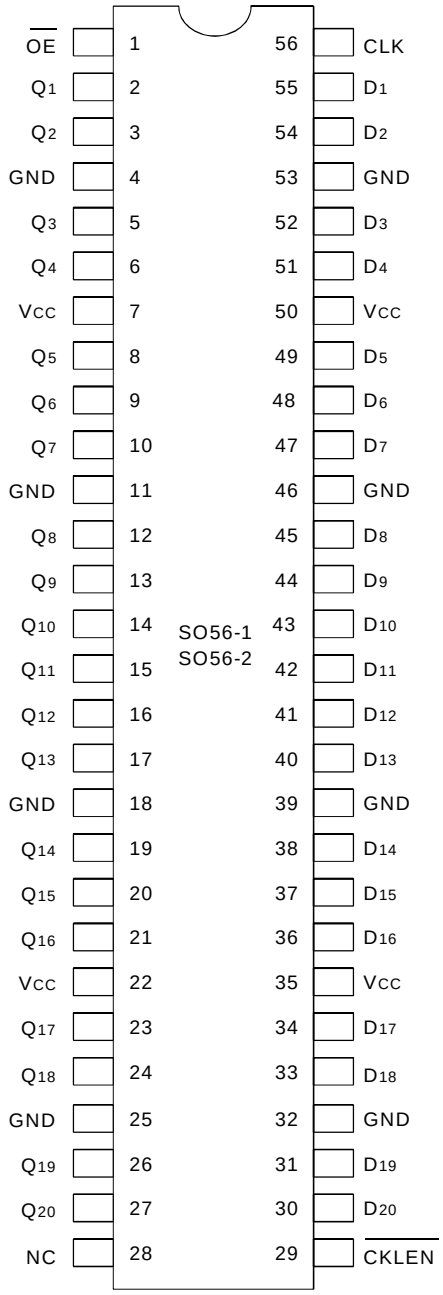
DESCRIPTION:

The FCT16V721 20-bit register is built using advanced dual metal CMOS technology. These high speed devices have been designed for use in high speed, synchronous, memory driving applications. A common clock enable allows memory bank select for memory interleaving applications. The signal skew between output pins is typically less than 250ps, giving a high level of predictability to system timing.

FUNCTIONAL BLOCK DIAGRAM



PIN CONFIGURATION



SSOP/ TSSOP
TOP VIEW

ABSOLUTE MAXIMUM RATINGS(1)

Symbol	Description	Max.	Unit
V_{TERM}(2)	Terminal Voltage with Respect to GND	–0.5 to +4.6	V
V_{TERM}(3)	Terminal Voltage with Respect to GND	–0.5 to V_{CC} +0.5	V
T_{STG}	Storage Temperature	–65 to +150	°C
I_{OUT}	DC Output Current	–60 to +60	mA

NOTES:
1. Stresses greater than those listed under ABSOLUTE MAXIMUM RATINGS may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect reliability.
2. Non-bus-hold input terminals and V_{CC} terminals.
3. Output, I/O terminals, and bus-hold input terminals.

CAPACITANCE (T_A = +25°C, f = 1.0MHz)

Symbol	Parameter(1)	Conditions	Typ.	Max.	Unit
C_{IN}	Input Capacitance	V_{IN} = 0V	3.5	6	pF
C_{OUT}	Output Capacitance	V_{OUT} = 0V	3.5	8	pF

3v16-link

NOTE:
1. This parameter is measured at characterization but not tested.

PIN DESCRIPTION

Pin Names	Description
$\overline{OE}$	3–State Output Enable Input (Active LOW)
Dx	Data Inputs
Qx	3-State Outputs
CLK	Clock Input
$\overline{CLKEN}$	Clock Enable Input

FUNCTION TABLE(1)

Inputs				Outputs
$\overline{OE}$	$\overline{CLKEN}$	CLK	Dx	Qx
L	H	X	X	Q_0
L	L	↑	H	H
L	L	↑	L	L
L	L	L	X	Q_0
H	X	X	X	Z

NOTE:
1. H = HIGH Voltage Level
   L = LOW Voltage Level
   X = Don't Care
   Z = High-Impedance
   Q_0 = Output level before the indicated steady-state conditions were established.

DC ELECTRICAL CHARACTERISTICS OVER OPERATING RANGE

Following Conditions Apply Unless Otherwise Specified:
Industrial: T_A = -40°C to +85°C

Symbol	Parameter	Test Conditions		Min.	Typ.(1)	Max.	Unit
V_{IH}	Input HIGH Voltage Level	V_{CC} = 2.3V to 2.7V		1.7	—	3.6	V
		V_{CC} = 2.7V to 3.6V		2	—	3.6	
V_{IL}	Input LOW Voltage Level	V_{CC} = 2.3V to 2.7V		–0.5	—	0.7	V
		V_{CC} = 2.7V to 3.6V		–0.5	—	0.8	
I_{IH}	Input HIGH Current	V_{CC} = 3.6V	V_I = V_{CC}	—	—	±1	µA
I_{IL}	Input LOW Current	V_{CC} = 3.6V	V_I = GND	—	—	±1	
I_{OZH}	High Impedance Output Current	V_{CC} = 3.6V	V_O = V_{CC}	—	—	±1	µA
I_{OZL}	(3-State Output pins)		V_O = GND	—	—	±1	
V_{IK}	Clamp Diode Voltage	V_{CC} = 2.3V, I_{IN} = –18mA		—	–0.7	–1.2	V
V_H	Input Hysteresis	—		—	100	—	mV
I_{CCL} I_{CCH} I_{CCZ}	Quiescent Power Supply Current	V_{CC} = 3.6V V_{IN} = GND or V_{CC}		—	0.1	10	µA

NOTE:
1. Typical values are at Vcc = 3.3V, +25°C ambient.

OUTPUT DRIVE CHARACTERISTICS

Following Conditions Apply Unless Otherwise Specified:
Industrial: T_A = -40°C to +85°C

Symbol	Parameter	Test Conditions		Min.	Max.	Unit
V_{OH}	Output HIGH Voltage	V_{CC} = 2.3V	I_{OH} = 0.1mA	V_{CC}–0.2	—	V
			I_{OH} = –6mA	2	—	
		V_{CC} = 2.3V	I_{OH} = –12mA	1.7	—	
		V_{CC} = 2.7V		2.2	—	
		V_{CC} = 3V		2.4	—	
		V_{CC} = 3V	I_{OH} = –24mA	2	—	
V_{OL}	Output LOW Voltage	V_{CC} = 2.3V	I_{OL} = 0.1mA	—	0.2	V
			I_{OL} = 6mA	—	0.4	
			I_{OL} = 12mA	—	0.7	
		V_{CC} = 2.7V	I_{OL} = 12mA	—	0.4	
		V_{CC} = 3V	I_{OL} = 24mA	—	0.55	

NOTE:
1. V_{IH} and V_{IL} must be within the min. to max. range shown in the DC ELECTRICAL CHARACTERISTICS OVER OPERATING RANGE table for the appropriate V_{CC} range.

POWER SUPPLY CHARACTERISTICS

Symbol	Parameter	Test Conditions[1]		Min.	Typ.[2]	Max.	Unit
ΔI_{CC}	Quiescent Power Supply Current	V_{CC} = Max.	V_{IN} = V_{CC} – 0.6V[3]	—	2	30	µA
I_{CCD}	Dynamic Power Supply Current[4]	V_{CC} = Max. Outputs Open $\overline{OE}$ = GND $\overline{CLKEN}$ = GND 50% Duty Cycle One Input Toggling	V_{IN} = V_{CC} V_{IN} = GND	—	60	100	µA/ MHz
I_C	Total Power Supply Current[6]	V_{CC} = Max. Outputs Open f_{CP} = 10MHz 50% Duty Cycle $\overline{OE}$ = GND $\overline{CLKEN}$ = GND fi = 5MHz 50% Duty Cycle One Bit Toggling	V_{IN} = V_{CC} V_{IN} = GND	—	0.6	1	mA
			V_{IN} = V_{CC} –0.6V V_{IN} = GND	—	0.6	1	
		V_{CC} = Max. Outputs Open f_{CP} = 10MHz 50% Duty Cycle $\overline{OE}$ = GND $\overline{CLKEN}$ = GND fi = 2.5MHz 50% Duty Cycle Twenty Bits Toggling	V_{IN} = V_{CC} V_{IN} = GND	—	3.3	5.5[5]	
			V_{IN} = V_{CC} –0.6V V_{IN} = GND	—	3.4	5.9[5]	

NOTES:
1. V_{CC} (max.) = 3.6V
2. Typical values are at V_{CC} = 3.3V, +25°C ambient.
3. Per TTL driven input; all other inputs at V_{CC} or GND.
4. This parameter is not directly testable, but is derived for use in Total Power Supply Calculations.
5. Values for these conditions are examples of the I_{CC} formula. These limits are guaranteed but not tested.
6. $I_C = I_{QUIESCENT} + I_{INPUTS} + I_{DYNAMIC}$
   $I_C = I_{CC} + \Delta I_{CC} D_H N_T + I_{CCD} (f_{CP} N_{CP}/2 + fiNi)$
   I_{CC} = Quiescent Current (I_{CCL}, I_{CCH} and I_{CCZ})
   ΔI_{CC} = Power Supply Current for a TTL High Input
   D_H = Duty Cycle for TTL Inputs High
   N_T = Number of TTL Inputs at D_H
   I_{CCD} = Dynamic Current Caused by an Input Transition Pair (HLH or LHL)
   f_{CP} = Clock Frequency for Register Devices (Zero for Non-Register Devices)
   N_{CP} = Number of Clock Inputs at f_{CP}
   f_i = Input Frequency
   N_i = Number of Inputs at fi

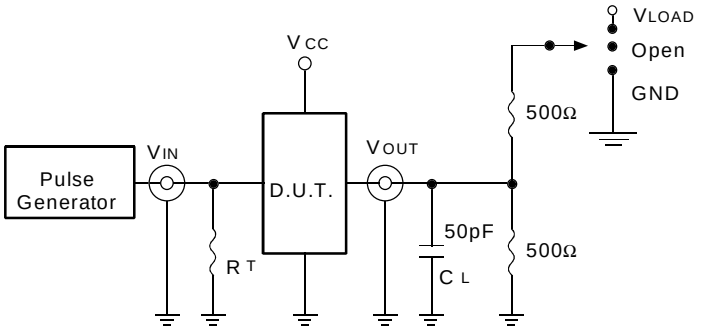
SWITCHING CHARACTERISTICS OVER OPERATING RANGE

Symbol	Parameter	Condition[1]	Vcc = 2.5V±0.2V		Vcc = 2.7V		Vcc = 3.3V±0.3V		Unit
			Min.[2]	Max.	Min.[2]	Max.	Min.[2]	Max.	
f_{MAX}	CLK Frequency	C_L = 50pF	—	150	—	150	—	150	MHz
t_{PLH} t_{PHL}	Propagation Delay CLK to Qx	R_L = 500Ω	—	7	—	5.7	1.5	4.9	ns
t_{PZH} t_{PZL}	Output Enable Time $\overline{OE}$ to Qx		—	7.4	—	6.5	1.5	5.4	ns
t_{PHZ} t_{PLZ}	Output Disable Time $\overline{OE}$ to Qx		—	6.2	—	5.1	1.5	4.8	ns
t_{SU}	Set-up Time $\overline{CLKEN}$ to CLK		3.4	—	3.1	—	2.7	—	ns
t_{SU}	Set-up Time Dx to CLK		4	—	3.6	—	3	—	ns
t_H	Hold Time Dx after CLK		0	—	0	—	0	—	ns
t_H	Hold Time $\overline{CLKEN}$ after CLK		0	—	0	—	0	—	ns
t_W	Pulse Width HIGH or LOW CLK[4]		3.3	—	3.3	—	3.3	—	ns
$t_{SK(o)}$	Output Skew[3]		—	0.5	—	0.5	—	0.5	ns

NOTES:
1. See test circuit and waveforms.
2. Minimum limits are guaranteed but not tested on Propagation Delays.
3. Skew between any two outputs, of the same package, switching in the same direction. This parameter is guaranteed by design.
4. This parameter is guaranteed but not tested.

TEST CIRCUITS AND WAVEFORMS

TEST CIRCUITS FOR ALL OUTPUTS



SWITCH POSITION

Test	Switch
Disable Low Enable Low	VLOAD
Disable High Enable High	GND
All Other tests	Open

DEFINITIONS:

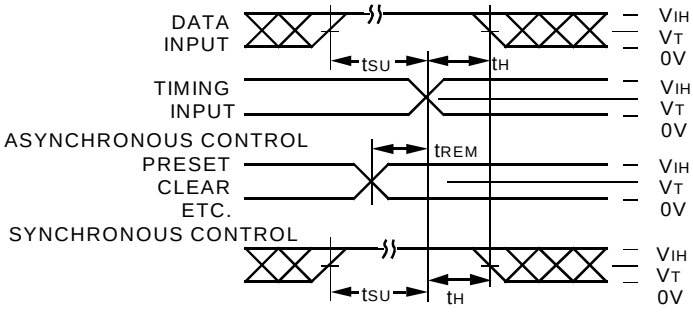
C_L = Load capacitance: includes jig and probe capacitance.

R_T = Termination resistance: should be equal to Z_{OUT} of the Pulse Generator.

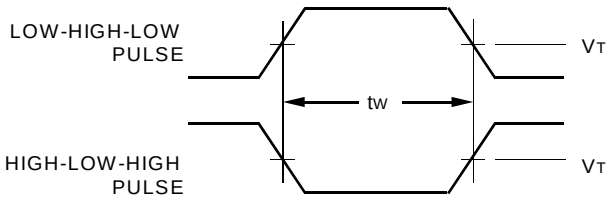
TEST VOLTAGES

Symbol	Vcc = 3.3V ±0.3V	Vcc = 2.7V	Vcc = 2.5V±0.2V	Unit
VLOAD	6	6	4.6	V
VIH	2.7	2.7	2.3	V
VT	1.5	1.5	1.2	V

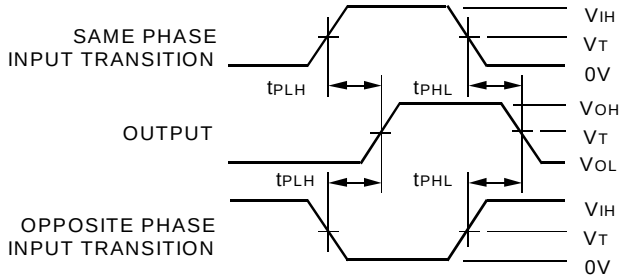
SET-UP, HOLD, AND RELEASE TIMES



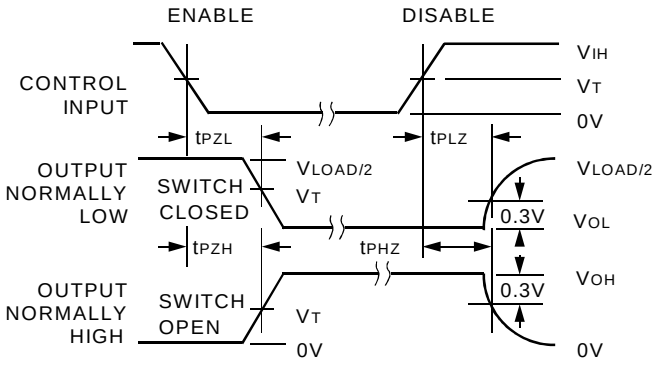
PULSE WIDTH



PROPAGATION DELAY



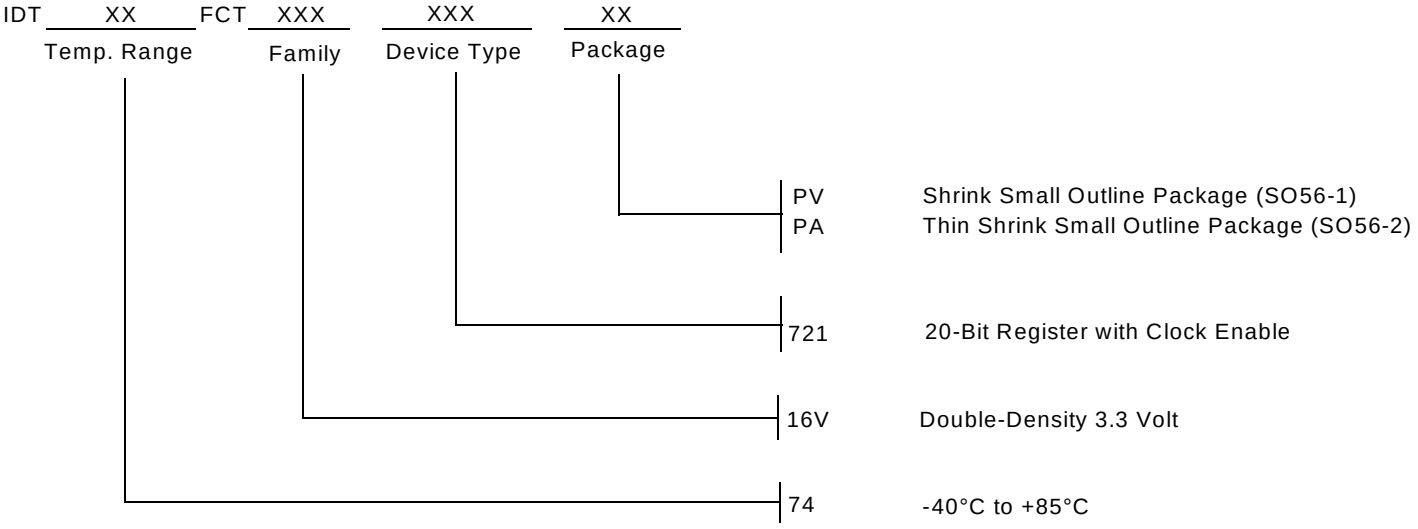
ENABLE AND DISABLE TIMES



NOTES:

1. Diagram shown for input Control Enable-LOW and input Control Disable-HIGH.
2. Pulse Generator for All Pulses: Rate ≤ 1MHz; t_F ≤ 2.5ns; t_R ≤ 2.5ns.
3. If V_{CC} is below 3V, input voltage swings should be adjusted not to exceed V_{CC}.

ORDERING INFORMATION



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