



FAST CMOS 18-BIT REGISTER

IDT54/74FCT16823AT/BT/CT/ET

FEATURES:

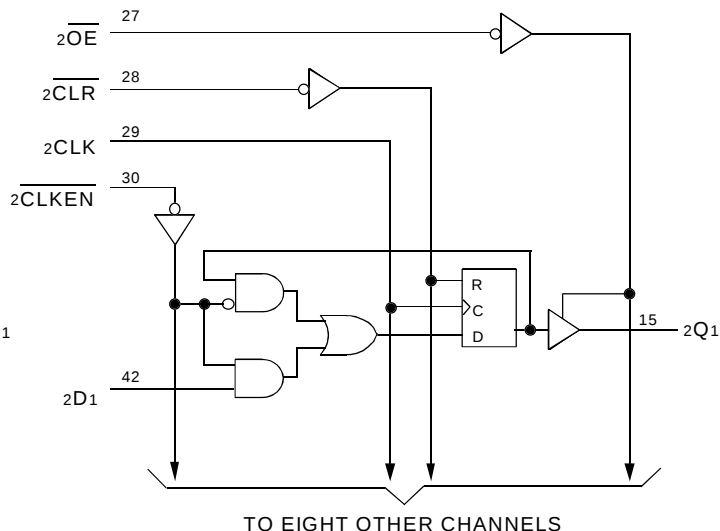
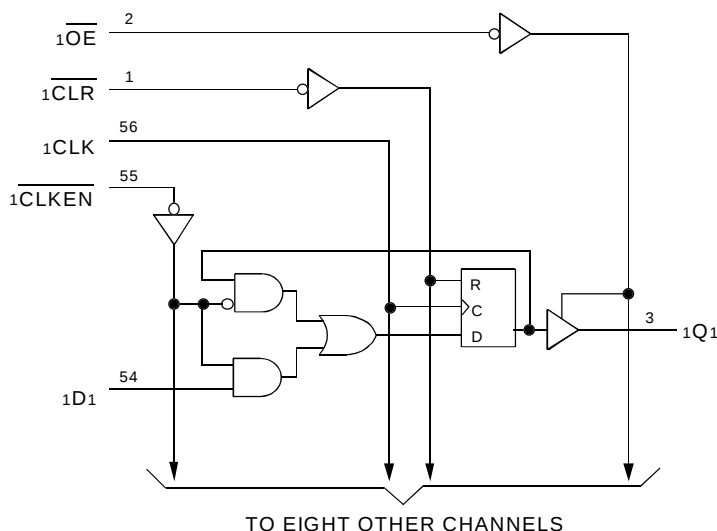
- 0.5 MICRON CMOS Technology
- High-speed, low-power CMOS replacement for ABT functions
- Typical tsk(o) (Output Skew) < 250ps
- Low input and output leakage $\leq 1\mu\text{A}$ (max.)
- ESD > 2000V per MIL-STD-883, Method 3015; > 200V using machine model (C = 200pF, R = 0)
- $V_{CC} = 5V \pm 10\%$
- High drive outputs (-32mA IOH, 64mA IOL)
- Power off disable outputs permit "live insertion"
- Typical VOLP (Output Ground Bounce) < 1.0V at $V_{CC} = 5V$, $T_A = 25^\circ\text{C}$
- Available in the following packages:
 - Industrial: SSOP, TSSOP, TVSOP
 - Military: CERPACK

DESCRIPTION:

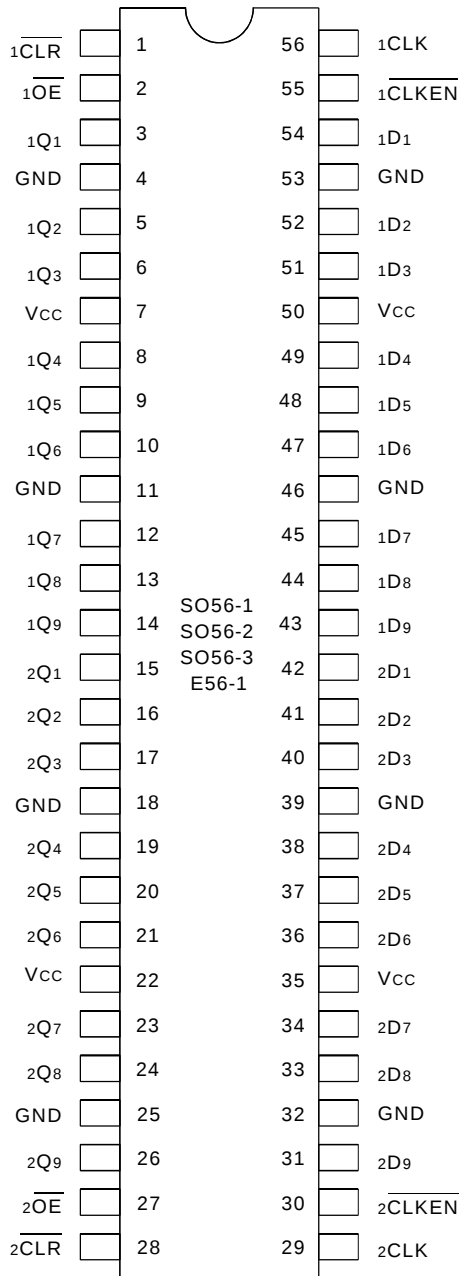
The FCT16823T 18-bit bus interface registers are built using advanced, dual metal CMOS technology. These high-speed, low-power registers with clock enable ($\overline{xCLKEN}$) and clear ($\overline{xCLR}$) controls are ideal for parity bus interfacing in high-performance synchronous systems. The control inputs are organized to operate the device as two 9-bit registers or one 18-bit register. Flow-through organization of signal pins simplifies layout. All inputs are designed with hysteresis for improved noise margin.

The FCT16823T is ideally suited for driving high-capacitance loads and low-impedance backplanes. The output buffers are designed with power off disable capability to allow "live insertion" of boards when used as backplane drivers.

FUNCTIONAL BLOCK DIAGRAM



PIN CONFIGURATION



SSOP/ TSSOP/ TVSOP/ CERPACK
TOP VIEW

ABSOLUTE MAXIMUM RATINGS(1)

Symbol	Description	Max	Unit
V _{TERM} ⁽²⁾	Terminal Voltage with Respect to GND	−0.5 to +7	V
V _{TERM} ⁽³⁾	Terminal Voltage with Respect to GND	−0.5 to V _{CC} +0.5	V
T _{STG}	Storage Temperature	−65 to +150	°C
I _{OUT}	DC Output Current	−60 to +120	mA

5v16-link

NOTES:

- Stresses greater than those listed under ABSOLUTE MAXIMUM RATINGS may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect reliability.
- All device terminals except FCT162XXX Output and I/O terminals.
- Output and I/O terminals for FCT162XXX.

CAPACITANCE (T_A = +25°C, f = 1.0MHz)

Symbol	Parameter ⁽¹⁾	Conditions	Typ.	Max.	Unit
C _{IN}	Input Capacitance	V _{IN} = 0V	3.5	6	pF
C _{OUT}	Output Capacitance	V _{OUT} = 0V	3.5	8	pF

5v16-link

NOTE:

- This parameter is measured at characterization but not tested.

PIN DESCRIPTION

Pin Names	Description
xDx	Data inputs
xCLK	Clock Inputs
x $\overline{\text{CLKEN}}$	Clock Enable Inputs (Active LOW)
x $\overline{\text{CLR}}$	Asynchronous clear Inputs (Active LOW)
x $\overline{\text{OE}}$	Output Enable Inputs (Active LOW)
xQx	3-State Outputs

FUNCTION TABLE(1)

Inputs					Outputs	Function
x $\overline{\text{OE}}$	x $\overline{\text{CLR}}$	x $\overline{\text{CLKEN}}$	xCLK	xDx	xQx	
H	X	X	X	X	Z	High Z
L	L	X	X	X	L	Clear
L	H	H	X	X	Q ⁽²⁾	Hold
H	H	L	↑	L	Z	Load
H	H	L	↑	H	Z	
L	H	L	↑	L	L	
L	H	L	↑	H	H	

NOTES:

- H = HIGH Voltage Level
L = LOW Voltage Level
X = Don't Care
Z = High-Impedance
- Output level before indicated steady-state input conditions were established.

DC ELECTRICAL CHARACTERISTICS OVER OPERATING RANGE

Following Conditions Apply Unless Otherwise Specified:

Industrial: $T_A = -40^{\circ}\text{C}$ to $+85^{\circ}\text{C}$, $V_{CC} = 5.0\text{V} \pm 10\%$; Military: $T_A = -55^{\circ}\text{C}$ to $+125^{\circ}\text{C}$, $V_{CC} = 5.0\text{V} \pm 10\%$

Symbol	Parameter	Test Conditions ⁽¹⁾		Min.	Typ. ⁽²⁾	Max.	Unit
V_{IH}	Input HIGH Level	Guaranteed Logic HIGH Level		2	—	—	V
V_{IL}	Input LOW Level	Guaranteed Logic LOW Level		—	—	0.8	V
I_{IH}	Input HIGH Current (Input pins) ⁽⁵⁾	$V_{CC} = \text{Max.}$	$V_I = V_{CC}$	—	—	± 1	μA
	Input HIGH Current (I/O pins) ⁽⁵⁾			—	—	± 1	
I_{IL}	Input LOW Current (Input pins) ⁽⁵⁾		$V_I = \text{GND}$	—	—	± 1	
	Input LOW Current (I/O pins) ⁽⁵⁾			—	—	± 1	
I_{OZH}	High Impedance Output Current	$V_{CC} = \text{Max.}$	$V_O = 2.7\text{V}$	—	—	± 1	μA
I_{OZL}	(3-State Output pins) ⁽⁵⁾		$V_O = 0.5\text{V}$	—	—	± 1	
V_{IK}	Clamp Diode Voltage	$V_{CC} = \text{Min.}, I_{IN} = -18\text{mA}$		—	-0.7	-1.2	V
I_{OS}	Short Circuit Current	$V_{CC} = \text{Max.}, V_O = \text{GND}^{(3)}$		-80	-140	-250	mA
V_H	Input Hysteresis	—		—	100	—	mV
I_{CCL} I_{CCH} I_{CCZ}	Quiescent Power Supply Current	$V_{CC} = \text{Max.}$ $V_{IN} = \text{GND or } V_{CC}$		—	5	500	μA

5v16-link

OUTPUT DRIVE CHARACTERISTICS

Symbol	Parameter	Test Conditions ⁽¹⁾		Min.	Typ. ⁽²⁾	Max.	Unit
I_O	Output Drive Current	$V_{CC} = \text{Max.}, V_O = 2.5\text{V}^{(3)}$		-50	—	-180	mA
V_{OH}	Output HIGH Voltage	$V_{CC} = \text{Min.}$ $V_{IN} = V_{IH} \text{ or } V_{IL}$	$I_{OH} = -3\text{mA}$	2.5	3.5	—	V
			$I_{OH} = -12\text{mA MIL}$	2.4	3.5	—	V
			$I_{OH} = -15\text{mA IND}$				
			$I_{OH} = -24\text{mA MIL}$ $I_{OH} = -32\text{mA IND}^{(4)}$	2	3	—	V
V_{OL}	Output LOW Voltage	$V_{CC} = \text{Min.}$ $V_{IN} = V_{IH} \text{ or } V_{IL}$	$I_{OL} = 48\text{mA MIL}$ $I_{OL} = 64\text{mA IND}$	—	0.2	0.55	V
I_{OFF}	Input/Output Power Off Leakage ⁽⁵⁾	$V_{CC} = 0\text{V}, V_{IN} \text{ or } V_O \leq 4.5\text{V}$		—	—	± 1	μA

NOTES:

- For conditions shown as Max. or Min., use appropriate value specified under Electrical Characteristics for the applicable device type.
- Typical values are at $V_{CC} = 5.0\text{V}$, $+25^{\circ}\text{C}$ ambient.
- Not more than one output should be shorted at one time. Duration of the test should not exceed one second.
- Duration of the condition can not exceed one second.
- The test limit for this parameter is $\pm 5\mu\text{A}$ at $T_A = -55^{\circ}\text{C}$.

POWER SUPPLY CHARACTERISTICS

Symbol	Parameter	Test Conditions ⁽¹⁾		Min.	Typ. ⁽²⁾	Max.	Unit
ΔI_{CC}	Quiescent Power Supply Current TTL Inputs HIGH	$V_{CC} = \text{Max.}$ $V_{IN} = 3.4V^{(3)}$		—	0.5	1.5	mA
I_{CCD}	Dynamic Power Supply Current ⁽⁴⁾	$V_{CC} = \text{Max.}$ Outputs Open $\overline{xOE} = \overline{xCLKEN} = \text{GND}$ One Input Toggling 50% Duty Cycle	$V_{IN} = V_{CC}$ $V_{IN} = \text{GND}$	—	75	120	$\mu A/\text{MHz}$
I_C	Total Power Supply Current ⁽⁶⁾	$V_{CC} = \text{Max.}$ Outputs Open $f_{CP} = 10\text{MHz}$ 50% Duty Cycle $\overline{xOE} = \overline{xCLKEN} = \text{GND}$ at $f_i = 5\text{MHz}$ 50% Duty Cycle One Bit Toggling	$V_{IN} = V_{CC}$ $V_{IN} = \text{GND}$	—	0.8	1.7	mA
			$V_{IN} = 3.4V$ $V_{IN} = \text{GND}$	—	1.3	3.2	
		$V_{CC} = \text{Max.}$ Outputs Open $f_{CP} = 10\text{MHz}$ 50% Duty Cycle $\overline{xOE} = \overline{xCLKEN} = \text{GND}$ at $f_i = 2.5\text{MHz}$ 50% Duty Cycle Eighteen Bits Toggling	$V_{IN} = V_{CC}$ $V_{IN} = \text{GND}$	—	4.2	7.1 ⁽⁵⁾	
			$V_{IN} = 3.4V$ $V_{IN} = \text{GND}$	—	9.2	22.1 ⁽⁵⁾	

NOTES:

- For conditions shown as Max. or Min., use appropriate value specified under Electrical Characteristics for the applicable device type.
- Typical values are at $V_{CC} = 5.0V$, $+25^\circ\text{C}$ ambient.
- Per TTL driven input ($V_{IN} = 3.4V$). All other inputs at V_{CC} or GND .
- This parameter is not directly testable, but is derived for use in Total Power Supply Calculations.
- Values for these conditions are examples of the I_{CC} formula. These limits are guaranteed but not tested.
- $I_C = I_{\text{QUIESCENT}} + I_{\text{INPUTS}} + I_{\text{DYNAMIC}}$
 $I_C = I_{CC} + \Delta I_{CC} D_{HNT} + I_{CCD} (f_{CP} N_{CP}/2 + f_i N_i)$
 $I_{CC} = \text{Quiescent Current } (I_{CCL}, I_{CCH} \text{ and } I_{CCZ})$
 $\Delta I_{CC} = \text{Power Supply Current for a TTL High Input } (V_{IN} = 3.4V)$
 $D_H = \text{Duty Cycle for TTL Inputs High}$
 $N_T = \text{Number of TTL Inputs at } D_H$
 $I_{CCD} = \text{Dynamic Current Caused by an Input Transition Pair (HLH or LHL)}$
 $f_{CP} = \text{Clock Frequency for Register Devices (Zero for Non-Register Devices)}$
 $N_{CP} = \text{Number of Clock Inputs at } f_{CP}$
 $f_i = \text{Input Frequency}$
 $N_i = \text{Number of Inputs at } f_i$

SWITCHING CHARACTERISTICS OVER OPERATING RANGE - INDUSTRIAL

Symbol	Parameter	Condition ⁽¹⁾	FCT16823AT		FCT16823BT		FCT16823CT		FCT16823ET		Unit
			Min. ⁽²⁾	Max.	Min. ⁽²⁾	Max.	Min. ⁽²⁾	Max.	Min. ⁽²⁾	Max.	
t _{PLH} t _{PHL}	Propagation Delay xCLK to xQx	CL = 50pF RL = 500Ω	1.5	10	1.5	7.5	1.5	6	1.5	4.4	ns
		CL = 300pF ⁽⁵⁾ RL = 500Ω	1.5	20	1.5	15	1.5	12.5	1.5	8	
t _{PHL}	Propagation Delay xCLR to xQx	CL = 50pF RL = 500Ω	1.5	14	1.5	9	1.5	6.1	1.5	4.4	ns
t _{PZH} t _{PZL}	Output Enable Time xOE to xQx	CL = 50pF RL = 500Ω	1.5	12	1.5	8	1.5	5.5	1.5	4.4	ns
		CL = 300pF ⁽⁵⁾ RL = 500Ω	1.5	23	1.5	15	1.5	12.5	1.5	9	
t _{PHZ} t _{PLZ}	Output Disable Time xOE to xQx	CL = 5pF ⁽⁵⁾ RL = 500Ω	1.5	7	1.5	6.5	1.5	5.2	1.5	3.6	ns
		CL = 50pF RL = 500Ω	1.5	8	1.5	7.5	1.5	6.5	1.5	3.6	
t _{SU}	Set-up Time HIGH or LOW xDx to xCLK	CL = 50pF RL = 500Ω	3	—	3	—	2	—	1.5	—	ns
t _H	Hold Time HIGH or LOW xDx to xCLK		1.5	—	1.5	—	1.5	—	0	—	ns
t _{SU}	Set-up Time HIGH or LOW xCLKEN to xCLK		3	—	3	—	3	—	2.5	—	ns
t _H	Hold Time HIGH or LOW xCLKEN to xCLK		0	—	0	—	0	—	0	—	ns
t _W	xCLK Pulse Width HIGH or LOW		6	—	6	—	3.3	—	3 ⁽⁴⁾	—	ns
t _W	xCLR Pulse Width LOW		6	—	6	—	3.3	—	3 ⁽⁴⁾	—	ns
t _{REM}	Recovery Time xCLR to xCLK		6	—	6	—	6	—	3	—	ns
t _{SK(o)}	Output Skew ⁽³⁾		—	0.5	—	0.5	—	0.5	—	0.5	ns

NOTES:

1. See test circuit and waveforms.
2. Minimum limits are guaranteed but not tested on Propagation Delays.
3. Skew between any two outputs of the same package switching in the same direction. This parameter is guaranteed by design.
4. This limit is guaranteed but not tested.
5. This condition is guaranteed but not tested.

SWITCHING CHARACTERISTICS OVER OPERATING RANGE-MILITARY

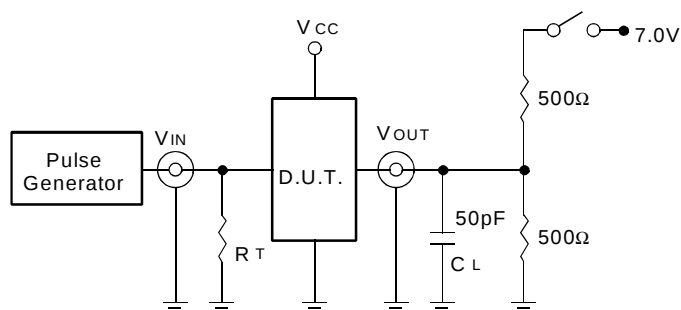
Symbol	Parameter	Condition ⁽¹⁾	FCT16823AT		FCT16823BT		FCT16823CT		Unit
			Min. ⁽²⁾	Max.	Min. ⁽²⁾	Max.	Min. ⁽²⁾	Max.	
t _{PLH} t _{PHL}	Propagation Delay xCLK to xQx	CL = 50pF RL = 500Ω	1.5	11.5	1.5	8.5	1.5	7	ns
		CL = 300pF ⁽⁵⁾ RL = 500Ω	1.5	20	1.5	16	1.5	13.5	
t _{PHL}	Propagation Delay xCLR to xQx	CL = 50pF RL = 500Ω	1.5	15	1.5	9.5	1.5	8.5	ns
t _{PZH} t _{PZL}	Output Enable Time xOE to xQx	CL = 50pF RL = 500Ω	1.5	13	1.5	9	1.5	8	ns
		CL = 300pF ⁽⁵⁾ RL = 500Ω	1.5	25	1.5	16	1.5	13.5	
t _{PHZ} t _{PLZ}	Output Disable Time xOE to xQx	CL = 5pF ⁽⁵⁾ RL = 500Ω	1.5	8	1.5	7	1.5	6.2	ns
		CL = 50pF RL = 500Ω	1.5	9	1.5	8	1.5	6.5	
t _{SU}	Set-up Time HIGH or LOW xDx to xCLK	CL = 50pF RL = 500Ω	4	—	3	—	3	—	ns
t _H	Hold Time HIGH or LOW xDx to xCLK		2	—	1.5	—	1.5	—	ns
t _{SU}	Set-up Time HIGH or LOW xCLKEN to xCLK		4	—	3	—	3	—	ns
t _H	Hold Time HIGH or LOW xCLKEN to xCLK		2	—	0	—	0	—	ns
t _W	xCLK Pulse Width HIGH or LOW		7	—	6	—	6	—	ns
t _W	xCLR Pulse Width LOW		7	—	6	—	6	—	ns
t _{REM}	Recovery Time xCLR to xCLK		7	—	6	—	6	—	ns
t _{SK(0)}	Output Skew ⁽³⁾		—	0.5	—	0.5	—	0.5	ns

NOTES:

1. See test circuit and waveforms.
2. Minimum limits are guaranteed but not tested on Propagation Delays.
3. Skew between any two outputs of the same package switching in the same direction. This parameter is guaranteed by design.
4. This limit is guaranteed but not tested.
5. This condition is guaranteed but not tested.

TEST CIRCUITS AND WAVEFORMS

TEST CIRCUITS FOR ALL OUTPUTS



SWITCH POSITION

Test	Switch
Open Drain Disable Low Enable Low	Closed
All Other Tests	Open

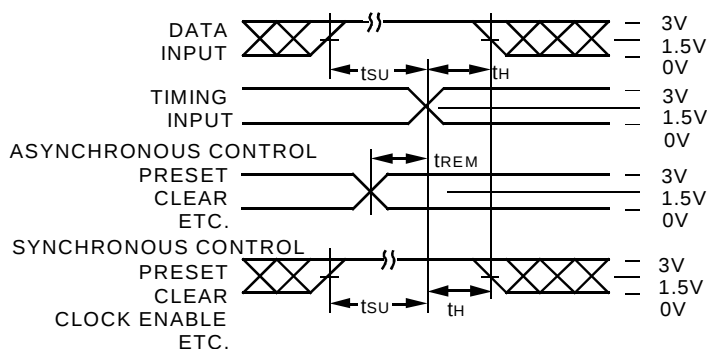
5v16-link

DEFINITIONS:

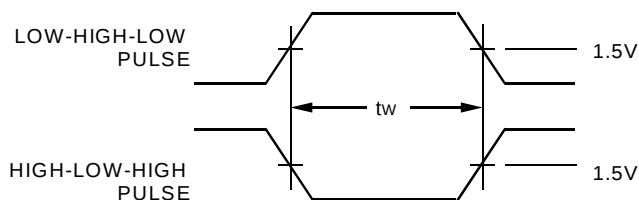
C_L = Load capacitance: includes jig and probe capacitance.

R_T = Termination resistance: should be equal to Z_{OUT} of the Pulse Generator.

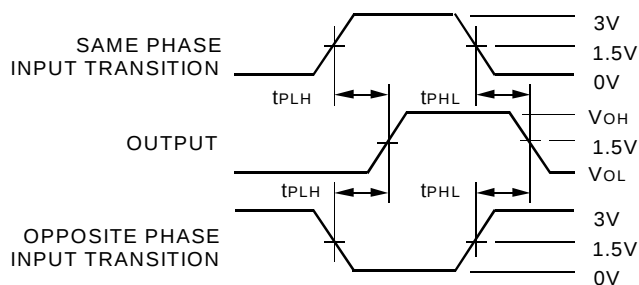
SET-UP, HOLD, AND RELEASE TIMES



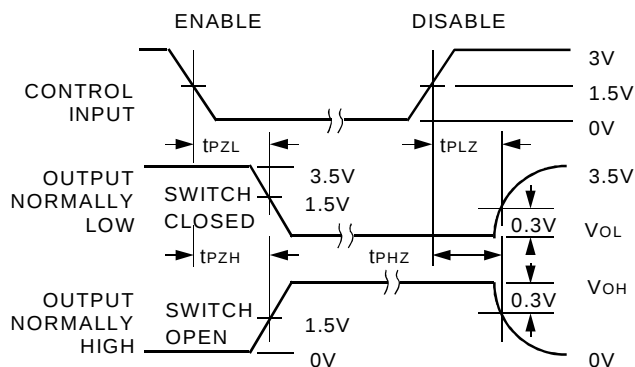
PULSE WIDTH



PROPAGATION DELAY



ENABLE AND DISABLE TIMES



NOTES:

- Diagram shown for input Control Enable-LOW and input Control Disable-HIGH.
- Pulse Generator for All Pulses: Rate $\leq 1.0\text{MHz}$; $t_F \leq 2.5\text{ns}$; $t_R \leq 2.5\text{ns}$.

ORDERING INFORMATION

IDT	XX	FCT	XXX	XXXX	XX	X		
Temp. Range	Family		Device Type	Package	Process			
						Blank	Industrial	
						B	MIL-STD-883, Class B	
							<u>Industrial Options</u>	
						PV	Shrink Small Outline Package (SO56-1)	
						PA	Thin Shrink Small Outline Package (SO56-2)	
						PF	Thin Very Small Outline Package (SO56-3)	
							<u>Military Options</u>	
						E	CERPACK (E56-1)	
						823AT	18-Bit Register	
						823BT		
						823CT		
						823ET		
						16	Double-Density, 5 Volt, High Drive	
						54	– 55°C to +125°C	
						74	– 40°C to +85°C	



CORPORATE HEADQUARTERS

2975 Stender Way
Santa Clara, CA 95054

for SALES:

800-345-7015 or 408-727-6116
fax: 408-492-8674
www.idt.com*

*To search for sales office near you, please click the sales button found on our home page or dial the 800# above and press 2.
The IDT logo is a registered trademark of Integrated Device Technology, Inc.