



3.3V CMOS 18-BIT UNIVERSAL BUS TRANSCEIVER WITH 3-STATE OUTPUTS

IDT74FCT163601/A
ADVANCE
INFORMATION

FEATURES:

- 0.5 MICRON CMOS Technology
- Typical $t_{sk(o)}$ (Output Skew) < 250ps
- ESD > 2000V per MIL-STD-883, Method 3015;
> 200V using machine model (C = 200pF, R = 0)
- $V_{cc} = 3.3V \pm 0.3V$, Normal Range or $V_{cc} = 2.7V$ to $3.6V$, Extended Range
- CMOS power levels ($0.4\mu W$ typ. static)
- Rail-to-Rail output swing for increased noise margin
- Low Ground Bounce ($0.3V$ typ.)
- Inputs (except I/O) can be driven by 3.3V or 5V components
- Available in SSOP, TSSOP and TVSOP Packages

DESCRIPTION:

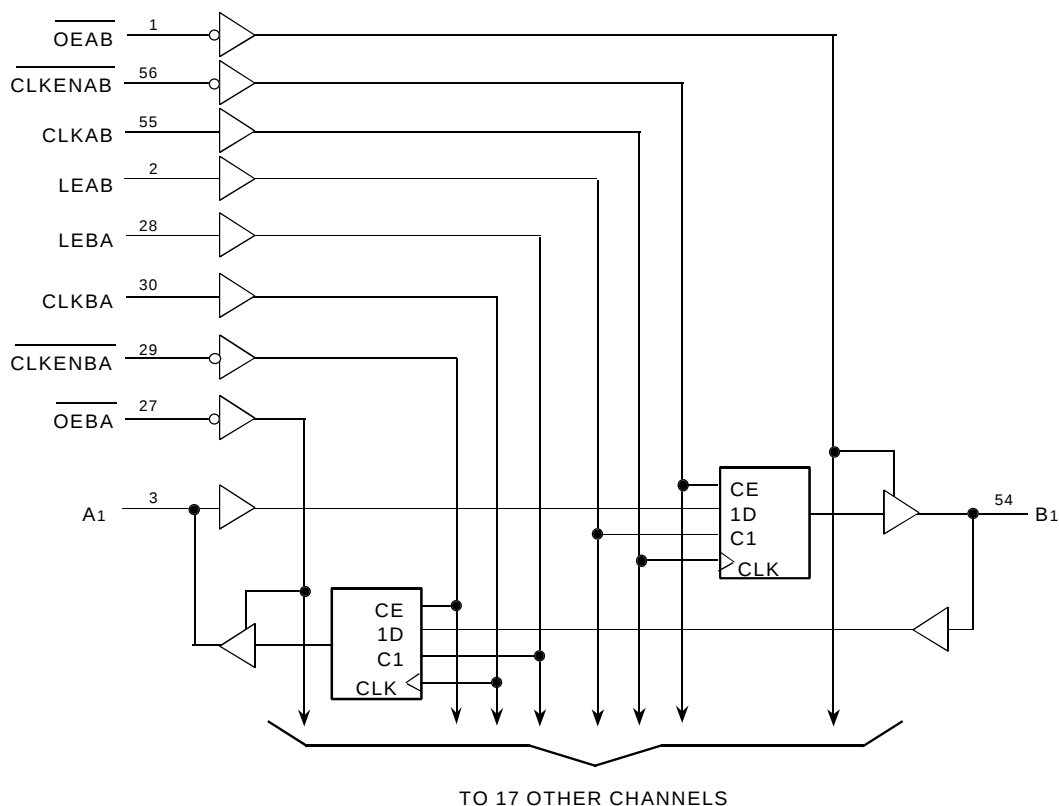
The FCT163601/A 18-bit registered transceiver is built using advanced dual metal CMOS technology. These 18-bit universal bus transceivers combine D-type latches and D-type flip-flops to allow data flow in transparent, latched and clocked modes.

Data flow in each direction is controlled by output-enable ($\overline{OEAB}$ and $\overline{OEBA}$), latch-enable (LEAB and LEBA), and clock (CLKAB and CLKBA) inputs. The clock can be controlled by the clock-enable ($\overline{CLKENAB}$ and $\overline{CLKENBA}$) inputs. For A-to-B data flow, the device operates in the transparent mode when LEAB is high. When LEAB is low, the A data is latched if CLKAB is held at a high or low logic level. If LEAB is low, the A-bus data is stored in the latch/flip-flop on the low-to-high transition of CLKAB. Output enable $\overline{OEAB}$ is active low. When $\overline{OEAB}$ is low, the outputs are active. When $\overline{OEAB}$ is high, the outputs are in the high-impedance state.

Data flow for B to A is similar to that of A to B but uses $\overline{OEBA}$, LEBA, CLKBA and $\overline{CLKENBA}$.

The FCT163601 has series current limiting resistors. These offer low ground bounce, minimal undershoot, and controlled output fall times—reducing the need for external series terminating resistors.

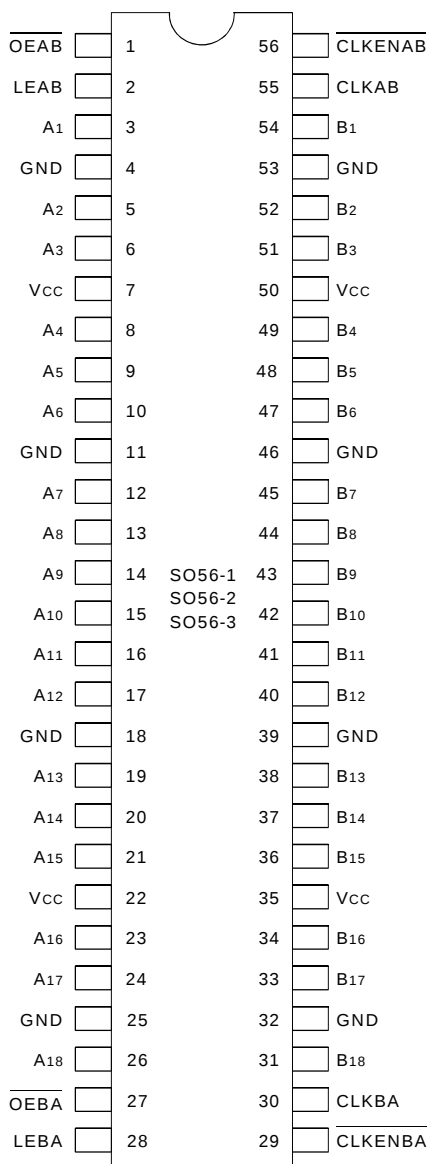
FUNCTIONAL BLOCK DIAGRAM



INDUSTRIAL TEMPERATURE RANGE

JUNE 2000

PIN CONFIGURATION



SSOPI/ TSSOP/ TVSOP
TOP VIEW

PIN DESCRIPTION

Pin Names	Description
$\overline{OEAB}$	A-to-B Output Enable Input (Active LOW)
$\overline{OEBA}$	B-to-A Output Enable Input (Active LOW)
LEAB	A-to-B Latch Enable Input
LEBA	B-to-A Latch Enable Input
CLKAB	A-to-B Clock Input
CLKBA	B-to-A Clock Input
Ax	A-to-B Data Inputs or B-to-A 3-State Outputs
Bx	B-to-A Data Inputs or A-to-B 3-State Outputs
$\overline{CLKENAB}$	A to B Clock Enable Input (Active LOW)
$\overline{CLKENBA}$	B to A Clock Enable Input (Active LOW)

ABSOLUTE MAXIMUM RATINGS⁽¹⁾

Symbol	Description	Max	Unit
$V_{TERM}^{(2)}$	Terminal Voltage with Respect to GND	-0.5 to +4.6	V
$V_{TERM}^{(3)}$	Terminal Voltage with Respect to GND	-0.5 to +7	V
$V_{TERM}^{(4)}$	Terminal Voltage with Respect to GND	-0.5 to $V_{CC}+0.5$	V
TSTG	Storage Temperature	-65 to +150	°C
IOUT	DC Output Current	-60 to +60	mA

3v16-link

NOTES:

- Stresses greater than those listed under ABSOLUTE MAXIMUM RATINGS may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect reliability.
- VCC terminals.
- Input terminals.
- Outputs and I/O terminals.

CAPACITANCE (TA = +25°C, f = 1.0MHz)

Symbol	Parameter ⁽¹⁾	Conditions	Typ.	Max.	Unit
CIN	Input Capacitance	VIN = 0V	3.5	6	pF
COUT	Output Capacitance	VOUT = 0V	3.5	8	pF

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NOTE:

- This parameter is measured at characterization but not tested.

FUNCTION TABLE^(1,4)

Inputs				Outputs	
$\overline{CLKENAB}$	$\overline{OEAB}$	LEAB	CLKAB	A	B
X	H	X	X	X	Z
X	L	H	X	L	L
X	L	H	X	H	H
H	L	L	X	X	B ₀ ⁽²⁾
L	L	L	↑	L	L
L	L	L	↑	H	H
L	L	L	L	X	B ₀ ⁽²⁾
L	L	L	H	X	B ₀ ⁽³⁾

NOTES:

- A-to-B data flow is shown. B-to-A data flow is similar but uses $\overline{OEBA}$, LEBA, CLKBA and $\overline{CLKENBA}$.
- Output level before the indicated steady-state input conditions were established.
- Output level before the indicated steady-state input conditions were established, provided that CLKAB was HIGH before LEAB went LOW.
- H = HIGH Voltage Level
L = LOW Voltage Level
X = Don't Care
Z = High-impedance
↑ = LOW-to-HIGH Transition

DC ELECTRICAL CHARACTERISTICS OVER OPERATING RANGE

Following Conditions Apply Unless Otherwise Specified:

Industrial: $T_A = -40^{\circ}\text{C}$ to $+85^{\circ}\text{C}$, $V_{CC} = 2.7\text{V}$ to 3.6V

Symbol	Parameter	Test Conditions ⁽¹⁾		Min.	Typ. ⁽²⁾	Max.	Unit
V_{IH}	Input HIGH Level (Input pins)	Guaranteed Logic HIGH Level		2	—	5.5	V
	Input HIGH Level (I/O pins)			2	—	$V_{CC}+0.5$	
V_{IL}	Input LOW Level (Input and I/O pins)	Guaranteed Logic LOW Level		-0.5	—	0.8	V
I_{IH}	Input HIGH Current (Input pins)	$V_{CC} = \text{Max.}$	$V_I = 5.5\text{V}$	—	—	± 1	μA
	Input HIGH Current (I/O pins)		$V_I = V_{CC}$	—	—	± 1	
I_{IL}	Input LOW Current (Input pins)		$V_I = \text{GND}$	—	—	± 1	
	Input LOW Current (I/O pins)		$V_I = \text{GND}$	—	—	± 1	
I_{OZH}	High Impedance Output Current	$V_{CC} = \text{Max.}$	$V_O = V_{CC}$	—	—	± 1	μA
I_{OZL}	(3-State Output pins)		$V_O = \text{GND}$	—	—	± 1	
V_{IK}	Clamp Diode Voltage	$V_{CC} = \text{Min.}, I_{IN} = -18\text{mA}$		—	-0.7	-1.2	V
I_{ODH}	Output HIGH Current	$V_{CC} = 3.3\text{V}, V_{IN} = V_{IH} \text{ or } V_{IL}, V_O = 1.5\text{V}^{(3)}$		-36	-60	-110	mA
I_{ODL}	Output LOW Current	$V_{CC} = 3.3\text{V}, V_{IN} = V_{IH} \text{ or } V_{IL}, V_O = 1.5\text{V}^{(3)}$		50	90	200	mA
V_{OH}	Output HIGH Voltage	$V_{CC} = \text{Min.}$ $V_{IN} = V_{IH} \text{ or } V_{IL}$	$I_{OH} = -0.1\text{mA}$	$V_{CC}-0.2$	—	—	V
			$I_{OH} = -3\text{mA}$	2.4	3	—	
		$V_{CC} = 3\text{V}$ $V_{IN} = V_{IH} \text{ or } V_{IL}$	$I_{OH} = -8\text{mA}$	2.4 ⁽⁵⁾	3	—	
V_{OL}	Output LOW Voltage	$V_{CC} = \text{Min.}$ $V_{IN} = V_{IH} \text{ or } V_{IL}$	$I_{OL} = 0.1\text{mA}$	—	—	0.2	V
			$I_{OL} = 16\text{mA}$	—	0.2	0.4	
			$I_{OL} = 24\text{mA}$	—	0.3	0.55	
		$V_{CC} = 3\text{V}$ $V_{IN} = V_{IH} \text{ or } V_{IL}$	$I_{OL} = 24\text{mA}$		0.3	0.5	
I_{OS}	Short Circuit Current ⁽⁴⁾	$V_{CC} = \text{Max.}, V_O = \text{GND}^{(3)}$		-60	-135	-240	mA
V_H	Input Hysteresis	—		—	150	—	mV
I_{CCL} I_{CCH} I_{CCZ}	Quiescent Power Supply Current	$V_{CC} = \text{Max.}$ $V_{IN} = \text{GND or } V_{CC}$		—	0.1	10	μA

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NOTES:

- For conditions shown as Max. or Min., use appropriate value specified under Electrical Characteristics for the applicable device type.
- Typical values are at $V_{CC} = 3.3\text{V}$, $+25^{\circ}\text{C}$ ambient.
- Not more than one output should be tested at one time. Duration of the test should not exceed one second.
- This parameter is guaranteed but not tested.
- $V_{OH} = V_{CC} - 0.6\text{V}$ at rated current.

POWER SUPPLY CHARACTERISTICS

Symbol	Parameter	Test Conditions ⁽¹⁾		Min.	Typ. ⁽²⁾	Max.	Unit
ΔI_{CC}	Quiescent Power Supply Current TTL Inputs HIGH	$V_{CC} = \text{Max.}$ $V_{IN} = V_{CC} - 0.6V^3$		—	2	30	μA
I_{CCD}	Dynamic Power Supply Current ⁽⁴⁾	$V_{CC} = \text{Max.}$, Outputs Open $\overline{OEAB} = V_{CC}$ $\overline{OEBA} = \text{GND}$ One Input Toggling 50% Duty Cycle	$V_{IN} = V_{CC}$ $V_{IN} = \text{GND}$	—	60	100	$\mu A / \text{MHz}$
I_C	Total Power Supply Current ⁽⁶⁾	$V_{CC} = \text{Max.}$, Outputs Open $f_{CP} = 10\text{MHz}$ (CLKBA) 50% Duty Cycle $\overline{OEAB} = V_{CC}$ $\overline{OEBA} = \text{GND}$ $\overline{LEBA} = \text{GND}$ $\overline{CLKENBA} = \text{GND}$ One Bit Toggling $f_i = 5\text{MHz}$ 50% Duty Cycle	$V_{IN} = V_{CC}$ $V_{IN} = \text{GND}$	—	0.6	1	mA
			$V_{IN} = V_{CC} - 0.6$ $V_{IN} = \text{GND}$	—	0.6	1	
		$V_{CC} = \text{Max.}$, Outputs Open $f_{CP} = 10\text{MHz}$ (CLKBA) 50% Duty Cycle $\overline{OEAB} = V_{CC}$ $\overline{OEBA} = \text{GND}$ $\overline{LEBA} = \text{GND}$ $\overline{CLKENBA} = \text{GND}$ Eighteen Bits Toggling $f_i = 2.5\text{MHz}$ 50% Duty Cycle	$V_{IN} = V_{CC}$ $V_{IN} = \text{GND}$	—	3	5 ⁽⁵⁾	
			$V_{IN} = V_{CC} - 0.6$ $V_{IN} = \text{GND}$	—	3	5.3 ⁽⁵⁾	

NOTES:

- For conditions shown as max. or min., use appropriate value specified under Electrical Characteristics for the applicable device type.
- Typical values are at $V_{CC} = 3.3V$, $+25^\circ C$ ambient.
- Per TTL driven input; all other inputs at V_{CC} or GND .
- This parameter is not directly testable, but is derived for use in Total Power Supply Calculations.
- Values for these conditions are examples of the I_{CC} formula. These limits are guaranteed but not tested.
- $I_C = I_{\text{QUIESCENT}} + I_{\text{INPUTS}} + I_{\text{DYNAMIC}}$
 $I_C = I_{CC} + \Delta I_{CC} D_{HNT} + I_{CCD} (f_{CP} N_{CP} / 2 + f_i N_i)$
 $I_{CC} = \text{Quiescent Current (} I_{CCL}, I_{CCH} \text{ and } I_{CCZ} \text{)}$
 $\Delta I_{CC} = \text{Power Supply Current for a TTL High Input}$
 $D_H = \text{Duty Cycle for TTL Inputs High}$
 $N_T = \text{Number of TTL Inputs at } D_H$
 $I_{CCD} = \text{Dynamic Current Caused by an Input Transition Pair (HLH or LHL)}$
 $f_{CP} = \text{Clock Frequency for Register Devices (Zero for Non-Register Devices)}$
 $N_{CP} = \text{Number of Clock Inputs at } f_{CP}$
 $f_i = \text{Input Frequency}$
 $N_i = \text{Number of Inputs at } f_i$

SWITCHING CHARACTERISTICS OVER OPERATING RANGE

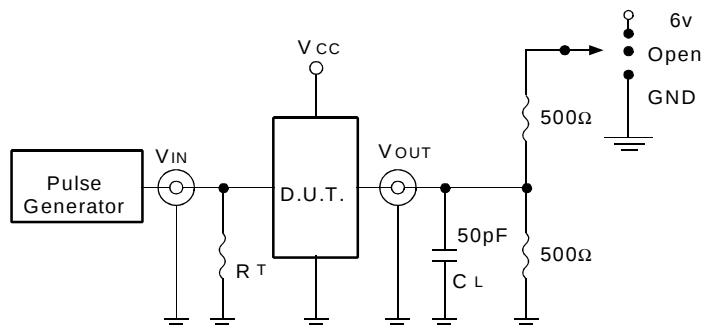
Symbol	Parameter		Condition ⁽¹⁾	FCT163601		FCT163601A		Unit
				Min. ⁽²⁾	Max.	Min. ⁽²⁾	Max.	
f _{MAX}	CLKAB or CLKBA frequency ⁽⁴⁾		CL = 50pF RL = 500Ω	—	100	—	150	MHz
t _{PLH} t _{PHL}	Propagation Delay Ax to Bx or Bx to Ax			1.5	6.5	1.5	5.5	ns
t _{PLH} t _{PHL}	Propagation Delay LEBA to Ax, LEAB to Bx			1.5	7.2	1.5	6.2	ns
t _{PLH} t _{PHL}	Propagation Delay CLKBA to Ax, CLKAB to Bx			1.5	7.3	1.5	6.3	ns
t _{PZH} t _{PZL}	Output Enable Time $\overline{OEBA}$ to Ax, $\overline{OEAB}$ to Bx			1.5	7.5	1.5	6.5	ns
t _{PHZ} t _{PLZ}	Output Disable Time $\overline{OEBA}$ to Ax, $\overline{OEAB}$ to Bx			1.5	6.5	1.5	5.2	ns
t _{SU}	Set-up Time, HIGH or LOW Ax to CLKAB, Bx to CLKBA			4	—	3	—	ns
t _H	Hold Time, HIGH or LOW Ax to CLKAB, Bx to CLKBA			0	—	0	—	ns
t _{SU}	Set-up Time HIGH or LOW Ax to LEAB, Bx to LEBA	Clock LOW		2.5	—	2.5	—	ns
		Clock HIGH		2	—	2	—	ns
t _{SU}	Set-up Time, $\overline{CLKEN}$ to CLK			3	—	2.5	—	ns
t _H	Hold Time HIGH or LOW Ax to LEAB, Bx to LEBA			1.5	—	1	—	ns
t _H	Hold Time, $\overline{CLKEN}$ after CLK			0	—	0	—	ns
t _w	LEAB or LEBA Pulse Width HIGH ⁽⁵⁾			3	—	2.5	—	ns
t _w	CLKAB or CLKBA Pulse Width HIGH or LOW ⁽⁵⁾			3	—	3	—	ns
t _{sk(0)}	Output Skew ⁽³⁾			—	0.5	—	0.5	ns

NOTES:

1. See test circuit and waveforms.
2. Minimum limits are guaranteed but not tested on Propagation Delays.
3. Skew between any two outputs of the same package switching in the same direction. This parameter is guaranteed by design.
4. This parameter is guaranteed but not tested.

TEST CIRCUITS AND WAVEFORMS

TEST CIRCUITS FOR ALL OUTPUTS



SWITCH POSITION

Test	Switch
Open Drain Disable Low Enable Low	6V
Disable High Enable High	GND
All Other Tests	Open

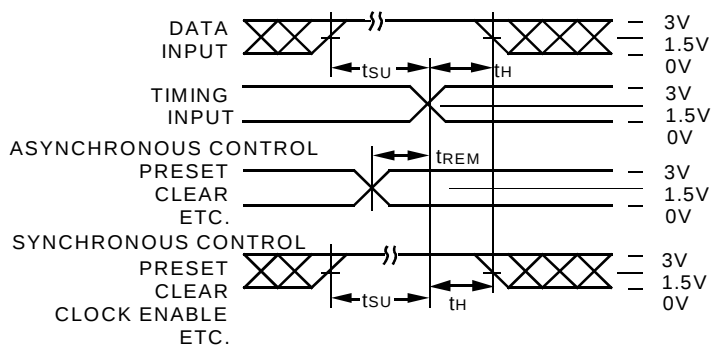
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DEFINITIONS:

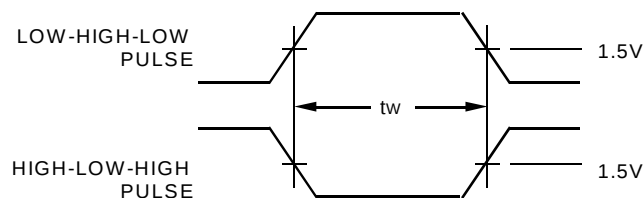
C_L = Load capacitance: includes jig and probe capacitance.

R_T = Termination resistance: should be equal to Z_{OUT} of the Pulse Generator.

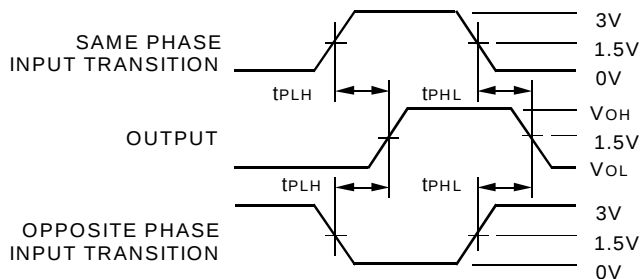
SET-UP, HOLD, AND RELEASE TIMES



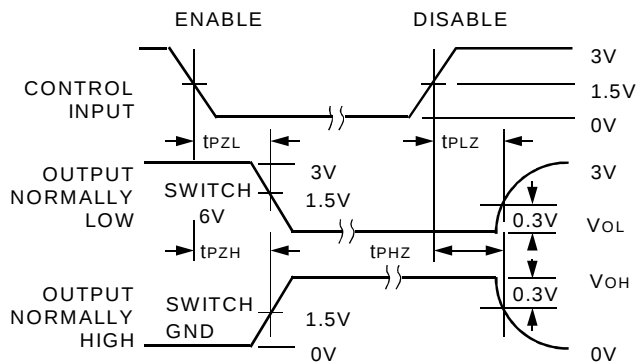
PULSE WIDTH



PROPAGATION DELAY



ENABLE AND DISABLE TIMES



NOTES:

- Diagram shown for input Control Enable-LOW and input Control Disable-HIGH.
- Pulse Generator for All Pulses: Rate $\leq 1.0\text{MHz}$; $t_F \leq 2.5\text{ns}$; $t_R \leq 2.5\text{ns}$.
- If V_{CC} is below 3V, input voltage swings should be adjusted not to exceed V_{CC} .

ORDERING INFORMATION

IDT	XX	FCT	XXX	XXXX	X		
Temp. Range	Family		Device Type	Package			
					PV		Shrink Small Outline Package (SO56-1)
					PA		Thin Shrink Small Outline Package (SO56-2)
					PF		Thin Very Small Outline Package (SO56-3)
					601		Non-Inverting 18-Bit Registered Transceiver
					601A		
					163		Double-Density 3.3Volt
					74		- 40°C to +85°C



CORPORATE HEADQUARTERS
 2975 Stender Way
 Santa Clara, CA 95054

for SALES:
 800-345-7015 or 408-727-6116
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