



FAST CMOS 16-BIT BUS TRANSCEIVER/ REGISTER

IDT54/74FCT162652AT/CT

FEATURES:

- 0.5 MICRON CMOS Technology
- High-speed, low-power CMOS replacement for ABT functions
- Typical $t_{sk(o)}$ (Output Skew) < 250ps
- Low input and output leakage $\leq 1\mu A$ (max.)
- ESD > 2000V per MIL-STD-883, Method 3015; > 200V using machine model (C = 200pF, R = 0)
- $V_{CC} = 5V \pm 10\%$
- **Balanced Output Drivers:**
 - $\pm 24mA$ (industrial)
 - $\pm 16mA$ (military)
- Reduced system switching noise
- Typical V_{OLP} (Output Ground Bounce) < 0.6V at $V_{CC} = 5V$, $T_A = 25^\circ C$
- Available in the following packages:
 - Industrial: SSOP, TSSOP
 - Military: CERPACK

DESCRIPTION:

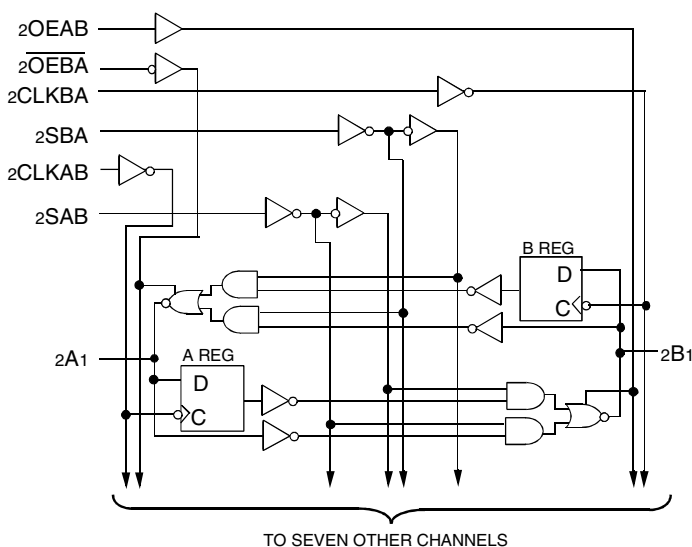
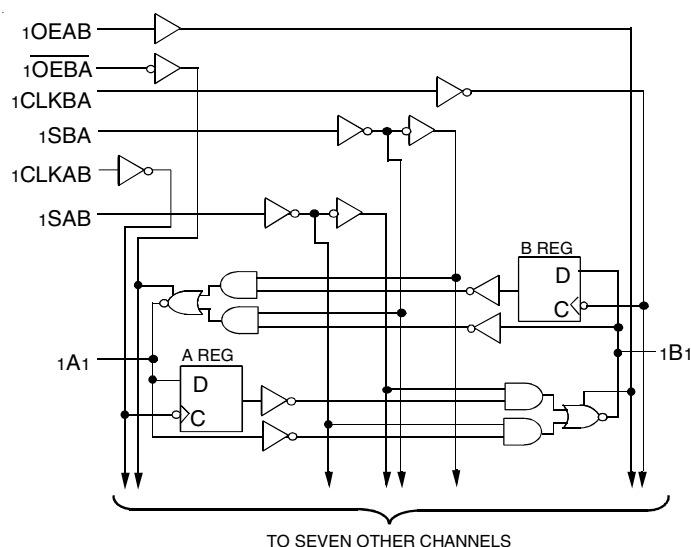
The FCT162652T 16-bit registered transceivers are built using advanced dual metal CMOS technology. These high-speed, low-power devices are organized as two independent 8-bit bus transceivers with 3-state D-type registers. For example, the $xOEAB$ and $x\overline{OEBA}$ signals control the transceiver functions.

The $xSAB$ and $xSBA$ control pins are provided to select either real time or stored data transfer. The circuitry used for select control will eliminate the typical decoding glitch that occurs in a multiplexer during the transition between stored and real time data. A low input level selects real-time data and a high level selects stored data.

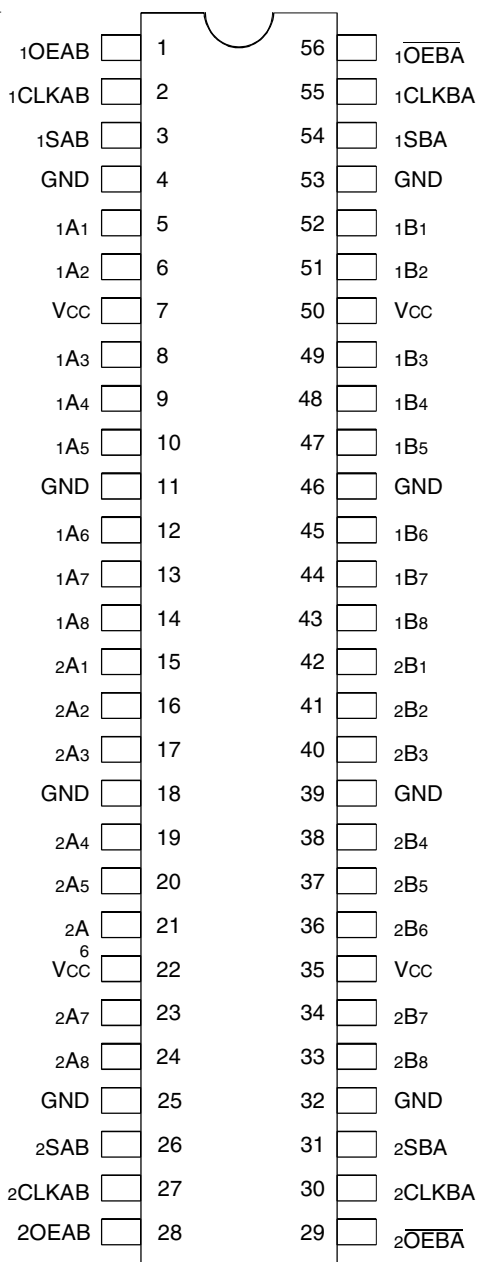
Data on the A or B data bus, or both, can be stored in the internal D-flip-flops by low-to-high transitions at the appropriate clock pins ($xCLKAB$ or $xCLKBA$), regardless of the select or enable control pins. Flow-through organization of signal pins simplifies layout. All inputs are designed with hysteresis for improved noise margin.

The FCT162652T has balanced output drive with current limiting resistors. This offers low ground bounce, minimal undershoot, and controlled output fall times—reducing the need for external series terminating resistors. The FCT162652T is a plug-in replacement for the FCT16652T and ABT16652 for on-board bus interface applications.

FUNCTIONAL BLOCK DIAGRAM



PIN CONFIGURATION



SSOP/ TSSOP/ CERPACK
TOP VIEW

ABSOLUTE MAXIMUM RATINGS⁽¹⁾

Symbol	Description	Max	Unit
VTERM ⁽²⁾	Terminal Voltage with Respect to GND	-0.5 to 7	V
VTERM ⁽³⁾	Terminal Voltage with Respect to GND	-0.5 to V _{CC} +0.5	V
TSTG	Storage Temperature	-65 to +150	°C
I _{OUT}	DC Output Current	-60 to +120	mA

NOTES:

- Stresses greater than those listed under ABSOLUTE MAXIMUM RATINGS may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect reliability.
- All device terminals except FCT162XXX Output and I/O terminals.
- Output and I/O terminals for FCT162XXX.

CAPACITANCE (T_A = +25°C, f = 1.0MHz)

Symbol	Parameter ⁽¹⁾	Conditions	Typ.	Max.	Unit
C _{IN}	Input Capacitance	V _{IN} = 0V	4.5	6	pF
C _{OUT}	Output Capacitance	V _{OUT} = 0V	5.5	8	pF

NOTE:

- This parameter is measured at characterization but not tested.

PIN DESCRIPTION

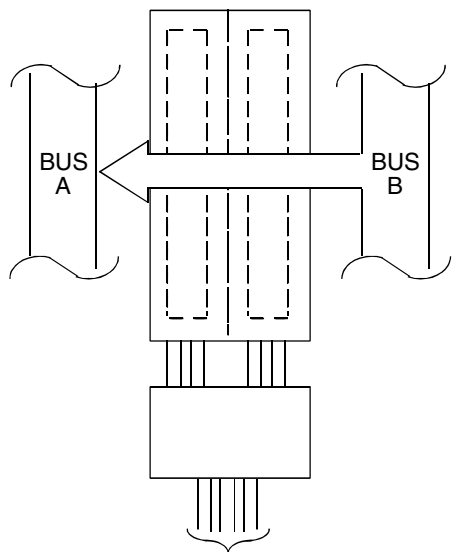
Pin Names	Description
xAx	Data Register A Inputs Data Register B Outputs
xBx	Data Register B Inputs Data Register A Outputs
xCLKAB, xCLKBA	Clock Pulse Inputs
xSAB, xSBA	Output Data Source Select Inputs
xOEAB, xOEBA	Output Enable Inputs

FUNCTION TABLE

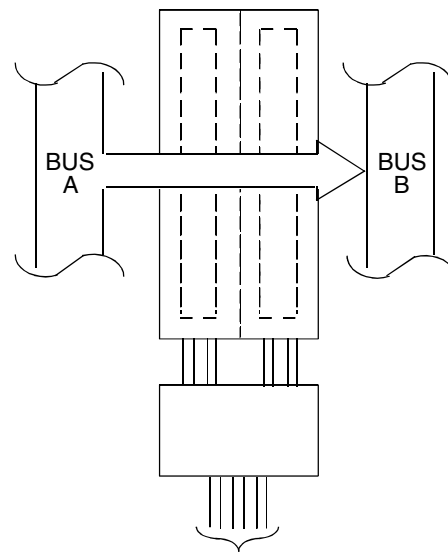
Inputs						Data I/O ⁽¹⁾		Operation or Function
xOEAB	xOEBA	xCLKAB	xCLKBA	xSAB	xSBA	xAx	xBx	
L L	H H	H or L ↑	H or L ↑	X X	X X	Input	Input	Isolation Store A and B Data
X H	H H	↑ ↑	H or L ↑	X X ⁽²⁾	X X	Input Input	Unspecified ⁽¹⁾ Output	Store A, Hold B Store A in Both Registers
L L	X L	H or L ↑	↑ ↑	X X	X X ⁽²⁾	Unspecified ⁽¹⁾ Output	Input Input	Hold A, Store B Store B in both Registers
L L	L L	X X	X H or L	X X	L H	Output	Input	Real Time B Data to A Bus Stored B Data to A Bus
H H	H H	X H or L	X X	L H	X X	Input	Output	Real Time A Data To B Bus Stored A Data to B Bus
H	L	H or L	H or L	H	H	Output	Output	Stored A Data to B Bus and Stored B Data to A Bus

NOTES:

1. The data output functions may be enabled or disabled by various signals at the xOEAB or xOEBA inputs. Data input functions are always enabled, i.e., data at the bus pins will be stored on every LOW-to-HIGH transition on the clocks inputs.
2. Select control = L: clocks can occur simultaneously.
Select control = H: clocks must be staggered to load both registers.
3. H = HIGH Voltage Level
L = LOW Voltage Level
X = Don't care
↑ = LOW-to-HIGH Transition

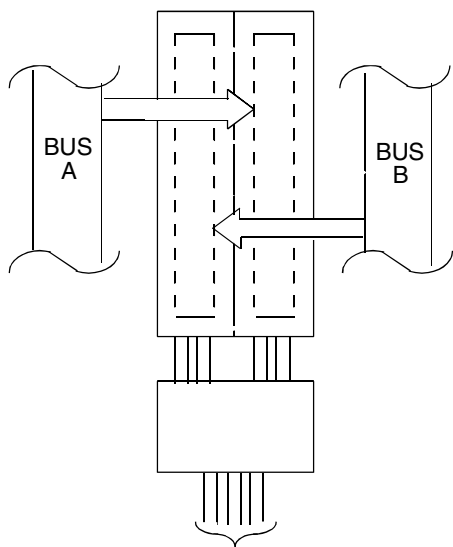


xOEAB	xOEBA	xCLKAB	xCLKBA	xSAB	xSBA
L	L	X	X	X	L



xOEAB	xOEBA	xCLKAB	xCLKBA	xSAB	xSBA
H	H	X	X	L	X

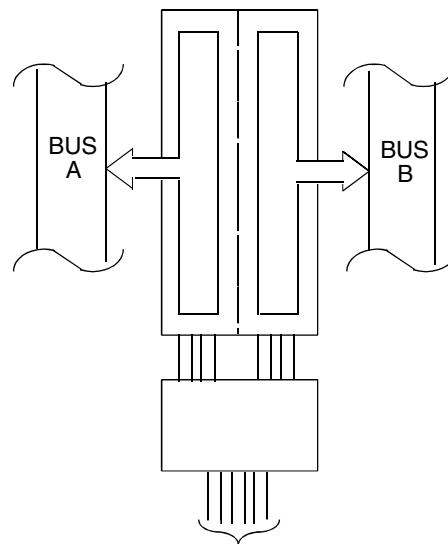
**Real-time Transfer
Bus B to A**



xOEAB	xOEBA	xCLKAB	xCLKBA	xSAB	xSBA
X	H	↑	X	X	X
L	X	X	↑	X	X
L	H	↑	↑	X	X

**Storage From
A and/or B**

**Real-time Transfer
Bus A to B**



xOEAB	xOEBA	xCLKAB	xCLKBA	xSAB	xSBA
H	L	H or L	H or L	H	H

**Transfer Stored
Data to A and/or B**

DC ELECTRICAL CHARACTERISTICS OVER OPERATING RANGE

Following Conditions Apply Unless Otherwise Specified:

Industrial: $T_A = -40^{\circ}\text{C}$ to $+85^{\circ}\text{C}$, $V_{CC} = 5.0\text{V} \pm 10\%$; Military: $T_A = -55^{\circ}\text{C}$ to $+125^{\circ}\text{C}$, $V_{CC} = 5.0\text{V} \pm 10\%$

Symbol	Parameter	Test Conditions ⁽¹⁾		Min.	Typ. ⁽²⁾	Max.	Unit
V_{IH}	Input HIGH Level	Guaranteed Logic HIGH Level		2	—	—	V
V_{IL}	Input LOW Level	Guaranteed Logic LOW Level		—	—	0.8	V
I_{IH}	Input HIGH Current (Input pins) ⁽⁴⁾	$V_{CC} = \text{Max.}$	$V_I = V_{CC}$	—	—	± 1	μA
	Input HIGH Current (I/O pins) ⁽⁴⁾		$V_I = V_{CC}$	—	—	± 1	
I_{IL}	Input LOW Current (Input pins) ⁽⁴⁾	$V_{CC} = \text{Max.}$	$V_I = \text{GND}$	—	—	± 1	
	Input LOW Current (I/O pins) ⁽⁴⁾		$V_I = \text{GND}$	—	—	± 1	
I_{OZH}	High Impedance Output Current	$V_{CC} = \text{Max.}$	$V_O = 2.7\text{V}$	—	—	± 1	μA
I_{OZL}	(3-State Output pins) ⁽⁴⁾		$V_O = 0.5\text{V}$	—	—	± 1	
V_{IK}	Clamp Diode Voltage	$V_{CC} = \text{Min.}, I_{IN} = -18\text{mA}$		—	-0.7	-1.2	V
I_{OS}	Short Circuit Current	$V_{CC} = \text{Max.}, V_O = \text{GND}^{(3)}$		-80	-140	-250	mA
V_H	Input Hysteresis	—		—	100	—	mV
I_{CCL} I_{CCH} I_{CCZ}	Quiescent Power Supply Current	$V_{CC} = \text{Max.}$ $V_{IN} = \text{GND}$ or V_{CC}		—	5	500	μA

OUTPUT DRIVE CHARACTERISTICS

Symbol	Parameter	Test Conditions ⁽¹⁾		Min.	Typ. ⁽²⁾	Max.	Unit
I_{ODL}	Output LOW Current	$V_{CC} = 5\text{V}, V_{IN} = V_{IH}$ or $V_{IL}, V_O = 1.5\text{V}^{(3)}$		60	115	200	mA
I_{ODH}	Output HIGH Current	$V_{CC} = 5\text{V}, V_{IN} = V_{IH}$ or $V_{IL}, V_O = 1.5\text{V}^{(3)}$		-60	-115	-200	mA
V_{OH}	Output HIGH Voltage	$V_{CC} = \text{Min.}$ $V_{IN} = V_{IH}$ or V_{IL}	$I_{OH} = -16\text{mA MIL}$ $I_{OH} = -24\text{mA IND}$	2.4	3.3	—	V
V_{OL}	Output LOW Voltage	$V_{CC} = \text{Min.}$ $V_{IN} = V_{IH}$ or V_{IL}	$I_{OL} = 16\text{mA MIL}$ $I_{OL} = 24\text{mA IND}$	—	0.3	0.55	V

NOTES:

1. For conditions shown as Min. or Max., use appropriate value specified under Electrical Characteristics for the applicable device type.

2. Typical values are at $V_{CC} = 5.0\text{V}$, $+25^{\circ}\text{C}$ ambient.

3. Not more than one output should be shorted at one time. Duration of the test should not exceed one second.

4. The test limit of this parameter is $\pm 5\mu\text{A}$ at $T_A = -55^{\circ}\text{C}$.

POWER SUPPLY CHARACTERISTICS

Symbol	Parameter	Test Conditions ⁽¹⁾		Min.	Typ. ⁽²⁾	Max.	Unit
ΔI_{CC}	Quiescent Power Supply Current TTL Inputs HIGH	$V_{CC} = \text{Max.}$ $V_{IN} = 3.4V^{(3)}$		—	0.5	1.5	μA
I_{CCD}	Dynamic Power Supply Current ⁽⁴⁾	$V_{CC} = \text{Max.}$ Outputs Open $\overline{xOEAB} = \overline{xOEBA} = \text{GND}$ One Input Toggling 50% Duty Cycle	$V_{IN} = V_{CC}$ $V_{IN} = \text{GND}$	—	75	120	$\mu A / \text{MHz}$
I_C	Total Power Supply Current ⁽⁶⁾	$V_{CC} = \text{Max.}$ Outputs Open $f_{CP} = 10\text{MHz}$ ($xCLKBA$) 50% Duty Cycle $\overline{xOEAB} = \overline{xOEBA} = \text{GND}$ One Bit Toggling $f_i = 5\text{MHz}$ 50% Duty Cycle	$V_{IN} = V_{CC}$ $V_{IN} = \text{GND}$	—	0.8	1.7	mA
			$V_{IN} = 3.4V$ $V_{IN} = \text{GND}$	—	1.3	3.2	
		$V_{CC} = \text{Max.}$ Outputs Open $f_{CP} = 10\text{MHz}$ ($xCLKBA$) 50% Duty Cycle $\overline{xOEAB} = \overline{xOEBA} = \text{GND}$ Sixteen Bits Toggling $f_i = 2.5\text{MHz}$ 50% Duty Cycle	$V_{IN} = V_{CC}$ $V_{IN} = \text{GND}$	—	3.8	6.5 ⁽⁵⁾	
			$V_{IN} = 3.4V$ $V_{IN} = \text{GND}$	—	8.3	20 ⁽⁵⁾	

NOTES:

1. For conditions shown as max. or min., use appropriate value specified under Electrical Characteristics for the applicable device type.

2. Typical values are at $V_{CC} = 5.0V$, $+25^\circ\text{C}$ ambient.

3. Per TTL driven input ($V_{IN} = 3.4V$). All other inputs at V_{CC} or GND.

4. This parameter is not directly testable, but is derived for use in Total Power Supply Calculations.

5. Values for these conditions are examples of the I_{CC} formula. These limits are guaranteed but not tested.

6. $I_C = I_{QUIESCENT} + I_{INPUTS} + I_{DYNAMIC}$

$I_C = I_{CC} + \Delta I_{CC} D_H N_T + I_{CCD} (f_{CP} N_{CP} / 2 + f_i N_i)$

$I_{CC} = \text{Quiescent Current (} I_{CCL}, I_{CCH} \text{ and } I_{CCZ} \text{)}$

$\Delta I_{CC} = \text{Power Supply Current for a TTL High Input (} V_{IN} = 3.4V \text{)}$

$D_H = \text{Duty Cycle for TTL Inputs High}$

$N_T = \text{Number of TTL Inputs at } D_H$

$I_{CCD} = \text{Dynamic Current Caused by an Input Transition Pair (HLH or LHL)}$

$f_{CP} = \text{Clock Frequency for Register Devices (Zero for Non-Register Devices)}$

$N_{CP} = \text{Number of Clock Inputs at } f_{CP}$

$f_i = \text{Input Frequency}$

$N_i = \text{Number of Inputs at } f_i$

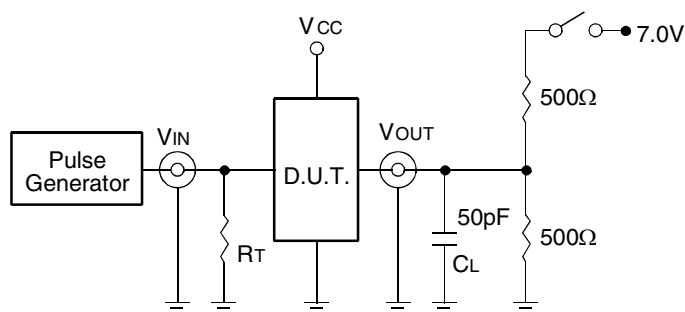
SWITCHING CHARACTERISTICS OVER OPERATING RANGE

Symbol	Parameter	Condition ⁽¹⁾	FCT162652AT				FCT162652CT				Unit
			Ind.		Mil.		Ind.		Mil.		
			Min. ⁽²⁾	Max.	Min. ⁽²⁾	Max.	Min. ⁽²⁾	Max.	Min. ⁽²⁾	Max.	
t _{PLH} t _{PHL}	Propagation Delay Bus to Bus	CL = 50pF RL = 500Ω	2	6.3	2	7.7	1.5	3.9	1.5	6	ns
t _{PZH} t _{PZL}	Output Enable Time xOEAB or xOEBA to Bus		2	9.8	2	10.5	1.5	4.8	1.5	8.9	ns
t _{PHZ} t _{PLZ}	Output Disable Time xOEAB or xOEBA to Bus		2	6.3	2	7.7	1.5	4.4	1.5	7.7	ns
t _{PLH} t _{PHL}	Propagation Delay Clock to Bus		2	6.3	2	7	1.5	4.1	1.5	6.3	ns
t _{PLH} t _{PHL}	Propagation Delay xSBA or xSAB to Bus		2	7.7	2	8.4	1.5	4.2	1.5	7	ns
t _{SU}	Set-up Time HIGH or LOW Bus to Clock		2	—	2	—	2	—	2	—	ns
t _H	Hold Time HIGH or LOW Bus to Clock		1.5	—	1.5	—	0	—	1.5	—	ns
t _W	Clock Pulse Width HIGH or LOW		5	—	5	—	3	—	5	—	ns
t _{sk(o)}	Output Skew ⁽³⁾		—	0.5	—	0.5	—	0.5	—	0.5	ns

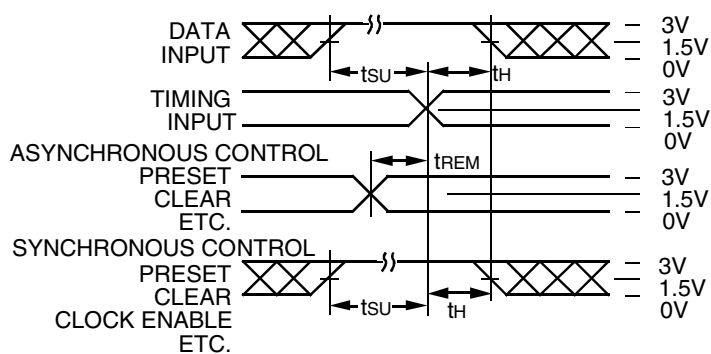
NOTES:

1. See test circuit and waveforms.
2. Minimum limits are guaranteed but not tested on Propagation Delays.
3. Skew between any two outputs of the same package switching in the same direction. This parameter is guaranteed by design.

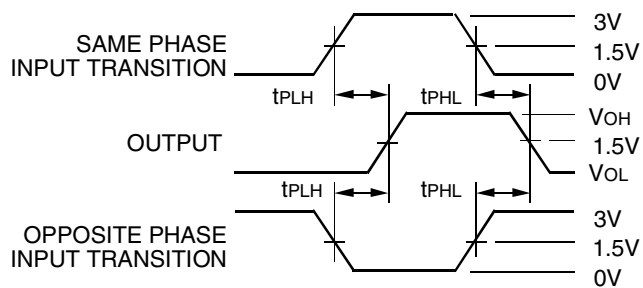
TEST CIRCUITS AND WAVEFORMS



Test Circuits for All Outputs



Set-up, Hold, and Release Times



Propagation Delay

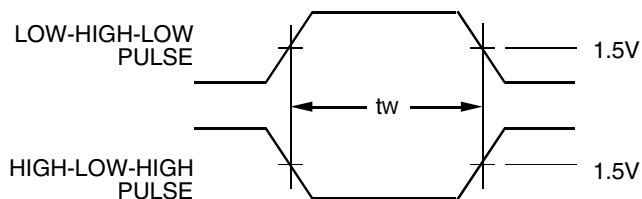
SWITCH POSITION

Test	Switch
Open Drain Disable Low Enable Low	Closed
All Other Tests	Open

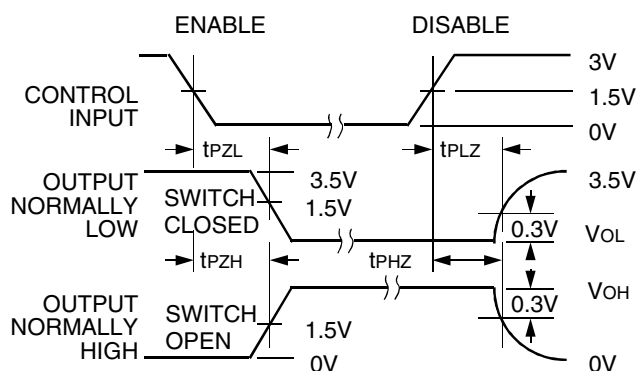
DEFINITIONS:

CL = Load capacitance: includes jig and probe capacitance.

RT = Termination resistance: should be equal to ZOUT of the Pulse Generator.



Pulse Width



Enable and Disable Times

NOTES:

- Diagram shown for input Control Enable-LOW and input Control Disable-HIGH.
- Pulse Generator for All Pulses: Rate $\leq 1.0\text{MHz}$; $t_F \leq 2.5\text{ns}$; $t_R \leq 2.5\text{ns}$.

ORDERING INFORMATION

IDT	XX	FCT	XXX	XXXX	XX	X		
Temp. Range	Family		Device Type	Package	Process			
						Blank	Industrial	
						B	MIL-STD-883, Class B	
						PV	<u>Industrial Options</u>	
						PA	Shrink Small Outline Package	
							Thin Shrink Small Outline Package	
						E	<u>Military Options</u>	
							CERPACK	
						652AT	16-Bit Bus Transceiver/Register	
						652CT		
						162	Double-Density, 5 Volt, Balanced Drive	
						54	– 55°C to +125°C	
						74	– 40°C to +85°C	

DATA SHEET DOCUMENT HISTORY

3/28/2002 Removed standard speed grade



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