FAST CMOS 8-INPUT MULTIPLEXER

IDT74FCT151T/AT/CT

FEATURES:

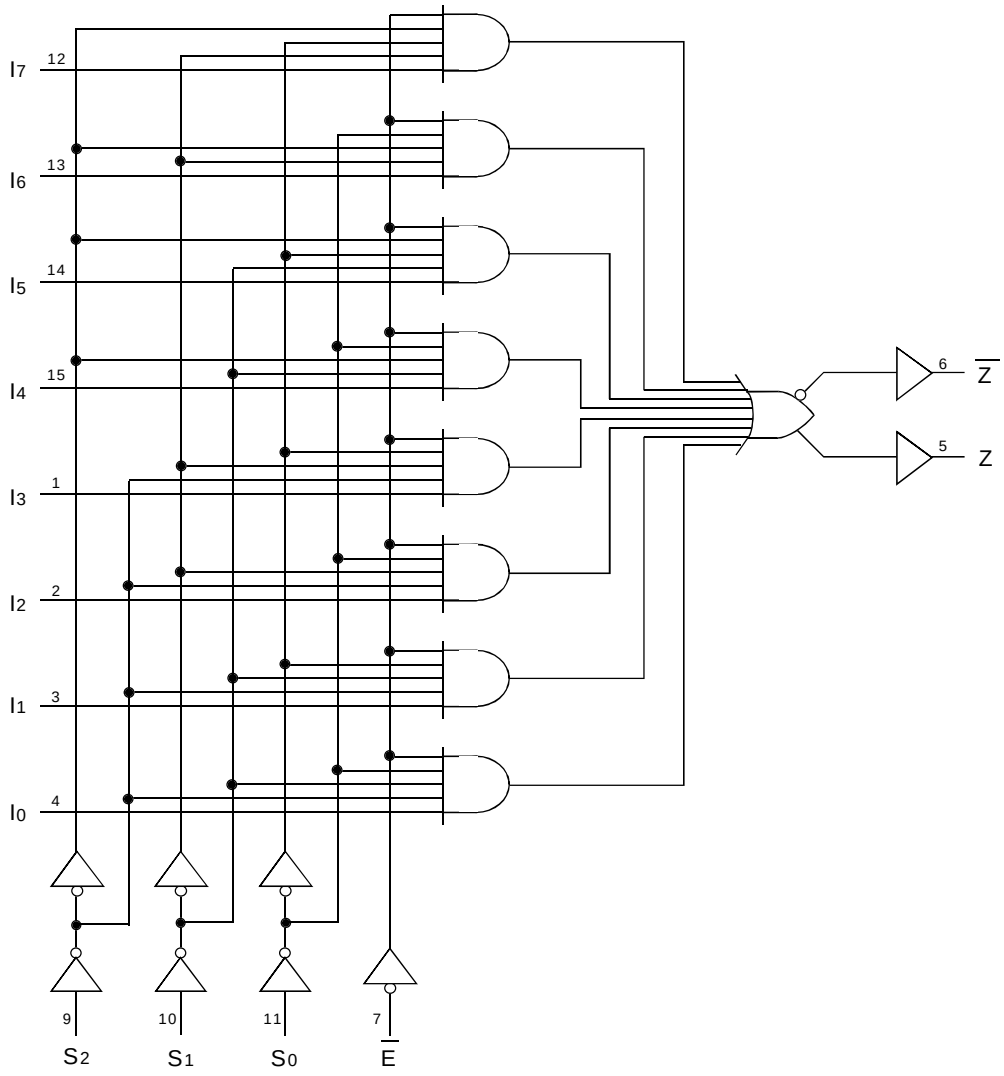
- A, and C speed grades
- Low input and output leakage ≤1µA (max.)
- CMOS power levels
- True TTL input and output compatibility
  - V_{OH} = 3.3V (typ.)
  - V_{OL} = 0.3V (typ.)
- High drive outputs (-15mA I_{OH}, 48mA I_{OL})
- Power off disable outputs permit "live insertion"
- Meets or exceeds JEDEC standard 18 specifications
- Available in SOIC and QSOP packages

DESCRIPTION:

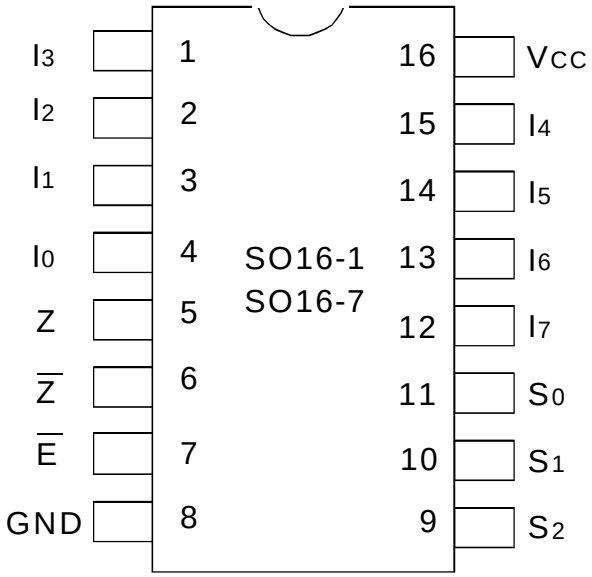
The IDT74FCT151T is a high-speed 8-input multiplexer built using an advanced dual metal CMOS technology. It selects one bit of data from up to eight sources under the control of three select inputs. Both assertion and negation outputs are provided.

The IDT74FCT151T has a common Active-low enable ($\overline{E}$) input. When $\overline{E}$ is low, data from one of eight inputs is routed to the complementary outputs according to the 3-bit code applied to the Select (S_0-S_2) inputs. A common application of the FCT151 is data routing from one of eight sources.

FUNCTIONAL BLOCK DIAGRAM



PIN CONFIGURATION



SOIC/ QSOP
TOP VIEW

ABSOLUTE MAXIMUM RATINGS(1)

Symbol	Rating	Max.	Unit
V_{TERM}(2)	Terminal Voltage with Respect to GND	–0.5 to +7	V
V_{TERM}(3)	Terminal Voltage with Respect to GND	–0.5 to V_{CC}+0.5	V
T_{STG}	Storage Temperature	–65 to +150	°C
I_{OUT}	DC Output Current	–60 to +120	mA

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NOTES:

1. Stresses greater than those listed under ABSOLUTE MAXIMUM RATINGS may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect reliability. No terminal voltage may exceed Vcc by +0.5V unless otherwise noted.
2. Inputs and Vcc terminals only.
3. Outputs and I/O terminals only.

CAPACITANCE (T_A = +25°C, f = 1.0MHz)

Symbol	Parameter(1)	Conditions	Typ.	Max.	Unit
C_{IN}	Input Capacitance	V_{IN} = 0V	6	10	pF
C_{OUT}	Output Capacitance	V_{OUT} = 0V	8	12	pF

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NOTE:

1. This parameter is measured at characterization but not tested.

PIN DESCRIPTION

Pin Names	Description
I_0 - I_7	Data Inputs
S_0 - S_2	Selects Inputs
$\overline{E}$	Enable Input (Active LOW)
Z	Data Output
$\overline{Z}$	Inverted Data Output

FUNCTION TABLE(1)

Inputs				Outputs	
S_2	S_1	S_0	$\overline{E}$	Z	$\overline{Z}$
X	X	X	H	L	H
L	L	L	L	I_0	$\overline{I}_0$
L	L	H	L	I_1	$\overline{I}_1$
L	H	L	L	I_2	$\overline{I}_2$
L	H	H	L	I_3	$\overline{I}_3$
H	L	L	L	I_4	$\overline{I}_4$
H	L	H	L	I_5	$\overline{I}_5$
H	H	L	L	I_6	$\overline{I}_6$
H	H	H	L	I_7	$\overline{I}_7$

NOTE:

1. H = HIGH Voltage Level
   L = LOW Voltage Level
   X = Don't Care
   Z = High Impedance

DC ELECTRICAL CHARACTERISTICS OVER OPERATING RANGE

Following Conditions Apply Unless Otherwise Specified:
Industrial: T_A = -40°C to +85°C, V_{CC} = 5.0V ± 5%

Symbol	Parameter	Test Conditions[1]		Min.	Typ.[2]	Max.	Unit
V_{IH}	Input HIGH Level	Guaranteed Logic HIGH Level		2	—	—	V
V_{IL}	Input LOW Level	Guaranteed Logic LOW Level		—	—	0.8	V
I_{IH}	Input HIGH Current[4]	V_{CC} = Max.	V_I = 2.7V	—	—	±1	µA
I_{IL}	Input LOW Current[4]	V_{CC} = Max.	V_I = 0.5V	—	—	±1	µA
I_{OZH}	High Impedance Output Current[4]	V_{CC} = Max.	V_O = 2.7V	—	—	±1	µA
I_{OZL}			V_O = 0.5V	—	—	±1	
I_I	Input HIGH Current[4]	V_{CC} = Max., V_I = V_{CC} (Max.)		—	—	20	µA
V_{IK}	Clamp Diode Voltage	V_{CC} = Min., I_N = –18mA		—	–0.7	–1.2	V
I_{OS}	Short Circuit Current	V_{CC} = Max.[3], V_O = GND		–60	–120	–225	mA
V_{OH}	Output HIGH Voltage	V_{CC} = Min.	I_{OH} = –8mA	2.4	3.3	—	V
		V_{IN} = V_{IH} or V_{IL}	I_{OH} = –15mA	2	3	—	
V_{OL}	Output LOW Voltage	V_{CC} = Min. V_{IN} = V_{IH} or V_{IL}	I_{OL} = 48mA	—	0.3	0.5	V
V_H	Input Hysteresis	—		—	200	—	mV
I_{CC}	Quiescent Power Supply Current	V_{CC} = Max. V_{IN} = GND or V_{CC}		—	0.01	1	mA

NOTES:
1. For conditions shown as Max. or Min., use appropriate value specified under Electrical Characteristics for the applicable device type.
2. Typical values are at V_{CC} = 5.0V, +25°C ambient and maximum loading.
3. Not more than one output should be shorted at one time. Duration of the short circuit test should not exceed one second.
4. The test limit for this parameter is ±5µ A at T_A = -55°C.

POWER SUPPLY CHARACTERISTICS

Symbol	Parameter	Test Conditions[1]		Min.	Typ.[2]	Max.	Unit
ΔI_{CC}	QuiescentPower Supply Current TTL Inputs HIGH	V_{CC} = Max. V_{IN} = 3.4V[3]		—	0.5	2	mA
I_{CCD}	Dynamic Power Supply Current[4]	V_{CC} = Max. Outputs Open $\overline{E}$ or $\overline{OE}$ = GND One Bit Toggling 50% Duty Cycle	V_{IN} = V_{CC} V_{IN} = GND	—	0.15	0.25	mA/ MHz
I_C	Total Power Supply Current[5]	V_{CC} = Max. Outputs Open fi = 10MHz 50% Duty Cycle $\overline{E}$ or $\overline{OE}$= GND One Input Toggling	V_{IN} = V_{CC} V_{IN} = GND	—	3.2	6.5	mA
			V_{IN} = 3.4V V_{IN} = GND	—	3.5	7.5	

NOTES:

1. For conditions shown as Max. or Min., use appropriate value specified under Electrical Characteristics for the applicable device type.
2. Typical values are at V_{CC} = 5.0V, +25°C ambient.
3. Per TTL driven input (V_{IN} = 3.4V). All other inputs at V_{CC} or GND.
4. This parameter is not directly testable, but is derived for use in Total Power Supply Calculations.
5. Values for these conditions are examples of the I_{CC} formula. These limits are guaranteed but not tested.
6. $I_C = I_{QUIESCENT} + I_{INPUTS} + I_{DYNAMIC}$
   $I_C = I_{CC} + \Delta I_{CC} D_H N_T + I_{CCD} (f_{CP}/2 + f_i N_O)$
   I_{CC} = Quiescent Current
   ΔI_{CC} = Power Supply Current for a TTL High Input (V_{IN} = 3.4V)
   D_H = Duty Cycle for TTL Inputs High
   N_T = Number of TTL Inputs at D_H
   I_{CCD} = Dynamic Current Caused by an Input Transition Pair (HLH or LHL)
   f_{CP} = Clock Frequency for Register Devices (Zero for Non-Register Devices)
   f_i = Input Frequency
   N_O = Number of Inputs at f_i
   All currents are in milliamps and all frequencies are in megahertz.

SWITCHING CHARACTERISTICS OVER OPERATING RANGE

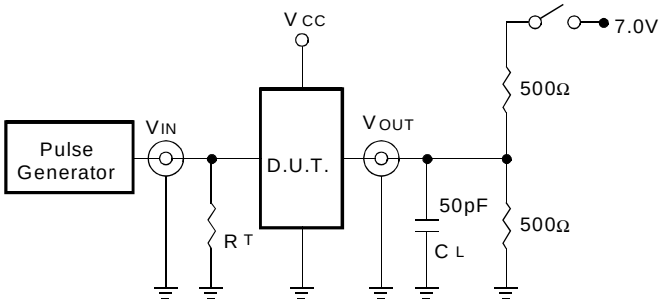
Symbol	Parameter	Condition[1]	IDT74FCT151T		IDT74FCT151AT		IDT74FCT151CT		Unit
			Min.[2]	Max.	Min.[2]	Max.	Min.[2]	Max.	
t_{PLH} t_{PHL}	Propagation Delay S_N to $\overline{Z}$	C_L = 50pF R_L = 500Ω	1.5	9	1.5	6.6	1.5	5.6	ns
t_{PLH} t_{PHL}	Propagation Delay S_N to Z		1.5	10.5	1.5	6.8	1.5	5.8	ns
t_{PLH} t_{PHL}	Propagation Delay $\overline{E}$ to$\overline{Z}$		1.5	7	1.5	5.6	1.5	4.8	ns
t_{PLH} t_{PHL}	Propagation Delay $\overline{E}$ to Z		1.5	9.5	1.5	5.8	1.5	5	ns
t_{PLH} t_{PHL}	Propagation Delay I_N to $\overline{Z}$		1.5	6.5	1.5	5.2	1.5	4.4	ns
t_{PLH} t_{PHL}	Propagation Delay I_N to Z		1.5	7.5	1.5	5.5	1.5	4.7	ns

NOTES:

1. See test circuit and waveforms.
2. Minimum limits are guaranteed but not tested on Propagation Delays.

TEST CIRCUITS AND WAVEFORMS

TEST CIRCUITS FOR ALL OUTPUTS



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SWITCH POSITION

Test	Switch
Open Drain Disable Low Enable Low	Closed
All Other Tests	Open

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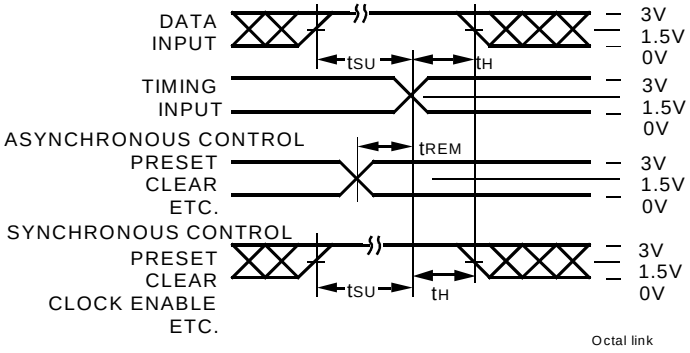
DEFINITIONS:

C_L = Load capacitance: includes jig and probe capacitance.

R_T = Termination resistance: should be equal to Z_{OUT} of the Pulse Generator.

SET-UP, HOLD, AND RELEASE TIMES



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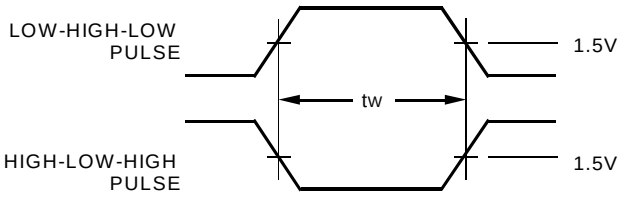
PULSE WIDTH



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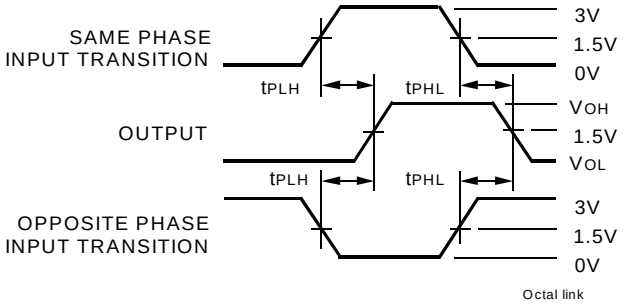
PROPAGATION DELAY



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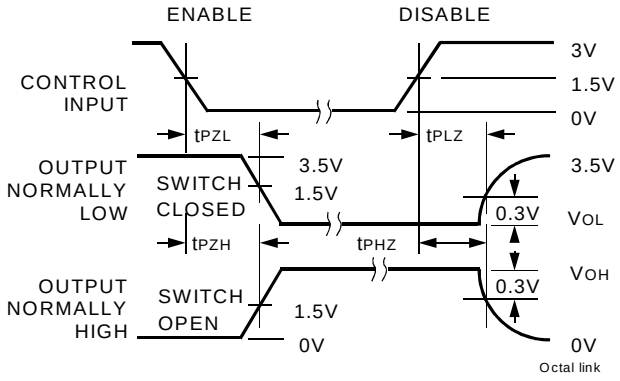
ENABLE AND DISABLE TIMES



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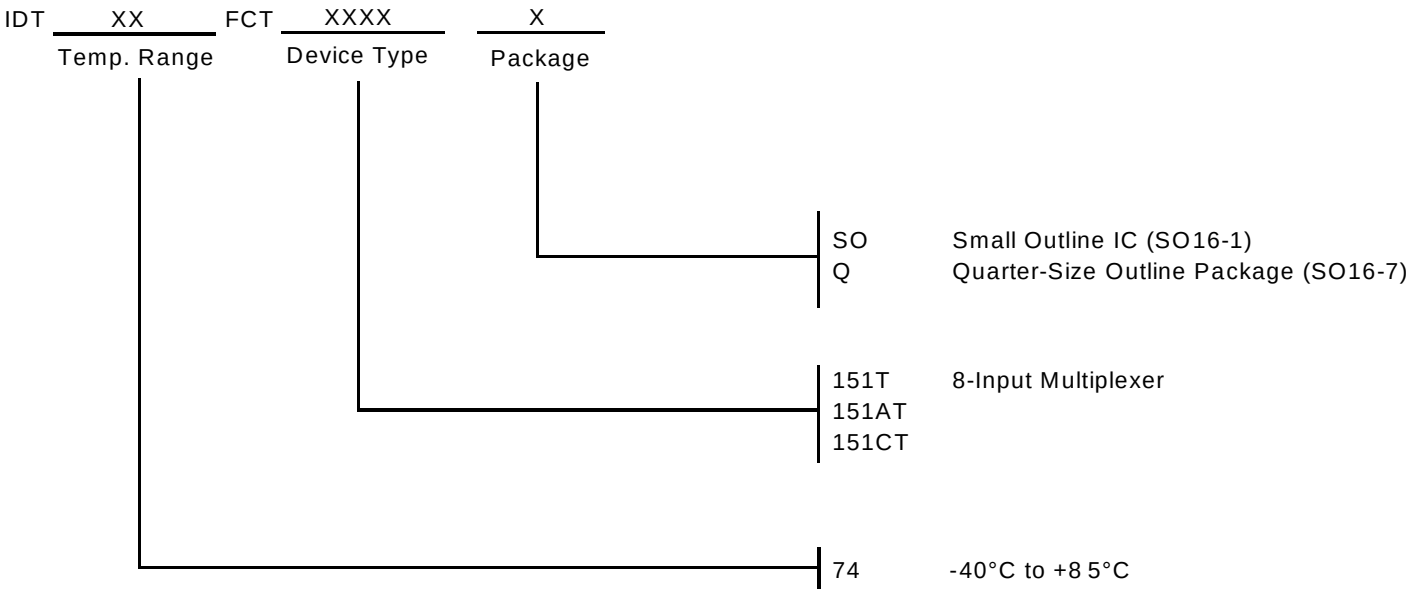
NOTES:

1. Diagram shown for input Control Enable-LOW and input Control Disable-HIGH
2. Pulse Generator for All Pulses: Rate ≤ 1.0MHz; t_F ≤ 2.5ns; t_R ≤ 2.5ns

ORDERING INFORMATION



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