



3.3V CMOS 9-BIT, 4-PORT UNIVERSAL BUS EXCHANGER WITH 3-STATE OUTPUTS AND BUS-HOLD

IDT74ALVCHR16409

FEATURES:

- 0.5 MICRON CMOS Technology
- Typical $t_{SK(0)}$ (Output Skew) < 250ps
- ESD > 2000V per MIL-STD-883, Method 3015;
> 200V using machine model (C = 200pF, R = 0)
- 0.635mm pitch SSOP, 0.50mm pitch TSSOP,
and 0.40mm pitch TVSOP packages
- Extended commercial range of -40°C to $+85^{\circ}\text{C}$
- $V_{CC} = 3.3\text{V} \pm 0.3\text{V}$, Normal Range
- $V_{CC} = 2.7\text{V}$ to 3.6V , Extended Range
- $V_{CC} = 2.5\text{V} \pm 0.2\text{V}$
- CMOS power levels (0.4 μW typ. static)
- Rail-to-Rail output swing for increased noise margin

Drive Features for ALVCHR16409:

- Balanced Output Drivers: $\pm 12\text{mA}$
- Low switching noise

APPLICATIONS:

- 3.3V High Speed Systems
- 3.3V and lower voltage computing systems

DESCRIPTION:

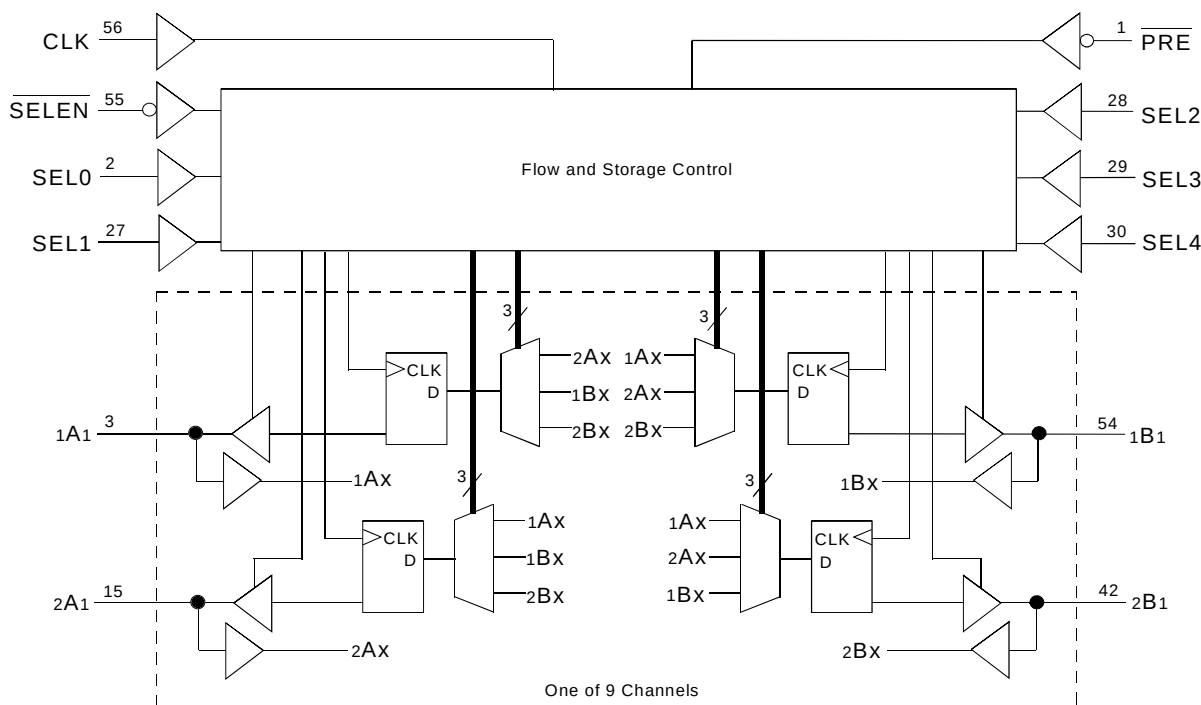
This 9-bit, 4-port universal bus exchanger is built using advanced dual metal CMOS technology. The ALVCHR16409 allows synchronous data exchange between four different buses. Data flow is controlled by the select (SEL0–SEL4) inputs. A data-flow state is stored on the rising edge of the clock (CLK) input if the select-enable (SELEN) input is low. Once a data-flow state has been established, data is stored in the flip-flop on the rising edge of CLK if SELEN is high. The data-flow control logic is designed to allow glitch-free data transmission.

When preset ($\overline{\text{PRE}}$) transitions high, the outputs are disabled immediately without waiting for a clock pulse. To leave the high-impedance state, both $\overline{\text{PRE}}$ and $\overline{\text{SELEN}}$ must be low and a clock pulse must be applied.

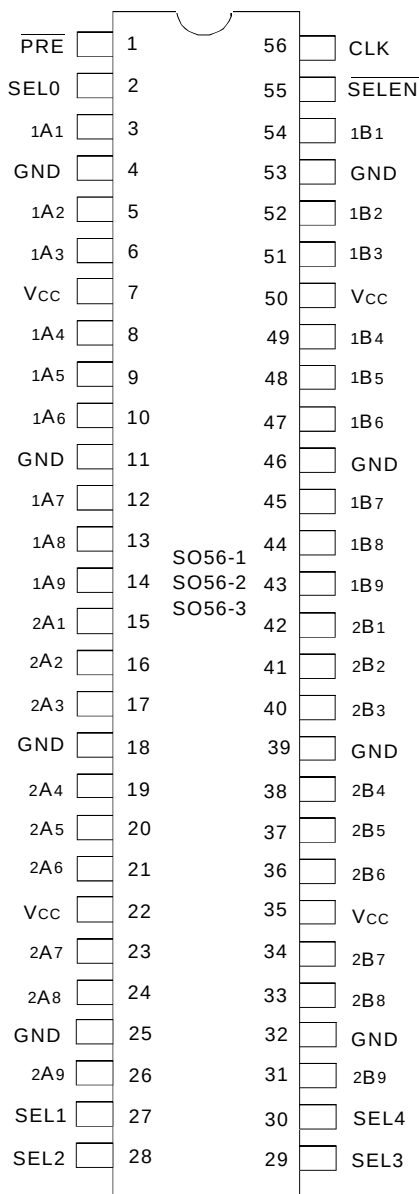
The ALVCHR16409 has been designed with a $\pm 24\text{mA}$ output driver. This driver is capable of driving a moderate to heavy load while maintaining speed performance.

The ALVCHR16409 has “bus-hold” which retains the inputs’ last state whenever the input bus goes to a high impedance. This prevents floating inputs and eliminates the need for pull-up/down resistors.

FUNCTIONAL BLOCK DIAGRAM



PIN CONFIGURATION



SSOP/TSSOP/TVSOP
TOP VIEW

PIN DESCRIPTION

Pin Names	Description
$\overline{\text{PRE}}$	Preset Input (Active LOW)
$\overline{\text{SELEN}}$	Select Enable Input (Active LOW)
SELE0-SEL4	Select Inputs
CLK	Clock Input
xAx	A-to-B Data Inputs or B-to-A 3-State Outputs ⁽¹⁾
xBx	B-to-A Data Inputs or A-to-B 3-State Outputs ⁽¹⁾

NOTE:

- These pins have "Bus-Hold." All other pins are standard inputs, outputs, or I/Os.

ABSOLUTE MAXIMUM RATING ⁽¹⁾

Symbol	Description	Max.	Unit
$V_{\text{TERM}}^{(2)}$	Terminal Voltage with Respect to GND	-0.5 to +4.6	V
$V_{\text{TERM}}^{(3)}$	Terminal Voltage with Respect to GND	-0.5 to $V_{\text{CC}} + 0.5$	V
T_{STG}	Storage Temperature	-65 to +150	°C
I_{OUT}	DC Output Current	-50 to +50	mA
I_{IK}	Continuous Clamp Current, $V_{\text{I}} < 0$ or $V_{\text{I}} > V_{\text{CC}}$	±50	mA
I_{OK}	Continuous Clamp Current, $V_{\text{O}} < 0$	-50	mA
I_{CC}	Continuous Current through each V_{CC} or GND	±100	mA

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NOTES:

- Stresses greater than those listed under ABSOLUTE MAXIMUM RATINGS may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect reliability.
- V_{CC} terminals.
- All terminals except V_{CC} .

CAPACITANCE ($T_{\text{A}} = +25^{\circ}\text{C}$, $f = 1.0\text{MHz}$)

Symbol	Parameter ⁽¹⁾	Conditions	Typ.	Max.	Unit
C_{IN}	Input Capacitance	$V_{\text{IN}} = 0\text{V}$	5	7	pF
C_{OUT}	Output Capacitance	$V_{\text{OUT}} = 0\text{V}$	7	9	pF
$C_{\text{I/O}}$	I/O Port Capacitance	$V_{\text{IN}} = 0\text{V}$	7	9	pF

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NOTE:

- As applicable to the device type.

FUNCTION TABLE ⁽¹⁾

Inputs		Output
CLK	Send Port	Receive Port
↑	L	L
↑	H	H
H	X	$B_0^{(2)}$
L	X	$B_0^{(2)}$

NOTES:

- H = HIGH Voltage Level
L = LOW Voltage Level
X = Don't Care
↑ = LOW-to-HIGH Transition
- B_0 = Output level before the indicated steady-state input conditions were established.

DATA FLOW CONTROL

Inputs								Data Flow
$\overline{\text{PRE}}$	$\overline{\text{SELEN}}$	CLK	SEL0	SEL1	SEL2	SEL3	SEL4	
H	X	X	X	X	X	X	X	All outputs disabled
L	H	↑	X	X	X	X	X	No change
L	L	↑	0	0	0	0	0	None, all I/Os off
L	L	↑	0	0	0	0	1	Not used
L	L	↑	0	0	0	1	0	Not used
L	L	↑	0	0	0	1	1	Not used
L	L	↑	0	0	1	0	0	Not used
L	L	↑	0	0	1	0	1	Not used
L	L	↑	0	0	1	1	0	Not used
L	L	↑	0	0	1	1	1	Not used
L	L	↑	0	1	0	0	0	2A to 1A and 1B to 2B
L	L	↑	0	1	0	0	1	2A to 1A
L	L	↑	0	1	0	1	0	2B to 1B
L	L	↑	0	1	0	1	1	2A to 1A and 2B to 1B
L	L	↑	0	1	1	0	0	1A to 2A and 1B to 2B
L	L	↑	0	1	1	0	1	1A to 2A
L	L	↑	0	1	1	1	0	1B to 2B
L	L	↑	0	1	1	1	1	1A to 2A and 2B to 1B
L	L	↑	1	0	0	0	0	1A to 1B and 2B to 2A
L	L	↑	1	0	0	0	1	1A to 1B
L	L	↑	1	0	0	1	0	2A to 2B
L	L	↑	1	0	0	1	1	1A to 1B and 2A to 2B
L	L	↑	1	0	1	0	0	1B to 1A and 2A to 2B
L	L	↑	1	0	1	0	1	1B to 1A
L	L	↑	1	0	1	1	0	2B to 2A
L	L	↑	1	0	1	1	1	1B to 1A and 2B to 2A
L	L	↑	1	1	0	0	0	2B to 1A and 2A to 1B
L	L	↑	1	1	0	0	1	1B to 2A
L	L	↑	1	1	0	1	0	2B to 1A
L	L	↑	1	1	0	1	1	2B to 1A and 1B to 2A
L	L	↑	1	1	1	0	0	1A to 2B and 1B to 2A
L	L	↑	1	1	1	0	1	1A to 2B
L	L	↑	1	1	1	1	0	2A to 1B
L	L	↑	1	1	1	1	1	1A to 2B and 2A to 1B

DC ELECTRICAL CHARACTERISTICS OVER OPERATING RANGE

Following Conditions Apply Unless Otherwise Specified:

Operating Condition: TA = – 40°C to +85°C

Symbol	Parameter	Test Conditions		Min.	Typ. ⁽¹⁾	Max.	Unit
VIH	Input HIGH Voltage Level	VCC = 2.3V to 2.7V		1.7	—	—	V
		VCC = 2.7V to 3.6V		2	—	—	
VIL	Input LOW Voltage Level	VCC = 2.3V to 2.7V		—	—	0.7	V
		VCC = 2.7V to 3.6V		—	—	0.8	
IiH	Input HIGH Current	VCC = 3.6V	Vi = VCC	—	—	± 5	μA
IiL	Input LOW Current	VCC = 3.6V	Vi = GND	—	—	± 5	
IoZH IoZL	High Impedance Output Current (3-State Output pins)	VCC = 3.6V	Vo = VCC	—	—	± 10	μA
			Vo = GND	—	—	± 10	μA
VIK	Clamp Diode Voltage	VCC = 2.3V, IIN = – 18mA		—	– 0.7	– 1.2	V
VH	Input Hysteresis	VCC = 3.3V		—	100	—	mV
ICCL ICCH IC CZ	Quiescent Power Supply Current	VCC = 3.6V VIN = GND or VCC		—	0.1	40	μA
ΔICC	Quiescent Power Supply Current Variation	One input at VCC – 0.6V, other inputs at VCC or GND		—	—	750	μA

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NOTE:

1. Typical values are at VCC = 3.3V, +25°C ambient.

BUS-HOLD CHARACTERISTICS

Symbol	Parameter ⁽¹⁾	Test Conditions		Min.	Typ. ⁽²⁾	Max.	Unit
IBHH IBHL	Bus-Hold Input Sustain Current	VCC = 3.0V	Vi = 2.0V	– 75	—	—	μA
			Vi = 0.8V	75	—	—	
IBHH IBHL	Bus-Hold Input Sustain Current	VCC = 2.3V	Vi = 1.7V	– 45	—	—	μA
			Vi = 0.7V	45	—	—	
IBHHO IBHLO	Bus-Hold Input Overdrive Current	VCC = 3.6V	Vi = 0 to 3.6V	—	—	± 500	μA

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NOTES:

1. Pins with Bus-hold are identified in the pin description.
2. Typical values are at VCC = 3.3V, +25°C ambient.

OUTPUT DRIVE CHARACTERISTICS

Symbol	Parameter	Test Conditions ⁽¹⁾		Min.	Max.	Unit
VOH	Output HIGH Voltage	VCC = 2.3V to 3.6V	IOH = – 0.1mA	VCC – 0.2	—	V
		VCC = 2.3V	IOH = – 4mA	1.9	—	
			IOH = – 6mA	1.7	—	
		VCC = 2.7V	IOH = – 4mA	2.2	—	
			IOH = – 8mA	2	—	
		VCC = 3.0V	IOH = – 6mA	2.4	—	
			IOH = – 12mA	2	—	
VOL	Output LOW Voltage	VCC = 2.3V to 3.6V	IOL = 0.1mA	—	0.2	V
		VCC = 2.3V	IOL = 4mA	—	0.4	
			IOL = 6mA	—	0.55	
		VCC = 2.7V	IOL = 4mA	—	0.4	
			IOL = 8mA	—	0.6	
		VCC = 3.0V	IOL = 6mA	—	0.55	
			IOL = 12mA	—	0.8	

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NOTE:

1. VIH and VIL must be within the min. or max. range shown in the DC ELECTRICAL CHARACTERISTICS OVER OPERATING RANGE table for the appropriate VCC range. TA = – 40°C to + 85°C.

OPERATING CHARACTERISTICS, TA = 25°C

Symbol	Parameter	Test Conditions	VCC = 2.5V ± 0.2V	VCC = 3.3V ± 0.3V	Unit
			Typical	Typical	
CPD	Power Dissipation Capacitance per exchanger Outputs enabled	CL = 0pF, f = 10Mhz		60	pF
CPD	Power Dissipation Capacitance per exchanger Outputs disabled			60	pF

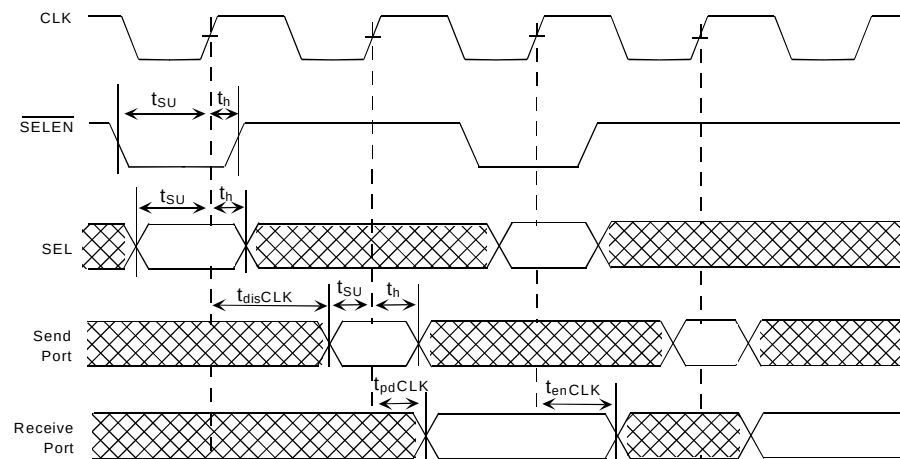
SWITCHING CHARACTERISTICS ⁽¹⁾

Symbol	Parameter	V _{CC} = 2.5V ± 0.2V		V _{CC} = 2.7V		V _{CC} = 3.3V ± 0.3V		Unit
		Min.	Max.	Min.	Max.	Min.	Max.	
f _{MAX}		120	—	120	—	120	—	MHz
t _{PLH} t _{PHL}	Propagation Delay CLK to xAx or xBx	1.5	6.9	—	7	1.5	6.2	ns
t _{PZH} t _{PZL}	Output Enable Time CLK to xAx or xBx	2.4	7.8	—	7.6	2	6.8	ns
t _{PHZ} t _{PLZ}	Output Disable Time CLK to xAx or xBx	2.3	7.1	—	6.4	2	6.1	ns
t _{PHZ} t _{PLZ}	Output Disable Time $\overline{\text{PRE}}$ to xAx or xBx	2.8	7.7	—	7	2.5	6.4	ns
t _{SU}	Setup Time, xAx or xBx before CLK↑	1.9	—	1.9	—	1.4	—	ns
t _H	Hold Time, xAx or xBx after CLK↑	0.8	—	0.8	—	1	—	ns
t _{SU}	Setup Time, SEL before CLK↑	5.1	—	4.2	—	3.5	—	ns
t _H	Hold Time, SEL after CLK↑	0	—	0	—	0	—	ns
t _{SU}	Setup Time, $\overline{\text{SELEN}}$ before CLK↑	2.5	—	2.5	—	1.8	—	ns
t _H	Hold Time, $\overline{\text{SELEN}}$ after CLK↑	0.5	—	0.5	—	0.8	—	ns
t _{SU}	Setup Time, $\overline{\text{PRE}}$ before CLK↑	1	—	1	—	0.7	—	ns
t _w	Pulse Width, CLK HIGH or LOW	4.2	—	4.2	—	3	—	ns
t _{sk(o)}	Output Skew ⁽²⁾	—	—	—	—	—	500	ps

NOTES:

- See test circuits and waveforms. T_A = – 40°C to + 85°C.
- Skew between any two outputs of the same package and switching in the same direction.

TIMING DIAGRAM



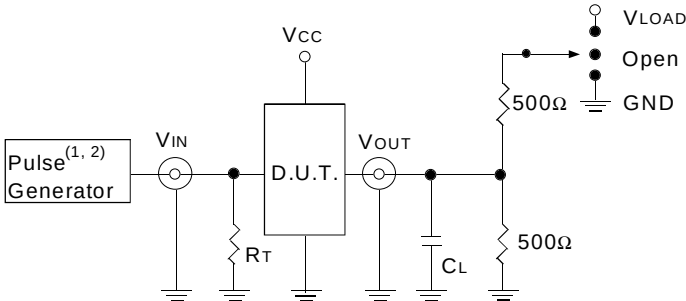
TEST CIRCUITS AND WAVEFORMS:

TEST CONDITIONS

Symbol	V _{CC} (1)= 3.3V±0.3V	V _{CC} (1)= 2.7V	V _{CC} (2)= 2.5V±0.2V	Unit
V _{LOAD}	6	6	2 x V _{CC}	V
V _{IH}	2.7	2.7	V _{CC}	V
V _T	1.5	1.5	V _{CC} / 2	V
V _{LZ}	300	300	150	mV
V _{HZ}	300	300	150	mV
C _L	50	50	30	pF

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TEST CIRCUITS FOR ALL OUTPUTS



DEFINITIONS:

C_L = Load capacitance: includes jig and probe capacitance.

R_T = Termination resistance: should be equal to Z_{OUT} of the Pulse Generator.

NOTES:

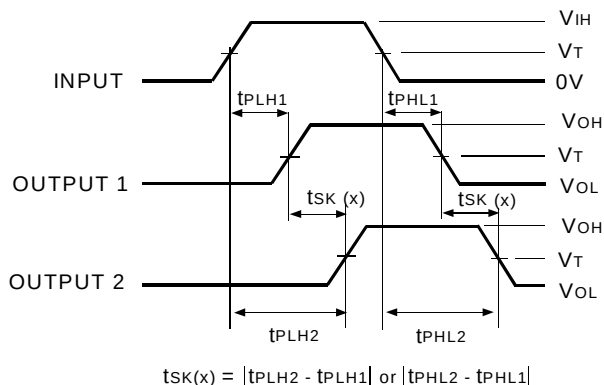
1. Pulse Generator for All Pulses: Rate ≤ 10MHz; t_F ≤ 2.5ns; t_R ≤ 2.5ns.
2. Pulse Generator for All Pulses: Rate ≤ 10MHz; t_F ≤ 2ns; t_R ≤ 2ns.

SWITCH POSITION

Test	Switch
Open Drain Disable Low Enable Low	V _{LOAD}
Disable High Enable High	GND
All Other tests	Open

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OUTPUT SKEW - t_{SK} (x)



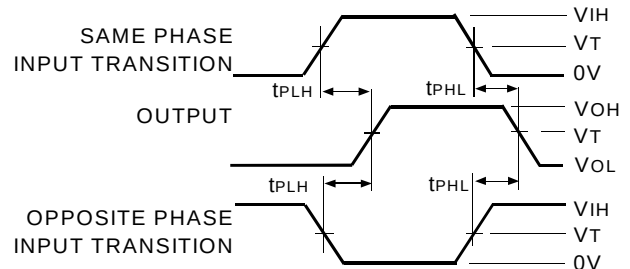
$$t_{SK}(x) = |t_{PLH2} - t_{PLH1}| \text{ or } |t_{PHL2} - t_{PHL1}|$$

ALVC Link

NOTES:

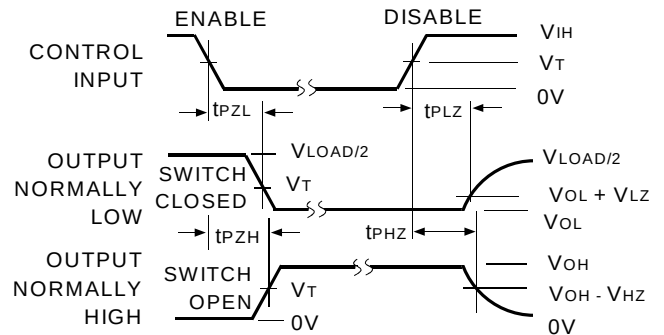
1. For t_{SK}(o) OUTPUT1 and OUTPUT2 are any two outputs.
2. For t_{SK}(b) OUTPUT1 and OUTPUT2 are in the same bank.

PROPAGATION DELAY



ALVC Link

ENABLE AND DISABLE TIMES

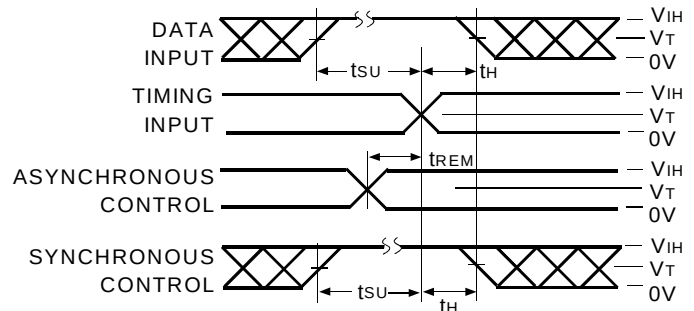


NOTE:

1. Diagram shown for input Control Enable-LOW and input Control Disable-HIGH.

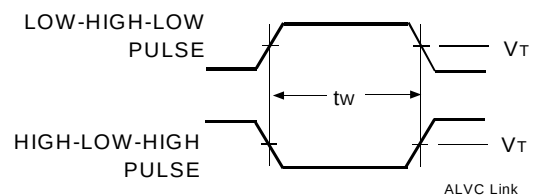
ALVC Link

SET-UP, HOLD, AND RELEASE TIMES



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PULSE WIDTH



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ORDERING INFORMATION

IDT	XX	ALVC	X	XX	XXX	XX	
	Temp. Range		Bus-Hold	Family	Device Type	Package	
						PV	Shrink Small Outline Package (SO56-1)
						PA	Thin Shrink Small Outline Package (SO56-2)
						PF	Thin Very Small Outline Package (SO56-3)
					409		9-Bit, 4-Port Universal Bus Exchanger With 3-State Outputs
					R16		Double-Density with Resistors, $\pm 12\text{mA}$
					H		Bus-Hold
					74		-40°C to $+85^{\circ}\text{C}$



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