3.3V CMOS 12-BIT TO 24-BIT REGISTERED BUS EXCHANGER WITH 3-STATE OUTPUTS AND BUS-HOLD

IDT74ALVCHR16270

FEATURES:

- 0.5 MICRON CMOS Technology
- Typical $t_{SK(0)}$ (Output Skew) < 250ps
- ESD > 2000V per MIL-STD-883, Method 3015; > 200V using machine model (C = 200pF, R = 0)
- 0.635mm pitch SSOP, 0.50mm pitch TSSOP, and 0.40mm pitch TVSOP packages
- Extended commercial range of – 40°C to + 85°C
- V_{CC} = 3.3V ± 0.3V, Normal Range
- V_{CC} = 2.7V to 3.6V, Extended Range
- V_{CC} = 2.5V ± 0.2V
- CMOS power levels (0.4µW typ. static)
- Rail-to-Rail output swing for increased noise margin

Drive Features for ALVCHR16270:

- Balanced Output Drivers: ±12mA
- Low switching noise

APPLICATIONS:

- 3.3V High Speed Systems
- 3.3V and lower voltage computing systems

DESCRIPTION:

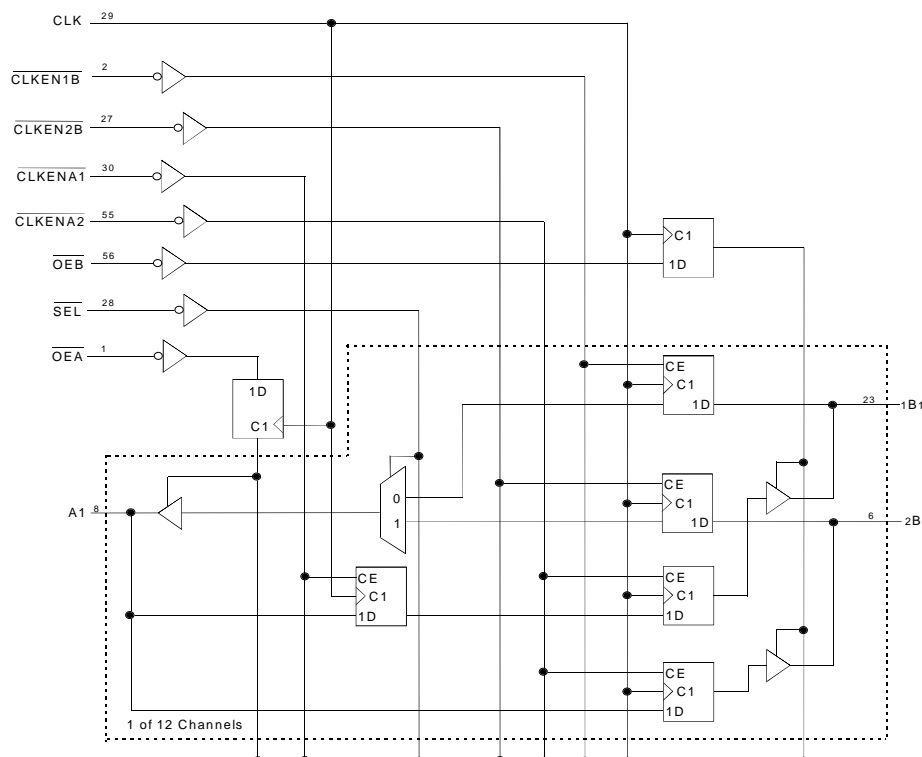This registered bus exchanger is built using advanced dual metal CMOS technology. The ALVCHR16270 is used in applications in which data must be transferred from a narrow high-speed bus to a wide lower-frequency bus.

This device provides synchronous data exchange between the two ports. Data is stored in the internal registers on the low-to-high transition of the clock (CLK) input when the appropriate clock-enable ($\overline{CLKEN}$) inputs are low. The select ($\overline{SEL}$) line selects 1B or 2B data for the A outputs. For data transfer in the A-to-B direction, a two-stage pipeline is provided in the A-to-1B path, with a single storage register in the A-to-2B path. Proper control of these inputs allows two sequential 12-bit words to be presented synchronously as a 24-bit word on the B-port. Data flow is controlled by the active-low output enables ($\overline{OEA}$ and $\overline{OEB}$). The control terminals are registered to synchronize the bus-direction changes with CLK.

The ALVCHR16270 has series resistors in the device output structure which will significantly reduce line noise when used with light loads. This driver has been designed to drive ±12mA at the designated threshold levels.

The ALVCHR16270 has "bus-hold" which retains the inputs' last state whenever the input goes to a high impedance. This prevents floating inputs and eliminates the need for pull-up/down resistors.
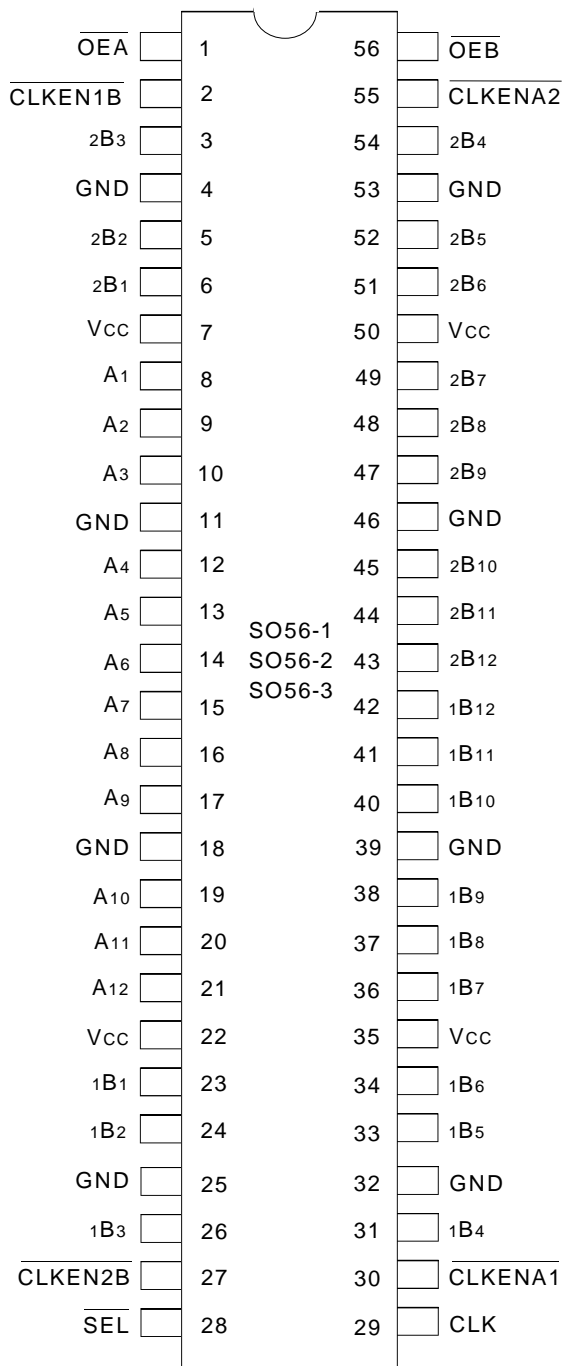
FUNCTIONAL BLOCK DIAGRAM

PIN CONFIGURATION

Left	Pin		Pin	Right
$\overline{OEA}$	1		56	$\overline{OEB}$
$\overline{CLKEN1B}$	2		55	$\overline{CLKENA2}$
2B3	3		54	2B4
GND	4		53	GND
2B2	5		52	2B5
2B1	6		51	2B6
Vcc	7		50	Vcc
A1	8		49	2B7
A2	9		48	2B8
A3	10		47	2B9
GND	11		46	GND
A4	12		45	2B10
A5	13	SO56-1	44	2B11
A6	14	SO56-2	43	2B12
A7	15	SO56-3	42	1B12
A8	16		41	1B11
A9	17		40	1B10
GND	18		39	GND
A10	19		38	1B9
A11	20		37	1B8
A12	21		36	1B7
Vcc	22		35	Vcc
1B1	23		34	1B6
1B2	24		33	1B5
GND	25		32	GND
1B3	26		31	1B4
$\overline{CLKEN2B}$	27		30	$\overline{CLKENA1}$
$\overline{SEL}$	28		29	CLK

**SSOP/
TSSOP/TVSOP
TOP VIEW**

FUNCTION TABLES [1]

OUTPUT ENABLE

Inputs			Outputs	
CLK	$\overline{OEA}$	$\overline{OEB}$	Ax	1Bx, 2Bx
↑	H	H	Z	Z
↑	H	L	Z	Active
↑	L	H	Active	Z
↑	L	L	Active	Active

A-TO-B STORAGE ($\overline{OEB}$ = L AND $\overline{OEA}$ = H)

Inputs				Outputs	
$\overline{CLKENA1}$	CLKENA2	CLK	Ax	1Bx	2Bx
L	H	X	X	1B0(2)	2B0(2)
L	H	X	X	1B0(2)	2B0(2)
L	L	↑	L	L(3)	L
L	L	↑	H	H(3)	H
H	L	↑	L	1B0(2)	L
H	L	↑	H	1B0(2)	H
H	H	X	X	1B0(2)	2B0(2)

B-TO-A STORAGE ($\overline{OEA}$ = L AND $\overline{OEB}$ = H)

Inputs						Outputs
$\overline{CLKEN1B}$	$\overline{CLKEN2B}$	CLK	$\overline{SEL}$	1Bx	2Bx	Ax
H	X	X	H	X	X	A0(2)
X	H	X	L	X	X	A0(2)
L	X	↑	H	L	X	L
L	X	↑	H	H	X	H
X	L	↑	L	X	L	L
X	L	↑	L	X	H	H

NOTES:
1. H = HIGH Voltage Level
   L = LOW Voltage Level
   X = Don't Care
   Z = High-Impedance
   ↑ = LOW-to-HIGH Transition
2. Output level before the indicated steady-state input conditions were established.
3. Two CLK edges are needed to propagate data.

PIN DESCRIPTION

Pin Names	I/O	Description
Ax$_{(1:12)}$	I/O	Bidirectional Data Port A. Usually connected to the CPU's Address/Data bus.[1]
1Bx$_{(1:12)}$	I/O	Bidirectional Data Port 1B. Usually connected to the even path or even bank of memory.[1]
2Bx$_{(1:12)}$	I/O	Bidirectional Data Port 2B. Usually connected to the odd path or odd bank of memory.[1]
CLK	I	Clock Input
$\overline{\text{CLKENA1}}$	I	Clock Enable Input for the A-1B Register. If $\overline{\text{CLKENA1}}$ is LOW during the rising edge of CLK, data will be clocked into register A-1B (Active LOW).
$\overline{\text{CLKENA2}}$	I	Clock Enable Input for the A-2B Register. If $\overline{\text{CLKENA2}}$ is LOW during the rising edge of CLK, data will be clocked into register A-2B (Active LOW).
$\overline{\text{CLKEN1B}}$	I	Clock Enable Input for the 1B-A Register. If $\overline{\text{CLKEN1B}}$ is LOW during the rising edge of CLK, data will be clocked into register 1B-A (Active LOW).
$\overline{\text{CLKEN2B}}$	I	Clock Enable Input for the 2B-A Register. If $\overline{\text{CLKEN2B}}$ is LOW during the rising edge of CLK, data will be clocked into register 2B-A (Active LOW).
$\overline{\text{SEL}}$	I	1B or 2B Port Selection. When HIGH during the rising edge of CLK, $\overline{\text{SEL}}$ enables data transfer from 1B Port to A Port. When LOW during the rising edge of CLK, $\overline{\text{SEL}}$ enables data transfer from 2B Port to A Port.
$\overline{\text{OEA}}$	I	Synchronous Output Enable for A Port (Active LOW)
$\overline{\text{OEB}}$	I	Synchronous Output Enable for B Port (Active LOW)

NOTE:
1. These pins have "Bus-Hold." All other pins are standard inputs,
   outputs, or I/Os.

ABSOLUTE MAXIMUM RATING [1]

Symbol	Description	Max.	Unit
V$_{TERM}$[2]	Terminal Voltage with Respect to GND	– 0.5 to + 4.6	V
V$_{TERM}$[3]	Terminal Voltage with Respect to GND	– 0.5 to V$_{CC}$ + 0.5	V
T$_{STG}$	Storage Temperature	– 65 to + 150	°C
I$_{OUT}$	DC Output Current	– 50 to + 50	mA
I$_{IK}$	Continuous Clamp Current, V$_I$ < 0 or V$_I$ > V$_{CC}$	± 50	mA
I$_{OK}$	Continuous Clamp Current, V$_O$ < 0	– 50	mA
I$_{CC}$ I$_{SS}$	Continuous Current through each V$_{CC}$ or GND	±100	mA

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NOTES:
1. Stresses greater than those listed under ABSOLUTE MAXIMUM RATINGS may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect reliability.
2. V$_{CC}$ terminals.
3. All terminals except V$_{CC}$.

CAPACITANCE (T$_A$ = +25°C, f = 1.0MHz)

Symbol	Parameter[1]	Conditions	Typ.	Max.	Unit
C$_{IN}$	Input Capacitance	V$_{IN}$ = 0V	5	7	pF
C$_{OUT}$	Output Capacitance	V$_{OUT}$ = 0V	7	9	pF
C$_{I/O}$	I/O Port Capacitance	V$_{IN}$ = 0V	7	9	pF

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NOTE:
1. As applicable to the device type.

DC ELECTRICAL CHARACTERISTICS OVER OPERATING RANGE

Following Conditions Apply Unless Otherwise Specified:

Operating Condition: TA = – 40°C to +85°C

Symbol	Parameter	Test Conditions		Min.	Typ.[1]	Max.	Unit
V_{IH}	Input HIGH Voltage Level	V_{CC} = 2.3V to 2.7V		1.7	—	—	V
		V_{CC} = 2.7V to 3.6V		2	—	—	
V_{IL}	Input LOW Voltage Level	V_{CC} = 2.3V to 2.7V		—	—	0.7	V
		V_{CC} = 2.7V to 3.6V		—	—	0.8	
I_{IH}	Input HIGH Current	V_{CC} = 3.6V	V_I = V_{CC}	—	—	± 5	µA
I_{IL}	Input LOW Current	V_{CC} = 3.6V	V_I = GND	—	—	± 5	
I_{OZH}	High Impedance Output Current	V_{CC} = 3.6V	V_O = V_{CC}	—	—	± 10	µA
I_{OZL}	(3-State Output pins)		V_O = GND	—	—	± 10	µA
V_{IK}	Clamp Diode Voltage	V_{CC} = 2.3V, I_{IN} = – 18mA		—	– 0.7	– 1.2	V
V_H	Input Hysteresis	V_{CC} = 3.3V		—	100	—	mV
I_{CCL} I_{CCH} I_{CCZ}	Quiescent Power Supply Current	V_{CC} = 3.6V V_{IN} = GND or V_{CC}		—	0.1	40	µA
ΔI_{CC}	Quiescent Power Supply Current Variation	One input at V_{CC} – 0.6V, other inputs at V_{CC} or GND		—	—	750	µA

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NOTE:
1. Typical values are at V_{CC} = 3.3V, +25°C ambient.

BUS-HOLD CHARACTERISTICS

Symbol	Parameter[1]	Test Conditions		Min.	Typ.[2]	Max.	Unit
I_{BHH}	Bus-Hold Input Sustain Current	V_{CC} = 3.0V	V_I = 2.0V	– 75	—	—	µA
I_{BHL}			V_I = 0.8V	75	—	—	
I_{BHH}	Bus-Hold Input Sustain Current	V_{CC} = 2.3V	V_I = 1.7V	– 45	—	—	µA
I_{BHL}			V_I = 0.7V	45	—	—	
I_{BHHO}	Bus-Hold Input Overdrive Current	V_{CC} = 3.6V	V_I = 0 to 3.6V	—	—	± 500	µA
I_{BHLO}							

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NOTES:
1. Pins with Bus-hold are identified in the pin description.
2. Typical values are at V_{CC} = 3.3V, +25°C ambient.

OUTPUT DRIVE CHARACTERISTICS

Symbol	Parameter	Test Conditions[1]		Min.	Max.	Unit
V_{OH}	Output HIGH Voltage	V_{CC} = 2.3V to 3.6V	I_{OH} = – 0.1mA	V_{CC} – 0.2	—	V
		V_{CC} = 2.3V	I_{OH} = – 4mA	1.9	—	
			I_{OH} = – 6mA	1.7	—	
		V_{CC} = 2.7V	I_{OH} = – 4mA	2.2	—	
			I_{OH} = – 8mA	2	—	
		V_{CC} = 3.0V	I_{OH} = – 6mA	2.4	—	
			I_{OH} = – 12mA	2	—	
V_{OL}	Output LOW Voltage	V_{CC} = 2.3V to 3.6V	I_{OL} = 0.1mA	—	0.2	V
		V_{CC} = 2.3V	I_{OL} = 4mA	—	0.4	
			I_{OL} = 6mA	—	0.55	
		V_{CC} = 2.7V	I_{OL} = 4mA	—	0.4	
			I_{OL} = 8mA	—	0.6	
		V_{CC} = 3.0V	I_{OL} = 6mA	—	0.55	
			I_{OL} = 12mA	—	0.8	

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NOTE:

1. V_{IH} and V_{IL} must be within the min. or max. range shown in the DC ELECTRICAL CHARACTERISTICS OVER OPERATING RANGE table for the appropriate V_{CC} range. T_A = – 40°C to + 85°C.

OPERATING CHARACTERISTICS, T_A = 25°C

Symbol	Parameter	Test Conditions	V_{CC} = 2.5V ± 0.2V	V_{CC} = 3.3V ± 0.3V	Unit
			Typical	Typical	
C_{PD}	Power Dissipation Capacitance Outputs enabled	C_L = 0pF, f = 10Mhz	—	—	pF
C_{PD}	Power Dissipation Capacitance Outputs disabled		—	—	pF

SWITCHING CHARACTERISTICS [1]

Symbol	Parameter	Vcc = 2.5V ± 0.2V		Vcc = 2.7V		Vcc = 3.3V ± 0.3V		Unit
		Min.	Max.	Min.	Max.	Min.	Max.	
tPLH tPHL	Propagation Delay CLK to xBx	2.5	6.9	—	6.4	1.7	5.6	ns
tPLH tPHL	Propagation Delay CLK to Ax	2.2	6.4	—	6	1.6	5.2	ns
tPLH tPHL	Propagation Delay $\overline{SEL}$ to Ax	2.4	7.2	—	7	1.6	6	ns
tPZH tPZL	Output Enable Time CLK to Ax or Bx	2.1	7.9	—	7.4	1.6	6.5	ns
tPHZ tPLZ	Output Disable Time CLK to Ax or Bx	3	7.8	—	7.1	1.7	6.2	ns
tSU	Setup Time, Ax data before CLK↑	4.1	—	3.8	—	3.1	—	ns
tSU	Setup Time, Bx data before CLK↑	0.9	—	1.2	—	0.9	—	ns
tSU	Setup Time, $\overline{CLKENA1}$ or $\overline{CLKENA2}$ before CLK↑	3.5	—	3.2	—	2.7	—	ns
tSU	Setup Time, $\overline{CLKEN1B}$ or $\overline{CLKEN2B}$ before CLK↑	3.4	—	3	—	2.6	—	ns
tSU	Setup Time, $\overline{OEB}$ or $\overline{OEA}$ before CLK↑	4.4	—	3.9	—	3.2	—	ns
tH	Hold Time, Ax data after CLK↑	0	—	0	—	0.2	—	ns
tH	Hold Time, Bx data after CLK↑	1.4	—	1	—	1.7	—	ns
tH	Hold Time, $\overline{CLKENA1}$ or $\overline{CLKENA2}$ after CLK↑	0	—	0.1	—	0.3	—	ns
tH	Hold Time, $\overline{CLKEN1B}$ or $\overline{CLKEN2B}$ after CLK↑	0	—	0	—	0.6	—	ns
tH	Hold Time, $\overline{OEB}$ or $\overline{OEA}$ after CLK↑	0	—	0	—	0.1	—	ns
tw	Pulse Width, CLK HIGH or LOW	3.3	—	3.3	—	3.3	—	ns
tSK(o)	Output Skew[2]	—	—	—	—	—	500	ps

NOTES:
1. See test circuits and waveforms. TA = – 40°C to + 85°C.
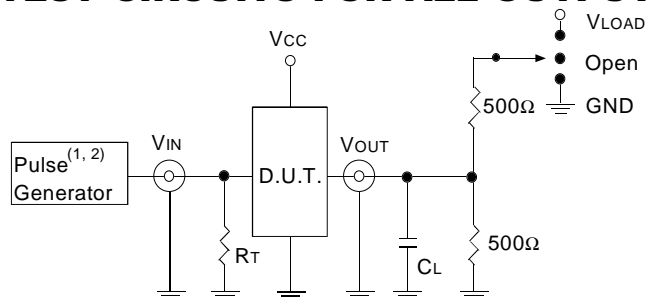2. Skew between any two outputs of the same package and switching in the same direction.

TEST CIRCUITS AND WAVEFORMS:

TEST CONDITIONS

Symbol	V_{CC}[(1)] = 3.3V±0.3V	V_{CC}[(1)] = 2.7V	V_{CC}[(2)] = 2.5V±0.2V	Unit
V_{LOAD}	6	6	2 x V_{CC}	V
V_{IH}	2.7	2.7	V_{CC}	V
V_T	1.5	1.5	V_{CC} / 2	V
V_{LZ}	300	300	150	mV
V_{HZ}	300	300	150	mV
C_L	50	50	30	pF

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TEST CIRCUITS FOR ALL OUTPUTS

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DEFINITIONS:
C_L = Load capacitance: includes jig and probe capacitance.
R_T = Termination resistance: should be equal to Z_{OUT} of the Pulse Generator.

NOTES:
1. Pulse Generator for All Pulses: Rate ≤ 10MHz; t_F ≤ 2.5ns; t_R ≤ 2.5ns.
2. Pulse Generator for All Pulses: Rate ≤ 10MHz; t_F ≤ 2ns; t_R ≤ 2ns.

SWITCH POSITION

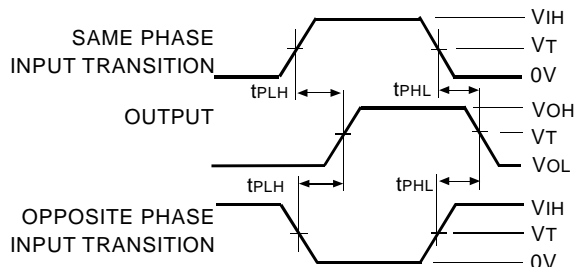| Test	Switch
Open Drain Disable Low Enable Low	V_{LOAD}
Disable High Enable High	GND
All Other tests	Open

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OUTPUT SKEW - t_{SK} (x)

$t_{SK}(x) = |t_{PLH2} - t_{PLH1}|$ or $|t_{PHL2} - t_{PHL1}|$
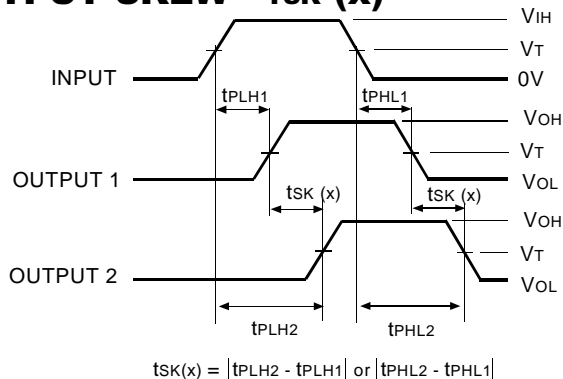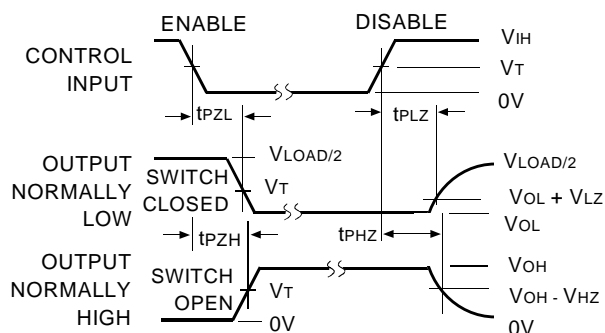
ALVC Link

NOTES:
1. For $t_{SK}(o)$ OUTPUT1 and OUTPUT2 are any two outputs.
2. For $t_{SK}(b)$ OUTPUT1 and OUTPUT2 are in the same bank.

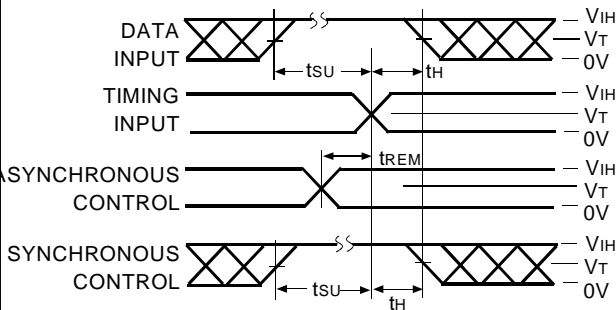## PROPAGATION DELAY

ALVC Link

ENABLE AND DISABLE TIMES

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NOTE:
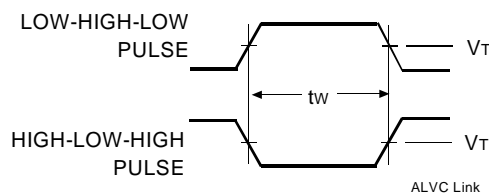1. Diagram shown for input Control Enable-LOW and input Control Disable-HIGH.

SET-UP, HOLD, AND RELEASE TIMES

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PULSE WIDTH

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ORDERING INFORMATION

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IDT    XX    ALVC    X       XX        XXX        XX
    Temp. Range   Bus-Hold  Family  Device Type  Package
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PV	Shrink Small Outline Package (SO56-1)
PA	Thin Shrink Small Outline Package (SO56-2)
PF	Thin Very Small Outline Package (SO56-3)
270	12-Bit To 24-Bit Registered Bus Exchanger with 3-State Outputs
R16	Double-Density, ±12mA
H	Bus-Hold
74	−40°C to +85°C