



3.3V CMOS 12-BIT TO 24-BIT MULTIPLEXED D-TYPE LATCH WITH 3-STATE OUTPUTS AND BUS-HOLD

IDT74ALVCHR16260

FEATURES:

- 0.5 MICRON CMOS Technology
- Typical $t_{SK(0)}$ (Output Skew) < 250ps
- ESD > 2000V per MIL-STD-883, Method 3015;
> 200V using machine model (C = 200pF, R = 0)
- 0.635mm pitch SSOP, 0.50mm pitch TSSOP,
and 0.40mm pitch TVSOP packages
- Extended commercial range of -40°C to $+85^{\circ}\text{C}$
- $V_{CC} = 3.3\text{V} \pm 0.3\text{V}$, Normal Range
- $V_{CC} = 2.7\text{V}$ to 3.6V , Extended Range
- $V_{CC} = 2.5\text{V} \pm 0.2\text{V}$
- CMOS power levels (0.4 μW typ. static)
- Rail-to-Rail output swing for increased noise margin

Drive Features for ALVCHR16260:

- Balanced Output Drivers: $\pm 12\text{mA}$
- Low switching noise

APPLICATIONS:

- 3.3V High Speed Systems
- 3.3V and lower voltage computing systems

DESCRIPTION:

This 12-bit to 24-bit multiplexed D-type latch is built using advanced dual metal technology. The ALVCHR16260 is used in

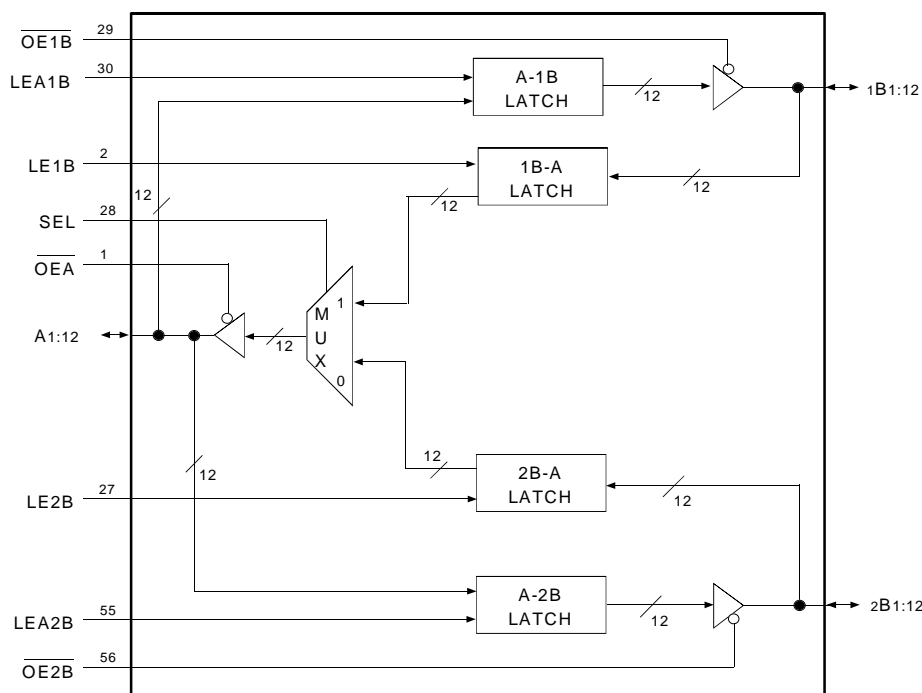
applications in which two separate data paths must be multiplexed onto, or demultiplexed from, a single data path. Typical applications include multiplexing and/or demultiplexing address and data information in microprocessor or bus-interface applications. This device also is useful in memory interleaving applications.

Three 12-bit I/O ports (A1-A12, 1B1-1B12, and 2B1-2B12) are available for address and/or data transfer. The output-enable ($\overline{\text{OE1B}}$, $\overline{\text{OE2B}}$, and $\overline{\text{OEA}}$) inputs control the bus transceiver functions. The $\overline{\text{OE1B}}$ and $\overline{\text{OE2B}}$ control signals also allow bank control in the A-to-B direction. Address and/or data information can be stored using the internal storage latches. The latch-enable (LE1B , LE2B , LEA1B , and LEA2B) inputs are used to control data storage. When the latch-enable input is high, the latch is transparent. When the latch-enable input goes low, the data present at the inputs is latched and remains latched until the latch-enable input is returned high.

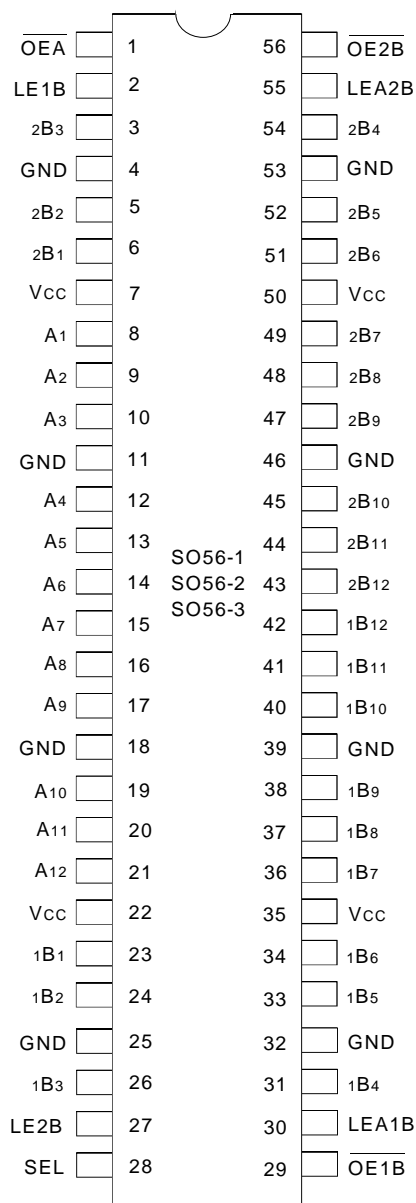
The ALVCHR16260 has series resistors in the device output structure which will significantly reduce line noise when used with light loads. This driver has been designed to drive $\pm 12\text{mA}$ at the designated threshold levels.

The ALVCHR16260 has "bus-hold" which retains the inputs' last state whenever the input goes to a high impedance. This prevents floating inputs and eliminates the need for pull-up/down resistors.

Functional Block Diagram



PIN CONFIGURATION



SSOP/
TSSOP/TVSOP
TOP VIEW

ABSOLUTE MAXIMUM RATING (1)

| Symbol | Description | Max. | Unit |
|------------------------------------|--|-------------------------|------|
| $V_{TERM}^{(2)}$ | Terminal Voltage with Respect to GND | - 0.5 to + 4.6 | V |
| $V_{TERM}^{(3)}$ | Terminal Voltage with Respect to GND | - 0.5 to $V_{CC} + 0.5$ | V |
| TSTG | Storage Temperature | - 65 to + 150 | °C |
| I _{OUT} | DC Output Current | - 50 to + 50 | mA |
| I _{IK} | Continuous Clamp Current, $V_I < 0$ or $V_I > V_{CC}$ | ± 50 | mA |
| I _{OK} | Continuous Clamp Current, $V_O < 0$ | - 50 | mA |
| I _{CC} I _{SS} | Continuous Current through each V _{CC} or GND | ± 100 | mA |

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NOTES:

- Stresses greater than those listed under ABSOLUTE MAXIMUM RATINGS may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect reliability.
- V_{CC} terminals.
- All terminals except V_{CC}.

CAPACITANCE (T_A = +25°C, f = 1.0MHz)

| Symbol | Parameter(1) | Conditions | Typ. | Max. | Unit |
|------------------|----------------------|-----------------------|------|------|------|
| C _{IN} | Input Capacitance | V _{IN} = 0V | 5 | 7 | pF |
| C _{OUT} | Output Capacitance | V _{OUT} = 0V | 7 | 9 | pF |
| C _{I/O} | I/O Port Capacitance | V _{IN} = 0V | 7 | 9 | pF |

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NOTE:

- As applicable to the device type.

PIN DESCRIPTION

| Pin Names | I/O | Description |
|-----------|-----|---|
| Ax(1:12) | I/O | Bidirectional Data Port A. Usually connected to the CPU's Address/Data bus. ⁽¹⁾ |
| 1Bx(1:12) | I/O | Bidirectional Data Port 1B. Connected to the even path or even bank of memory. ⁽¹⁾ |
| 2Bx(1:12) | I/O | Bidirectional Data Port 2B. Connected to the odd path or odd bank of memory. ⁽¹⁾ |
| LEA1B | I | Latch Enable Input for A-1B latch. The latch is open when LEA1B is HIGH. Data from the A port is latched on the HIGH to LOW transition of LEA1B. |
| LEA2B | I | Latch Enable Input for A-2B latch. The latch is open when LEA2B is HIGH. Data from the A port is latched on the HIGH to LOW transition of LEA2B. |
| LE1B | I | Latch Enable Input for 1B-A latch. The latch is open when LE1B is HIGH. Data from the 1B port is latched on the HIGH to LOW transition of LE1B. |
| LE2B | I | Latch Enable Input for 2B-A latch. The latch is open when LE2B is HIGH. Data from the 2B port is latched on the HIGH to LOW transition of LE2B. |
| SEL | I | 1B or 2B Path Selection. When HIGH, SEL enables data transfer from 1B port to A port. When LOW, SEL enables data transfer from 2B port to A port. |
| OEA | I | Output Enable for A port (Active LOW) |
| OE1B | I | Output Enable for 1B port (Active LOW) |
| OE2B | I | Output Enable for 2B port (Active LOW) |

NOTE:

1. These pins have "Bus-Hold." All other pins are standard inputs, outputs, or I/Os.

FUNCTION TABLES ⁽¹⁾

B TO A ($\overline{OEB} = H$)

| Inputs | | | | | | Outputs |
|--------|-----|-----|------|------|------------------|-------------------------------|
| 1Bx | 2Bx | SEL | LE1B | LE2B | \overline{OEA} | Ax |
| H | X | H | H | X | L | H |
| L | X | H | H | X | L | L |
| X | X | H | L | X | L | A ₀ ⁽²⁾ |
| X | H | L | X | H | L | H |
| X | L | L | X | H | L | L |
| X | X | L | X | L | L | A ₀ ⁽²⁾ |
| X | X | X | X | X | H | Z |

NOTES:

1. H = HIGH Voltage Level
L = LOW Voltage Level
X = Don't Care
Z = High-Impedance
2. Output level before the indicated steady-state input conditions were established.

A TO B ($\overline{OEB} = H$)

| Inputs | | | | | Outputs | |
|--------|-------|-------|-------------------|-------------------|--------------------------------|--------------------------------|
| Ax | LEA1B | LEA2B | $\overline{OE1B}$ | $\overline{OE2B}$ | 1Bx | 2Bx |
| H | H | H | L | L | H | H |
| L | H | H | L | L | L | L |
| H | H | L | L | L | H | 2B ₀ ⁽²⁾ |
| L | H | L | L | L | L | 2B ₀ ⁽²⁾ |
| H | L | H | L | L | 1B ₀ ⁽²⁾ | H |
| L | L | H | L | L | 1B ₀ ⁽²⁾ | L |
| X | L | L | L | L | 1B ₀ ⁽²⁾ | 2B ₀ ⁽²⁾ |
| X | X | X | H | H | Z | Z |
| X | X | X | L | H | Active | Z |
| X | X | X | H | L | Z | Active |
| X | X | X | L | L | Active | Active |

DC ELECTRICAL CHARACTERISTICS OVER OPERATING RANGE

Following Conditions Apply Unless Otherwise Specified:

Operating Condition: TA = – 40°C to +85°C

| Symbol | Parameter | Test Conditions | | Min. | Typ. ⁽¹⁾ | Max. | Unit |
|----------------------|--|--|----------|------|---------------------|-------|------|
| VIH | Input HIGH Voltage Level | VCC = 2.3V to 2.7V | | 1.7 | — | — | V |
| | | VCC = 2.7V to 3.6V | | 2 | — | — | |
| VIL | Input LOW Voltage Level | VCC = 2.3V to 2.7V | | — | — | 0.7 | V |
| | | VCC = 2.7V to 3.6V | | — | — | 0.8 | |
| IiH | Input HIGH Current | VCC = 3.6V | Vi = VCC | — | — | ± 5 | μA |
| IiL | Input LOW Current | VCC = 3.6V | Vi = GND | — | — | ± 5 | |
| IozH | High Impedance Output Current (3-State Output pins) | VCC = 3.6V | Vo = VCC | — | — | ± 10 | μA |
| IozL | | | Vo = GND | — | — | ± 10 | μA |
| Vik | Clamp Diode Voltage | VCC = 2.3V, IIN = – 18mA | | — | – 0.7 | – 1.2 | V |
| VH | Input Hysteresis | VCC = 3.3V | | — | 100 | — | mV |
| ICCL ICCH ICCZ | Quiescent Power Supply Current | VCC = 3.6V VIN = GND or VCC | | — | 0.1 | 40 | μA |
| ΔICC | Quiescent Power Supply Current Variation | One input at VCC – 0.6V, other inputs at VCC or GND | | — | — | 750 | μA |

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NOTE:

1. Typical values are at VCC = 3.3V, +25°C ambient.

BUS-HOLD CHARACTERISTICS

| Symbol | Parameter ⁽¹⁾ | Test Conditions | | Min. | Typ. ⁽²⁾ | Max. | Unit |
|----------------|----------------------------------|-----------------|----------------|------|---------------------|-------|------|
| IBHH IBHL | Bus-Hold Input Sustain Current | VCC = 3.0V | Vi = 2.0V | – 75 | — | — | μA |
| | | | Vi = 0.8V | 75 | — | — | |
| IBHH IBHL | Bus-Hold Input Sustain Current | VCC = 2.3V | Vi = 1.7V | – 45 | — | — | μA |
| | | | Vi = 0.7V | 45 | — | — | |
| IBHHO IBHLO | Bus-Hold Input Overdrive Current | VCC = 3.6V | Vi = 0 to 3.6V | — | — | ± 500 | μA |

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NOTES:

1. Pins with Bus-hold are identified in the pin description.
2. Typical values are at VCC = 3.3V, +25°C ambient.

OUTPUT DRIVE CHARACTERISTICS

| Symbol | Parameter | Test Conditions ⁽¹⁾ | | Min. | Max. | Unit |
|--------|---------------------|--------------------------------|---------------|-----------|------|------|
| VOH | Output HIGH Voltage | VCC = 2.3V to 3.6V | IOH = - 0.1mA | VCC - 0.2 | — | V |
| | | VCC = 2.3V | IOH = - 4mA | 1.9 | — | |
| | | | IOH = - 6mA | 1.7 | — | |
| | | VCC = 2.7V | IOH = - 4mA | 2.2 | — | |
| | | | IOH = - 8mA | 2 | — | |
| | | VCC = 3.0V | IOH = - 6mA | 2.4 | — | |
| | | | IOH = - 12mA | 2 | — | |
| VOL | Output LOW Voltage | VCC = 2.3V to 3.6V | IOL = 0.1mA | — | 0.2 | V |
| | | VCC = 2.3V | IOL = 4mA | — | 0.4 | |
| | | | IOL = 6mA | — | 0.55 | |
| | | VCC = 2.7V | IOL = 4mA | — | 0.4 | |
| | | | IOL = 8mA | — | 0.6 | |
| | | VCC = 3.0V | IOL = 6mA | — | 0.55 | |
| | | | IOL = 12mA | — | 0.8 | |

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NOTE:

1. VIH and VIL must be within the min. or max. range shown in the DC ELECTRICAL CHARACTERISTICS OVER OPERATING RANGE table for the appropriate VCC range. TA = - 40°C to + 85°C.

OPERATING CHARACTERISTICS, TA = 25°C

| Symbol | Parameter | Test Conditions | VCC = 2.5V ± 0.2V | VCC = 3.3V ± 0.3V | Unit |
|--------|---|---------------------|-------------------|-------------------|------|
| | | | Typical | Typical | |
| CPD | Power Dissipation Capacitance Outputs enabled | CL = 0pF, f = 10Mhz | 37 | 41 | pF |
| CPD | Power Dissipation Capacitance Outputs disabled | | 4 | 7 | pF |

SWITCHING CHARACTERISTICS⁽¹⁾

| Symbol | Parameter | V _{CC} = 2.5V ± 0.2V | | V _{CC} = 2.7V | | V _{CC} = 3.3V ± 0.3V | | Unit |
|--------------------------------------|---|-------------------------------|------|------------------------|------|-------------------------------|------|------|
| | | Min. | Max. | Min. | Max. | Min. | Max. | |
| t _{PLH} t _{PHL} | Propagation Delay Ax to 1Bx or Ax to 2Bx | 1 | 5.9 | — | 5.8 | 1.2 | 4.9 | ns |
| t _{PLH} t _{PHL} | Propagation Delay 1Bx to Ax or 2Bx to Ax | 1 | 5.9 | — | 5.8 | 1.2 | 4.9 | ns |
| t _{PLH} t _{PHL} | Propagation Delay LExB to Ax | 1 | 6.1 | — | 5.9 | 1 | 5 | ns |
| t _{PLH} t _{PHL} | Propagation Delay LEA1B to 1Bx or LEA2B to 2Bx | 1 | 6.1 | — | 5.9 | 1 | 5 | ns |
| t _{PLH} t _{PHL} | Propagation Delay SEL to Ax | 1 | 7.4 | — | 7.1 | 1.1 | 6.1 | ns |
| t _{PZH} t _{PZL} | Output Enable Time OEA to Ax, OE1B to 1Bx, or OE2B to 2Bx | 1 | 7.2 | — | 7.1 | 1 | 6 | ns |
| t _{PHZ} t _{PLZ} | Output Disable Time OEA to Ax, OE1B to 1Bx, or OE2B to 2Bx | 1 | 6.2 | — | 5.5 | 1.3 | 5.1 | ns |
| t _{SU} | Setup Time, data before LE1B, LE2B, LEA1B, LEA2B | 1.4 | — | 1.1 | — | 1.1 | — | ns |
| t _H | Hold Time, data after LE1B, LE2B, LEA1B, LEA2B | 1.6 | — | 1.9 | — | 1.5 | — | ns |
| t _W | Pulse Width, LE1B, LE2B, LEA1B, or LEA2B HIGH | 3.3 | — | 3.3 | — | 3.3 | — | ns |
| t _{SK(0)} | Output Skew ⁽²⁾ | — | — | — | — | — | 500 | ps |

NOTES:

1. See test circuits and waveforms. T_A = – 40°C to + 85°C.
2. Skew between any two outputs of the same package and switching in the same direction.

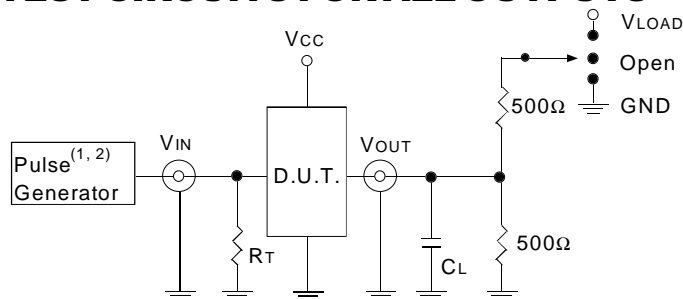
TEST CIRCUITS AND WAVEFORMS

TEST CONDITIONS

| Symbol | V _{CC} (1)= 3.3V±0.3V | V _{CC} (1)= 2.7V | V _{CC} (2)= 2.5V±0.2V | Unit |
|-------------------|--------------------------------|---------------------------|--------------------------------|------|
| V _{LOAD} | 6 | 6 | 2 x V _{CC} | V |
| V _{IH} | 2.7 | 2.7 | V _{CC} | V |
| V _T | 1.5 | 1.5 | V _{CC} / 2 | V |
| V _{LZ} | 300 | 300 | 150 | mV |
| V _{HZ} | 300 | 300 | 150 | mV |
| C _L | 50 | 50 | 30 | pF |

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TEST CIRCUITS FOR ALL OUTPUTS



ALVC Link

DEFINITIONS:

C_L= Load capacitance: includes jig and probe capacitance.

R_T= Termination resistance: should be equal to Z_{OUT} of the Pulse Generator.

NOTES:

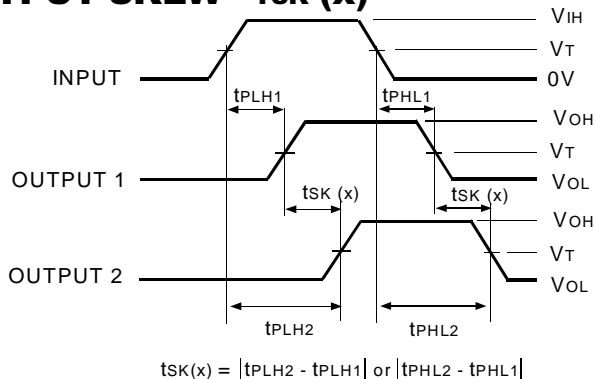
1. Pulse Generator for All Pulses: Rate ≤ 10MHz; t_r ≤ 2.5ns; t_r ≤ 2.5ns.
2. Pulse Generator for All Pulses: Rate ≤ 10MHz; t_r ≤ 2ns; t_r ≤ 2ns.

SWITCH POSITION

| Test | Switch |
|---|-------------------|
| Open Drain Disable Low Enable Low | V _{LOAD} |
| Disable High Enable High | GND |
| All Other tests | Open |

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OUTPUT SKEW - t_{SK} (x)

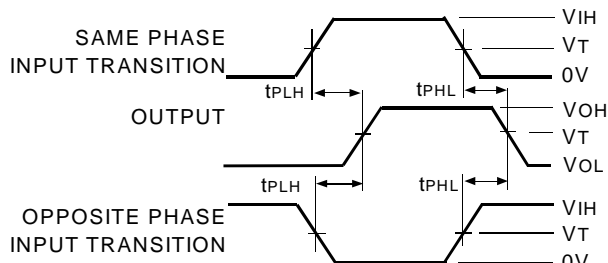


ALVC Link

NOTES:

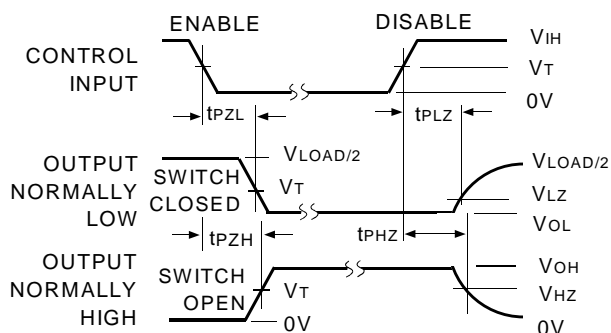
1. For t_{SK}(o) OUTPUT1 and OUTPUT2 are any two outputs.
2. For t_{SK}(b) OUTPUT1 and OUTPUT2 are in the same bank.

PROPAGATION DELAY



ALVC Link

ENABLE AND DISABLE TIMES

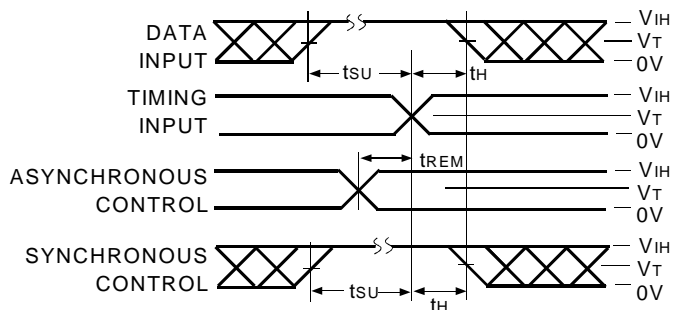


ALVC Link

NOTE:

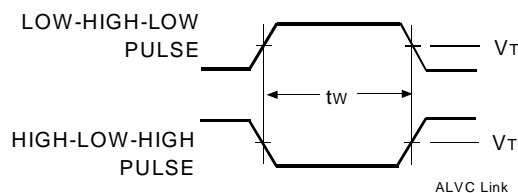
1. Diagram shown for input Control Enable-LOW and input Control Disable-HIGH.

SET-UP, HOLD, AND RELEASE TIMES



ALVC Link

PULSE WIDTH



ALVC Link

ORDERING INFORMATION

| IDT | XX | ALVC | X | XX | XXX | XX | |
|-------------|----------|--------|-------------|---------|-----|--|--|
| Temp. Range | Bus-Hold | Family | Device Type | Package | | | |
| | | | | | PV | Shrink Small Outline Package (SO56-1) | |
| | | | | | PA | Thin Shrink Small Outline Package (SO56-2) | |
| | | | | | PF | Thin Very Small Outline Package (SO56-3) | |
| | | | | 260 | | 12-Bit to 24-Bit Multiplexed D-Type Latch with 3-State Outputs | |
| | | | | R16 | | Double-Density with Resistors, $\pm 12\text{mA}$ | |
| | | | | H | | Bus-Hold | |
| | | | | 74 | | -40°C to $+85^{\circ}\text{C}$ | |



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