



3.3V CMOS 36-BIT UNIVERSAL BUS TRANS- CEIVER WITH 3-STATE OUTPUTS AND BUS-HOLD

IDT74ALVCH32501

FEATURES:

- 0.5 MICRON CMOS Technology
- Typical $t_{sk(o)}$ (Output Skew) < 250ps
- ESD > 2000V per MIL-STD-883, Method 3015;
> 200V using machine model (C = 200pF, R = 0)
- 0.8mm pitch LFBGA package, 114 balls
- Extended commercial range of -40°C to $+85^{\circ}\text{C}$
- $V_{CC} = 3.3\text{V} \pm 0.3\text{V}$, Normal Range
- $V_{CC} = 2.7\text{V}$ to 3.6V , Extended Range
- $V_{CC} = 2.5\text{V} \pm 0.2\text{V}$
- CMOS power levels ($0.4\mu\text{W}$ typ. static)
- Rail-to-Rail output swing for increased noise margin

Drive Features for ALVCH32501:

- High Output Drivers: $\pm 24\text{mA}$
- Suitable for heavy loads

APPLICATIONS:

- 3.3V High Speed Systems
- 3.3V and lower voltage computing systems

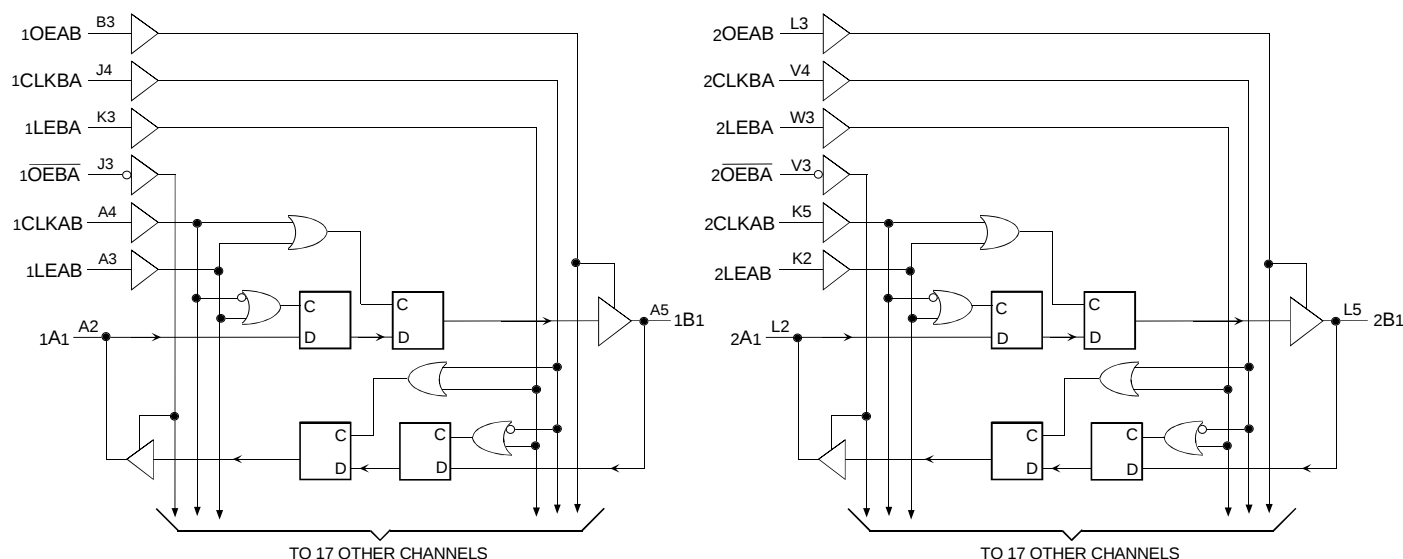
DESCRIPTION:

This 36-bit universal bus transceiver is built using advanced dual metal CMOS technology. The ALVCH32501 combines D-type latches and D-type flip-flops to allow data flow in transparent latched and clocked modes. Data flow in each direction is controlled by output-enable (OEAB and $\overline{\text{OEBA}}$), latch enable (LEAB and LEBA), and clock (CLKAB and CLKBA) inputs. For A-to-B data flow, the device operates in transparent mode when LEAB is high. When LEAB is low, the A data is latched if CLKAB is held at a HIGH or low logic level. If LEAB is low, the A bus data is stored in the latch/flip-flop on the low-to-high transition of CLKAB. OEAB performs the output enable function on the B port. Data flow from B port to A port is similar but requires using $\overline{\text{OEBA}}$, LEBA and CLKBA. Flow-through organization of signal pins simplifies layout. All inputs are designed with hysteresis for improved noise margin.

This ALVCH32501 has been designed with a $\pm 24\text{mA}$ output driver. This driver is capable of driving a moderate to heavy load while maintaining speed performance.

The ALVCH32501 has "bus-hold" which retains the inputs' last state whenever the input goes to a high impedance. This prevents floating inputs and eliminates the need for pull-up/down resistors.

FUNCTIONAL BLOCK DIAGRAM



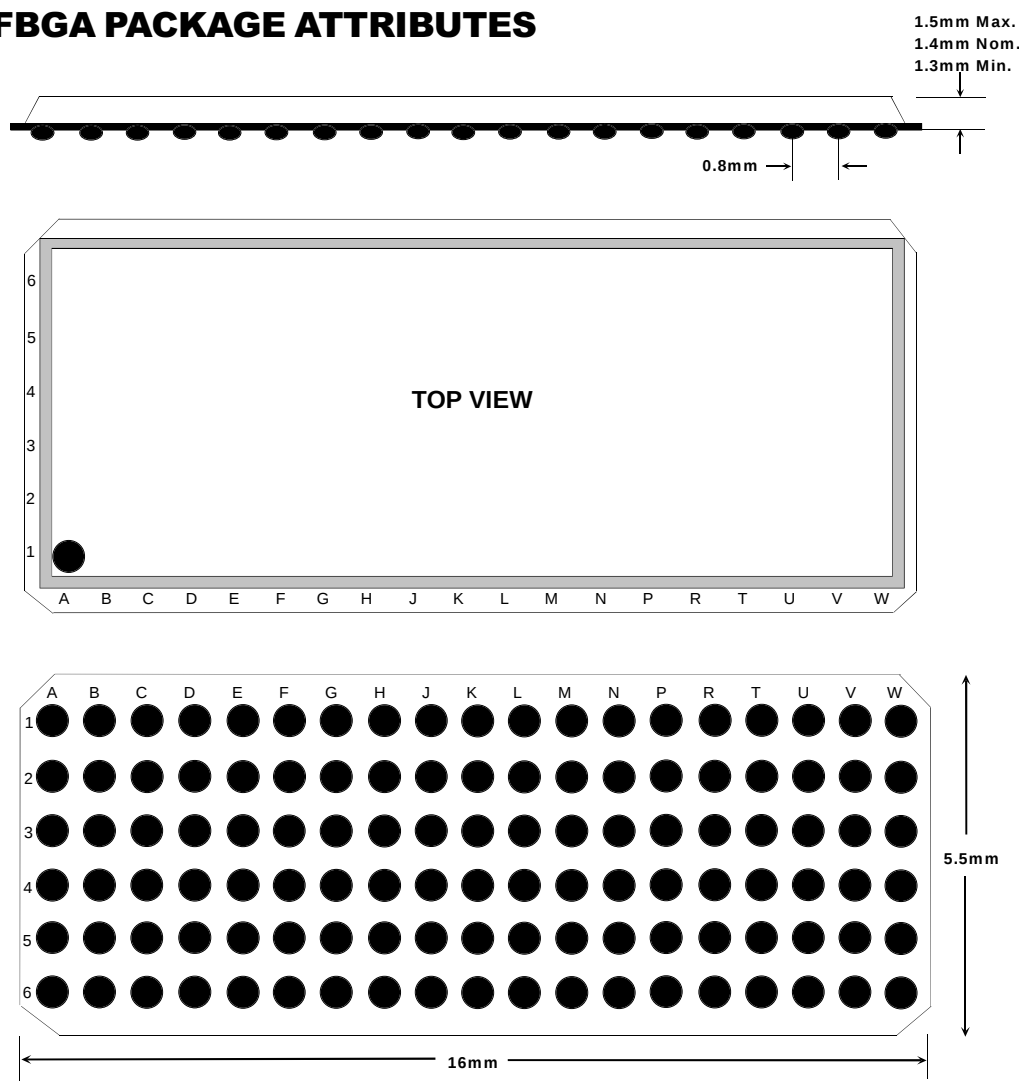
PIN CONFIGURATION

6	1B2	1B4	1B6	1B8	1B10	1B12	1B14	1B15	1B17	NC	2B2	2B4	2B6	2B8	2B10	2B12	2B14	2B15	2B17
5	1B1	1B3	1B5	1B7	1B9	1B11	1B13	1B16	1B18	2CLKAB	2B1	2B3	2B5	2B7	2B9	2B11	2B13	2B16	2B18
4	1CLKAB	GND	GND	Vcc	GND	GND	Vcc	GND	1CLKBA	GND	GND	GND	Vcc	GND	GND	Vcc	GND	2CLKBA	GND
3	1LEAB	1OEAB	GND	Vcc	GND	GND	Vcc	GND	1OEBA	1LEBA	2OEAB	GND	Vcc	GND	GND	Vcc	GND	2OEBA	2LEBA
2	1A1	1A3	1A5	1A7	1A9	1A11	1A13	1A16	1A18	2LEAB	2A1	2A3	2A5	2A7	2A9	2A11	2A13	2A16	2A18
1	1A2	1A4	1A6	1A8	1A10	1A12	1A14	1A15	1A17	NC	2A2	2A4	2A6	2A8	2A10	2A12	2A14	2A15	2A17
	A	B	C	D	E	F	G	H	J	K	L	M	N	P	R	T	U	V	W

32501

LFBGA
TOP VIEW

114 BALL LFBGA PACKAGE ATTRIBUTES



ABSOLUTE MAXIMUM RATING (1)

Symbol	Description	Max.	Unit
V _{TERM} (2)	Terminal Voltage with Respect to GND	– 0.5 to + 4.6	V
V _{TERM} (3)	Terminal Voltage with Respect to GND	– 0.5 to V _{CC} + 0.5	V
T _{STG}	Storage Temperature	– 65 to + 150	°C
I _{OUT}	DC Output Current	– 50 to + 50	mA
I _{IK}	Continuous Clamp Current, V _I < 0 or V _I > V _{CC}	± 50	mA
I _{OK}	Continuous Clamp Current, V _O < 0	– 50	mA
I _{CC} I _{SS}	Continuous Current through each V _{CC} or GND	±100	mA

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NOTES:

- Stresses greater than those listed under ABSOLUTE MAXIMUM RATINGS may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect reliability.
- V_{CC} terminals.
- All terminals except V_{CC}.

PIN DESCRIPTION

Pin Names	Description
OEAB	A-to-B Output Enable Input
$\overline{\text{OEBA}}$	B-to-A Output Enable Input (Active LOW)
LEAB	A-to-B Latch Enable Input
LEBA	B-to-A Latch Enable Input
CLKAB	A-to-B Clock Input
CLKBA	B-to-A Clock Input
xAx	A-to-B Data Inputs or B-to-A 3-State Outputs(1)
xBx	B-to-A Data Inputs or A-to-B 3-State Outputs(1)

NOTE:

- These pins have "Bus-Hold." All other pins are standard inputs, outputs, or I/Os.

CAPACITANCE (T_A = +25°C, f = 1.0MHz)

Symbol	Parameter(1)	Conditions	Typ.	Max.	Unit
C _{IN}	Input Capacitance	V _{IN} = 0V	5	7	pF
C _{OUT}	Output Capacitance	V _{OUT} = 0V	7	9	pF
C _{I/O}	I/O Port Capacitance	V _{IN} = 0V	7	9	pF

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NOTE:

- As applicable to the device type.

FUNCTION TABLE (1,2)

Inputs				Outputs
OEAB	LEAB	CLKAB	xAx	xBx
L	X	X	X	Z
H	H	X	L	L
H	H	X	H	H
H	L	↑	L	L
H	L	↑	H	H
H	L	L	X	B ₀ (3)
H	L	H	X	B ₀ (4)

NOTES:

- A-to-B data flow is shown. B-to-A data flow is similar but uses OEBA, LEBA, and CLKBA.
- H = HIGH Voltage Level
L = LOW Voltage Level
X = Don't Care
Z = High Impedance
↑ = LOW-to-HIGH Transition
- Output level before the indicated steady-state input conditions were established.
- Output level before the indicated steady-state input conditions were established, provided that CLKAB was high before LEAB went low.

DC ELECTRICAL CHARACTERISTICS OVER OPERATING RANGE

Following Conditions Apply Unless Otherwise Specified:

Operating Condition: TA = – 40°C to +85°C

Symbol	Parameter	Test Conditions		Min.	Typ. ⁽¹⁾	Max.	Unit
V _{IH}	Input HIGH Voltage Level	V _{CC} = 2.3V to 2.7V		1.7	—	—	V
		V _{CC} = 2.7V to 3.6V		2	—	—	
V _{IL}	Input LOW Voltage Level	V _{CC} = 2.3V to 2.7V		—	—	0.7	V
		V _{CC} = 2.7V to 3.6V		—	—	0.8	
I _{IH}	Input HIGH Current	V _{CC} = 3.6V	V _I = V _{CC}	—	—	± 5	μA
I _{IL}	Input LOW Current	V _{CC} = 3.6V	V _I = GND	—	—	± 5	
I _{OZH}	High Impedance Output Current (3-State Output pins)	V _{CC} = 3.6V	V _O = V _{CC}	—	—	± 10	μA
I _{OZL}			V _O = GND	—	—	± 10	μA
V _{IK}	Clamp Diode Voltage	V _{CC} = 2.3V, I _{IN} = – 18mA		—	– 0.7	– 1.2	V
V _H	Input Hysteresis	V _{CC} = 3.3V		—	100	—	mV
I _{CCL} I _{CCH} I _{CCZ}	Quiescent Power Supply Current	V _{CC} = 3.6V V _{IN} = GND or V _{CC}		—	0.1	40	μA
ΔI _{CC}	Quiescent Power Supply Current Variation	One input at V _{CC} – 0.6V, other inputs at V _{CC} or GND		—	—	750	μA

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NOTE:

1. Typical values are at VCC = 3.3V, +25°C ambient.

BUS-HOLD CHARACTERISTICS

Symbol	Parameter ⁽¹⁾	Test Conditions		Min.	Typ. ⁽²⁾	Max.	Unit
IBHH IBHL	Bus-Hold Input Sustain Current	VCC = 3.0V	Vi = 2.0V	– 75	—	—	μA
			Vi = 0.8V	75	—	—	
IBHH IBHL	Bus-Hold Input Sustain Current	VCC = 2.3V	Vi = 1.7V	– 45	—	—	μA
			Vi = 0.7V	45	—	—	
IBHHO IBHLO	Bus-Hold Input Overdrive Current	VCC = 3.6V	Vi = 0 to 3.6V	—	—	± 500	μA

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NOTES:

1. Pins with Bus-hold are identified in the pin description.
2. Typical values are at VCC = 3.3V, +25°C ambient.

OUTPUT DRIVE CHARACTERISTICS

Symbol	Parameter	Test Conditions ⁽¹⁾		Min.	Max.	Unit
VOH	Output HIGH Voltage	VCC = 2.3V to 3.6V	IOH = – 0.1mA	VCC – 0.2	—	V
		VCC = 2.3V	IOH = – 6mA	2	—	
		VCC = 2.3V	IOH = – 12mA	1.7	—	
		VCC = 2.7V		2.2	—	
		VCC = 3.0V		2.4	—	
		VCC = 3.0V	IOH = – 24mA	2	—	
VOL	Output LOW Voltage	VCC = 2.3V to 3.6V	IOL = 0.1mA	—	0.2	V
		VCC = 2.3V	IOL = 6mA	—	0.4	
			IOL = 12mA	—	0.7	
		VCC = 2.7V	IOL = 12mA	—	0.4	
		VCC = 3.0V	IOL = 24mA	—	0.55	

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NOTE:

1. VIH and VIL must be within the min. or max. range shown in the DC ELECTRICAL CHARACTERISTICS OVER OPERATING RANGE table for the appropriate VCC range. TA = – 40°C to + 85°C.

OPERATING CHARACTERISTICS, TA = 25°C

Symbol	Parameter	Test Conditions	VCC = 2.5V ± 0.2V	VCC = 3.3V ± 0.3V	Unit
			Typical	Typical	
CPD	Power Dissipation Capacitance Outputs enabled	CL = 0pF, f = 10Mhz	88	108	pF
CPD	Power Dissipation Capacitance Outputs disabled		12	12	pF

SWITCHING CHARACTERISTICS⁽¹⁾

Symbol	Parameter	V _{CC} = 2.5V ± 0.2V		V _{CC} = 2.7V		V _{CC} = 3.3V ± 0.3V		Unit
		Min.	Max.	Min.	Max.	Min.	Max.	
t _{PLH} t _{PHL}	Propagation Delay xAx to xBx or xBx to xAx	1	4.8	—	4.5	1	3.9	ns
t _{PLH} t _{PHL}	Propagation Delay LE to xAx or xBx	1.1	5.7	—	5.3	1.3	4.6	ns
t _{PLH} t _{PHL}	Propagation Delay CLK to xAx or xBx	1.2	6.1	—	5.6	1.4	4.9	ns
t _{PZH} t _{PZL}	Output Enable Time $\overline{\text{OEBA}}$ to xAx	1.3	6.3	—	6	1.1	5	ns
t _{PZH} t _{PZL}	Output Enable Time OEAB to xBx	1	5.8	—	5.3	1	4.6	ns
t _{PHZ} t _{PLZ}	Output Disable Time $\overline{\text{OEBA}}$ to xAx	1.3	5.3	—	4.6	1.3	4.2	ns
t _{PHZ} t _{PLZ}	Output Disable Time OEAB to xBx	1.5	6.2	—	5.7	1.4	5	ns
t _{SU}	Setup Time, data before CLK↑	2.2	—	2.1	—	1.7	—	ns
t _H	Hold Time, data after CLK↑	0.6	—	0.6	—	0.7	—	ns
t _{SU}	Setup Time, data before LE↓	CLK HIGH	1.9	—	1.6	—	1.5	ns
		CLK LOW	1.3	—	1.1	—	1	ns
t _H	Hold Time, data after LE↓, CLK HIGH or LOW	1.4	—	1.7	—	1.4	—	ns
t _w	Pulse Width, LE HIGH	3.3	—	3.3	—	3.3	—	ns
t _w	Pulse Width, CLK HIGH or LOW	3.3	—	3.3	—	3.3	—	ns
t _{SK(0)}	Output Skew ⁽²⁾	—	—	—	—	—	500	ps

NOTES:

- See test circuits and waveforms. T_A = – 40°C to + 85°C.
- Skew between any two outputs of the same package and switching in the same direction.

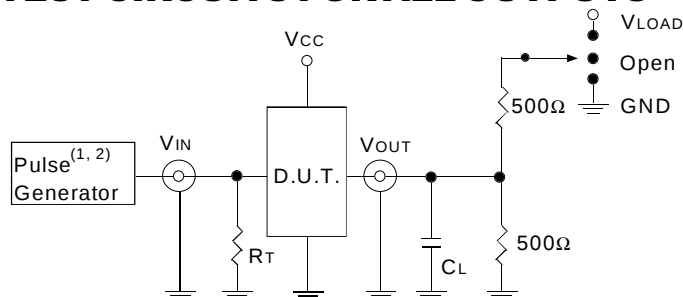
TEST CIRCUITS AND WAVEFORMS

TEST CONDITIONS

Symbol	V _{CC} (1)= 3.3V±0.3V	V _{CC} (1)= 2.7V	V _{CC} (2)= 2.5V±0.2V	Unit
V _{LOAD}	6	6	2 x V _{CC}	V
V _{IH}	2.7	2.7	V _{CC}	V
V _T	1.5	1.5	V _{CC} / 2	V
V _{LZ}	300	300	150	mV
V _{HZ}	300	300	150	mV
C _L	50	50	30	pF

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TEST CIRCUITS FOR ALL OUTPUTS



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DEFINITIONS:

C_L= Load capacitance: includes jig and probe capacitance.

R_T= Termination resistance: should be equal to Z_{OUT} of the Pulse Generator.

NOTES:

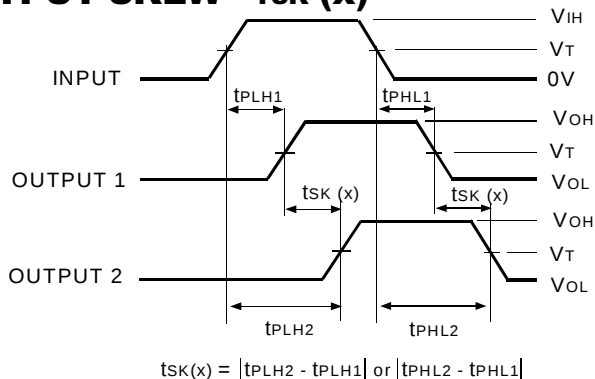
1. Pulse Generator for All Pulses: Rate ≤ 10MHz; t_r ≤ 2.5ns; t_r ≤ 2.5ns.
2. Pulse Generator for All Pulses: Rate ≤ 10MHz; t_r ≤ 2ns; t_r ≤ 2ns.

SWITCH POSITION

Test	Switch
Open Drain Disable Low Enable Low	V _{LOAD}
Disable High Enable High	GND
All Other tests	Open

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OUTPUT SKEW - τ_{SK} (x)

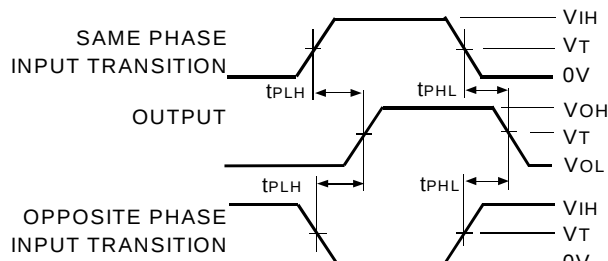


ALVC Link

NOTES:

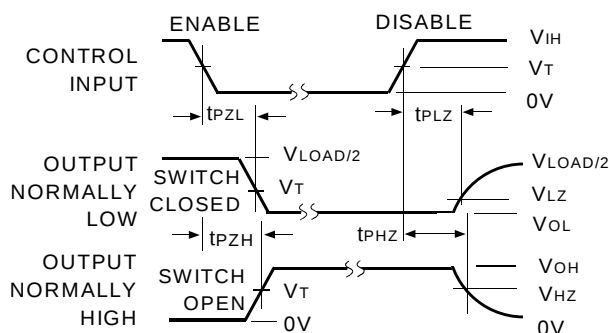
1. For τ_{SK}(o) OUTPUT1 and OUTPUT2 are any two outputs.
2. For τ_{SK}(b) OUTPUT1 and OUTPUT2 are in the same bank.

PROPAGATION DELAY



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ENABLE AND DISABLE TIMES

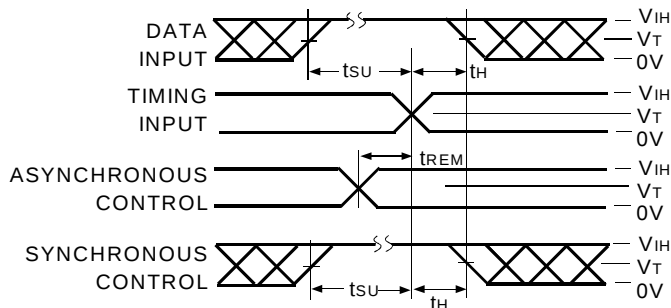


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NOTE:

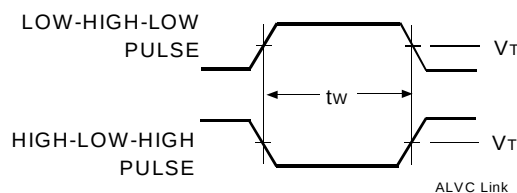
1. Diagram shown for input Control Enable-LOW and input Control Disable-HIGH.

SET-UP, HOLD, AND RELEASE TIMES



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PULSE WIDTH



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ORDERING INFORMATION

IDT	XX	ALVC	X	XX	XXXX	XX	
Temp. Range		Bus-Hold	Family	Device Type	Package		
					BF		Low-Profile Fine Pitch Ball Grid Array (BF114-1)
					501		36-Bit Universal Bus Transceiver with 3-State Outputs
					32		32-Bit Bus Density with Resistors, $\pm 24\text{mA}$
					H		Bus-Hold
					74		-40°C to $+85^{\circ}\text{C}$



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