



3.3V CMOS 12-BIT UNIVERSAL BUS DRIVER WITH PARITY CHECKER, DUAL 3-STATE OUTPUTS AND BUS-HOLD

IDT74ALVCH16903

FEATURES:

- 0.5 MICRON CMOS Technology
- Typical $t_{sk(0)}$ (Output Skew) < 250ps
- ESD > 2000V per MIL-STD-883, Method 3015;
> 200V using machine model (C = 200pF, R = 0)
- 0.635mm pitch SSOP, 0.50mm pitch TSSOP,
and 0.40mm pitch TVSOP packages
- Extended commercial range of -40°C to $+85^{\circ}\text{C}$
- $V_{cc} = 3.3\text{V} \pm 0.3\text{V}$, Normal Range
- $V_{cc} = 2.7\text{V}$ to 3.6V , Extended Range
- $V_{cc} = 2.5\text{V} \pm 0.2\text{V}$
- CMOS power levels (0.4 μW typ. static)
- Rail-to-Rail output swing for increased noise margin

Drive Features for ALVCH16903:

- High Output Drivers: $\pm 24\text{mA}$
- Suitable for heavy loads

APPLICATIONS:

- 3.3V High Speed Systems
- 3.3V and lower voltage computing systems

ABSOLUTE MAXIMUM RATING (1)

Symbol	Description	Max.	Unit
$V_{TERM(2)}$	Terminal Voltage with Respect to GND	-0.5 to $+4.6$	V
$V_{TERM(3)}$	Terminal Voltage with Respect to GND	-0.5 to $V_{cc} + 0.5$	V
TSTG	Storage Temperature	-65 to $+150$	$^{\circ}\text{C}$
IOUT	DC Output Current	-50 to $+50$	mA
I _{IK}	Continuous Clamp Current, $V_I < 0$ or $V_I > V_{cc}$	± 50	mA
I _{OK}	Continuous Clamp Current, $V_O < 0$	-50	mA
I _{CC} I _{SS}	Continuous Current through each V_{cc} or GND	± 100	mA

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NOTES:

1. Stresses greater than those listed under ABSOLUTE MAXIMUM RATINGS may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect reliability.
2. V_{cc} terminals.
3. All terminals except V_{cc} .

DESCRIPTION:

This 12-bit universal bus driver is built using advanced dual metal CMOS technology. This device has dual outputs and can operate as a buffer or an edge-triggered register. In both modes, parity is checked on $\overline{\text{APAR}}$, which arrives one cycle after the data to which it applies. The $\overline{\text{YERR}}$ output, which is produced one cycle after $\overline{\text{APAR}}$, is open drain.

MODE selects one of the two data paths. When MODE is low, the device operates as an edge-triggered register. On the positive transition of the clock (CLK) input and when the clock-enable ($\overline{\text{CLKEN}}$) input is low, data setup at the A inputs is stored in the internal registers. On the positive transition of CLK and when $\overline{\text{CLKEN}}$ is high, only data setup at the 9A-12A inputs is stored in their internal registers. When MODE is high, the device operates as a buffer and data at the A inputs passes directly to the outputs. The 11A/ $\overline{\text{YERREN}}$ serves a dual purpose; it acts as a normal data bit and also enables $\overline{\text{YERR}}$ data to be clocked into the $\overline{\text{YERR}}$ output register.

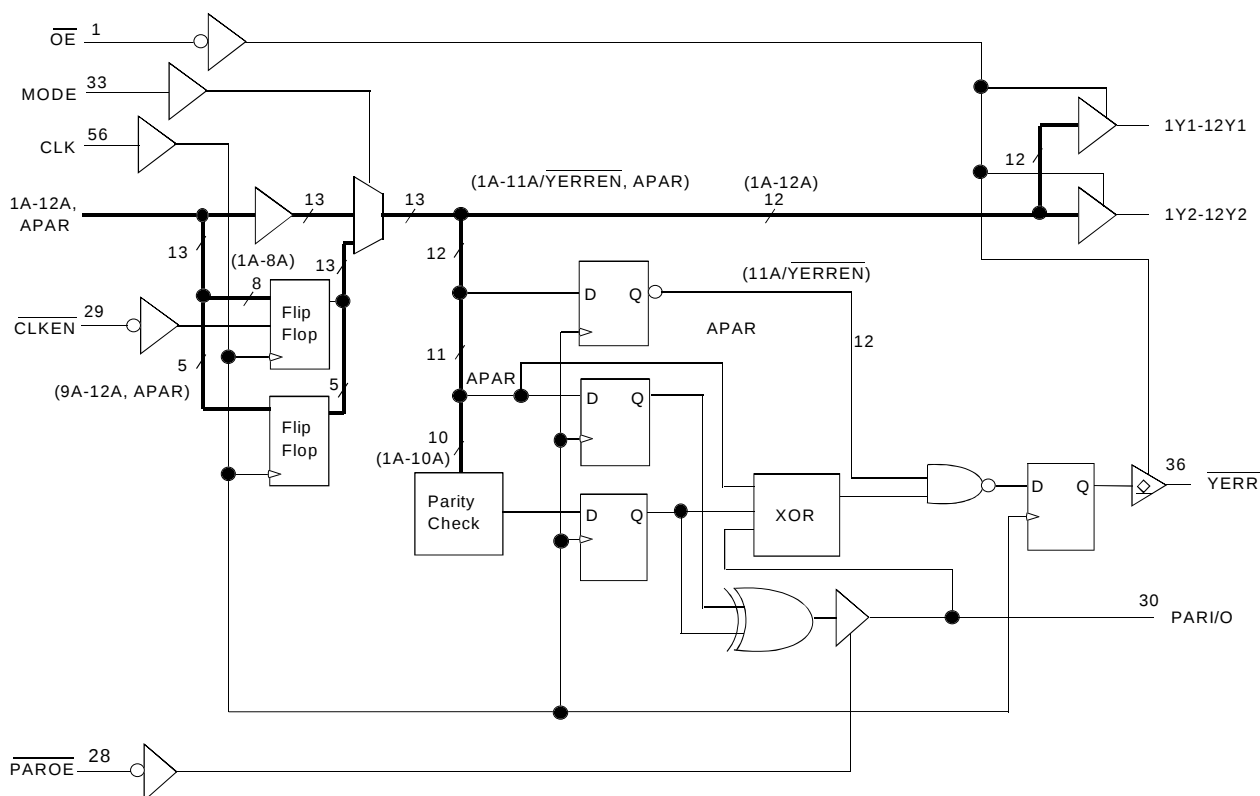
When used as a single device, parity output enable ($\overline{\text{PAROE}}$) must be tied high; when parity input/output ($\overline{\text{PARI/O}}$) is low, even parity is selected and when $\overline{\text{PARI/O}}$ is high, odd parity is selected. When used in pairs and $\overline{\text{PAROE}}$ is low, the parity sum is output on $\overline{\text{PARI/O}}$ for cascading to the second ALVCH16903. When used in pairs and $\overline{\text{PAROE}}$ is high, $\overline{\text{PARI/O}}$ accepts a partial parity sum from the first ALVCH16903.

A buffered output-enable ($\overline{\text{OE}}$) input can be used to place the 24 outputs and $\overline{\text{YERR}}$ in either a normal logic state (high or low logic levels) or a high-impedance state. In the high-impedance state, the outputs neither load nor drive the bus lines significantly. The high-impedance state and increased drive provide the capability to drive bus lines without need for interface or pullup components.

The ALVCH16903 has been designed with a $\pm 24\text{mA}$ output driver. This driver is capable of driving a moderate to heavy load while maintaining speed performance.

The ALVCH16903 has "bus-hold" which retains the inputs' last state whenever the input bus goes to a high-impedance. This prevents floating inputs and eliminates the need for pull-up/down resistors.

FUNCTIONAL BLOCK DIAGRAM



FUNCTION TABLES⁽¹⁾

FUNCTION

Inputs					Outputs	
OE	MODE	CLKEN	CLK	A	1Y _X -18Y _X	9Y _X -12Y _X
L	L	L	↑	H	H	H
L	L	L	↑	L	L	L
L	L	H	↑	H	Y ₀	H
L	L	H	↑	L	Y ₀	L
L	H	X	X	H	H	H
L	H	X	X	L	L	L
H	X	X	X	X	Z	Z

NOTES:

- H = HIGH Voltage Level
L = LOW Voltage Level
Y₀ = Level of Y before the indicated steady-state input conditions were established
X = Don't Care
Z = High-Impedance
↑ = LOW-to-HIGH Transition
- When used as a single device, PAROE must be tied high
- Valid after appropriate number of clock pulses have set internal register

PARITY FUNCTION TABLE

Inputs						Output
OE	PAROE ⁽²⁾	11A/YERREN ⁽³⁾	PARI/O	Σ OF INPUTS 1A-10A= H	APAR	YERR
L	H	L	L	0, 2, 4, 6, 8, 10	L	H
L	H	L	L	1, 3, 5, 7, 9	L	L
L	H	L	L	0, 2, 4, 6, 8, 10	H	L
L	H	L	L	1, 3, 5, 7, 9	H	H
L	H	L	H	0, 2, 4, 6, 8, 10	L	L
L	H	L	H	1, 3, 5, 7, 9	L	H
L	H	L	H	0, 2, 4, 6, 8, 10	H	H
L	H	L	H	1, 3, 5, 7, 9	H	L
H	X	X	X	X	X	H
L	X	H	X	X	X	H

PARI/O FUNCTION TABLE⁽¹⁾

Inputs			Output PARI/O
$\overline{\text{PAROE}}$	Σ OF INPUTS 1A-10A = H	APAR	
L	0, 2, 4, 6, 8, 10	L	L
L	1, 3, 5, 7, 9	L	H
L	0, 2, 4, 6, 8, 10	H	H
L	1, 3, 5, 7, 9	H	L
H	X	X	Z

NOTE:

- This table applies to the first device of a cascaded pair of ALVCH16903 devices.

PIN DESCRIPTION

Pin Names	I/O	Description
1A-12A	I	Data Inputs ⁽¹⁾
1Y1-12Y2	O	3-State Data Outputs
CLK	I	Clock Input
$\overline{\text{CLKEN}}$	I	Clock Enable Input (active low)
MODE	I	Select Pin
$\overline{\text{YERREN}}$	—	Error Signal Output Enable (active low)
$\overline{\text{PAROE}}$	I	Parity Output Enable (active low)
PARI/O	I/O	Parity Input/Output
$\overline{\text{YERR}}$	O	Error Signal (open drain)
$\overline{\text{OE}}$	I	Output Enable Input (active low)
APAR	I	Parity Input

NOTE:

- These pins have "Bus-Hold". All other pins are standard inputs, outputs, or I/Os.

CAPACITANCE ($T_A = +25^\circ\text{C}$, $f = 1.0\text{MHz}$)

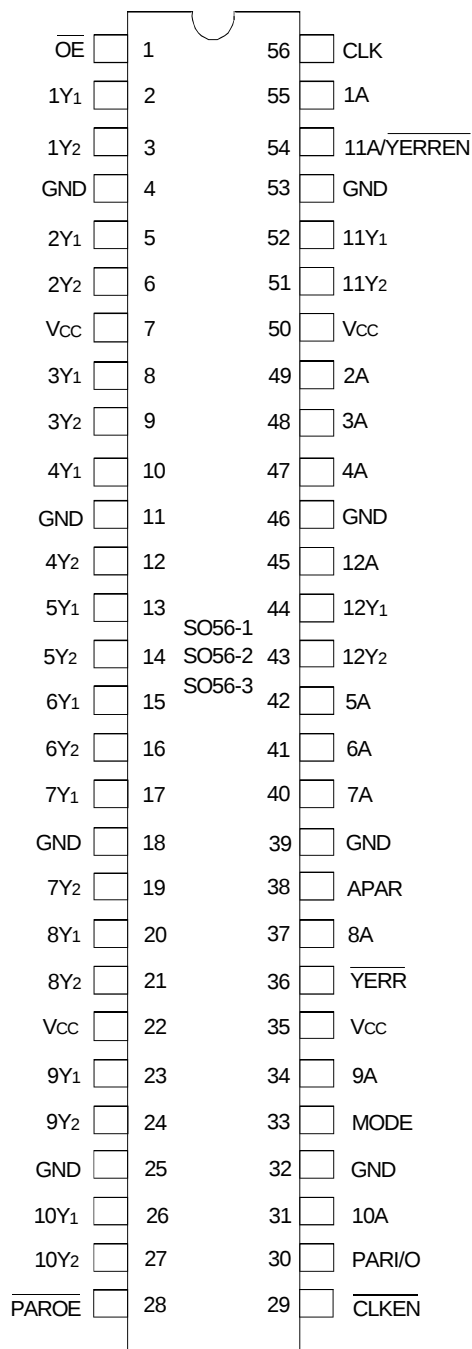
Symbol	Parameter ⁽¹⁾	Conditions	Typ.	Max.	Unit
C_{IN}	Input Capacitance	$V_{IN} = 0V$	5	7	pF
C_{OUT}	Output Capacitance	$V_{OUT} = 0V$	7	9	pF
$C_{I/O}$	I/O Port Capacitance	$V_{IN} = 0V$	7	9	pF

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NOTE:

- As applicable to the device type.

PIN CONFIGURATION



**SSOP/
TSSOP/TVSOP
TOP VIEW**

DC ELECTRICAL CHARACTERISTICS OVER OPERATING RANGE

Following Conditions Apply Unless Otherwise Specified:

Operating Condition: $T_A = -40^{\circ}\text{C}$ to $+85^{\circ}\text{C}$

Symbol	Parameter	Test Conditions		Min.	Typ. ⁽¹⁾	Max.	Unit
V_{IH}	Input HIGH Voltage Level	$V_{CC} = 2.3\text{V}$ to 2.7V		1.7	—	—	V
		$V_{CC} = 2.7\text{V}$ to 3.6V		2	—	—	
V_{IL}	Input LOW Voltage Level	$V_{CC} = 2.3\text{V}$ to 2.7V		—	—	0.7	V
		$V_{CC} = 2.7\text{V}$ to 3.6V		—	—	0.8	
I_{IH}	Input HIGH Current	$V_{CC} = 3.6\text{V}$	$V_I = V_{CC}$	—	—	± 5	μA
I_{IL}	Input LOW Current	$V_{CC} = 3.6\text{V}$	$V_I = \text{GND}$	—	—	± 5	
I_{OZH}	High Impedance Output Current (3-State Output pins)	$V_{CC} = 3.6\text{V}$	$V_O = V_{CC}$	—	—	± 10	μA
I_{OZL}			$V_O = \text{GND}$	—	—	± 10	μA
I_{OH}	$\overline{\text{YERR}}$ Output	$V_{CC} = 0\text{V}$ to 3.6V	$V_O = V_{CC}$	—	—	± 10	μA
$I_{OZ}^{(2)}$		$V_{CC} = 3.6\text{V}$	$V_O = V_{CC}$ or GND	—	—	± 10	μA
V_{IK}	Clamp Diode Voltage	$V_{CC} = 2.3\text{V}$, $I_{IN} = -18\text{mA}$		—	-0.7	-1.2	V
V_H	Input Hysteresis	$V_{CC} = 3.3\text{V}$		—	100	—	mV
I_{CCL} I_{CCH} I_{CCZ}	Quiescent Power Supply Current	$V_{CC} = 3.6\text{V}$ $V_{IN} = \text{GND}$ or V_{CC}		—	0.1	40	μA
ΔI_{CC}	Quiescent Power Supply Current Variation	One input at $V_{CC} - 0.6\text{V}$, other inputs at V_{CC} or GND		—	—	750	μA
C_i	Control Inputs	$V_{CC} = 3.3\text{V}$	$V_I = V_{CC}$ or GND	—	5.5	—	pF
	Data Inputs			—	5.5	—	
C_o	$\overline{\text{YERR}}$ Output	$V_{CC} = 3.3\text{V}$	$V_O = V_{CC}$ or GND	—	5	—	pF
	Data Outputs			—	6	—	
C_{IO}	PARI/O	$V_{CC} = 3.3\text{V}$	$V_O = V_{CC}$ or GND	—	7	—	pF

NOTES:

- Typical values are at $V_{CC} = 3.3\text{V}$, $+25^{\circ}\text{C}$ ambient.
- For I/O ports, the parameter I_{OZ} includes the input leakage current.

BUS-HOLD CHARACTERISTICS

Symbol	Parameter ⁽¹⁾	Test Conditions		Min.	Typ. ⁽²⁾	Max.	Unit
I_{BHH} I_{BHL}	Bus-Hold Input Sustain Current	$V_{CC} = 3.0\text{V}$	$V_I = 2.0\text{V}$	-75	—	—	μA
			$V_I = 0.8\text{V}$	75	—	—	
I_{BHH} I_{BHL}	Bus-Hold Input Sustain Current	$V_{CC} = 2.3\text{V}$	$V_I = 1.7\text{V}$	-45	—	—	μA
			$V_I = 0.7\text{V}$	45	—	—	
I_{BHHO} $I_{BHL O}$	Bus-Hold Input Overdrive Current	$V_{CC} = 3.6\text{V}$	$V_I = 0$ to 3.6V	—	—	± 500	μA

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NOTES:

- Pins with Bus-hold are identified in the pin description.
- Typical values are at $V_{CC} = 3.3\text{V}$, $+25^{\circ}\text{C}$ ambient.

OUTPUT DRIVE CHARACTERISTICS xYx PORTS

Symbol	Parameter	Test Conditions ⁽¹⁾		Min.	Max.	Unit
V _{OH}	Output HIGH Voltage	V _{CC} = 2.3V to 3.6V	I _{OH} = – 0.1mA	V _{CC} – 0.2	—	V
		V _{CC} = 2.3V	I _{OH} = – 6mA	2	—	
		V _{CC} = 2.3V	I _{OH} = – 12mA	1.7	—	
		V _{CC} = 2.7V		2.2	—	
		V _{CC} = 3V		2.4	—	
		V _{CC} = 3V	I _{OH} = – 24mA	2	—	
V _{OL}	Output LOW Voltage	V _{CC} = 2.3V to 3.6V	I _{OL} = 0.1mA	—	0.2	V
		V _{CC} = 2.3V	I _{OL} = 6mA	—	0.4	
			I _{OL} = 12mA	—	0.7	
		V _{CC} = 2.7V	I _{OL} = 12mA	—	0.4	
I _{OH}	High-Level Output Current	V _{CC} = 2.3V	Y Port	—	–12	mA
		V _{CC} = 2.7V		—	–12	
		V _{CC} = 3V	PARI/O	—	–12	
			Y Port	—	–24	
I _{OL}	Low-Level Output Current	V _{CC} = 2.3V	Y Port	—	12	mA
		V _{CC} = 2.7V		—	12	
		V _{CC} = 3V	PARI/O	—	12	
			Y Port	—	24	
			$\overline{\text{YERR}}$ Output	—	24	

OUTPUT DRIVE CHARACTERISTICS FOR $\overline{\text{YERR}}$ AND PARI/O

Symbol	Parameter	Test Conditions ⁽¹⁾		Min.	Max.	Unit
V _{OH}	PARI/O	V _{CC} = 3V	I _{OH} = – 12mA	2	—	V
V _{OL}	PARI/O	V _{CC} = 3V	I _{OL} = 12mA	—	0.55	V
V _{OL}	$\overline{\text{YERR}}$ Output only	V _{CC} = 3V	I _{OL} = 24mA	—	0.5	V

NOTE:

- V_{IH} and V_{IL} must be within the min. or max. range shown in the DC ELECTRICAL CHARACTERISTICS OVER OPERATING RANGE table for the appropriate V_{CC} range. T_A = – 40°C to + 85°C.

OPERATING CHARACTERISTICS FOR BUFFER MODE, $T_A = 25^\circ\text{C}$

Symbol	Parameter	Test Conditions	VCC = 2.5V $\pm$ 0.2V	VCC = 3.3V $\pm$ 0.3V	Unit
			Typical	Typical	
CPD	Power Dissipation Capacitance Outputs enabled	CL = 0pF, f = 10Mhz	57.5	65	pF
	Power Dissipation Capacitance Outputs disabled		15	17.5	

OPERATING CHARACTERISTICS FOR REGISTER MODE, $T_A = 25^\circ\text{C}$

Symbol	Parameter	Test Conditions	VCC = 2.5V $\pm$ 0.2V	VCC = 3.3V $\pm$ 0.3V	Unit
			Typical	Typical	
CPD	Power Dissipation Capacitance Outputs enabled	CL = 0pF, f = 10Mhz	57	87.5	pF
	Power Dissipation Capacitance Outputs disabled		16.5	34	

SIMULTANEOUS SWITCHING CHARACTERISTICS ⁽¹⁾

Parameter		From (Input)	To (Output)	VCC = 2.5V $\pm$ 0.2V		VCC = 2.7V		VCC = 3.3V $\pm$ 0.3V		Unit
				Min.	Max.	Min.	Max.	Min.	Max.	
tPLH	Register mode	CLK	Y	1.8	6.5		6.1	1.8	5	ns
tPHL				1.4	5.9		5.1	1.7	4.5	

NOTE:

1. All outputs switching.

SWITCHING CHARACTERISTICS ⁽¹⁾

Symbol	Parameter	V _{CC} = 2.5V ± 0.2V		V _{CC} = 2.7V		V _{CC} = 3.3V ± 0.3V		Unit
		Min.	Max.	Min.	Max.	Min.	Max.	
f _{MAX}		125	—	125	—	125	—	MHz
t _{PLH} t _{PHL}	Propagation Delay, Buffer Mode xA to xYx	1	4.4	—	4.2	1.1	3.8	ns
t _{PLH} t _{PHL}	Propagation Delay, Both Modes CLK to YERR	1	5.7	—	4.9	1.4	4.4	ns
t _{PLH} t _{PHL}	Propagation Delay, Both Modes CLK to PARI/O	1.2	8.6	—	7.9	1.7	6.6	ns
t _{PLH} t _{PHL}	Propagation Delay, Both Modes ⁽²⁾ CLK to PARI/O	1	6.8	—	5.2	1.3	4.5	ns
t _{PLH} t _{PHL}	Propagation Delay, Both Modes Mode to xYx	1	5.9	—	5.8	1.3	4.9	ns
t _{PLH}	Propagation Delay, Register Mode CLK to xYx	1	6.1	—	5.5	1.2	4.8	ns
t _{PHL}		1	5.9	—	4.9	1.2	4.6	ns
t _{PLH}	Propagation Delay, Both Modes OE to YERR	1	3.6	—	4.2	1.9	4	ns
t _{PHL}	Propagation Delay, Both Modes OE to YERR	1.2	5.1	—	4.9	1.5	4.2	ns
t _{PZH} t _{PZL}	Output Enable Time, Both Modes OE to xYx	1.1	6.5	—	6.4	1.4	5.4	ns
t _{PZH} t _{PZL}	Output Enable Time, Both Modes PAROE to PARI/O	1	5.6	—	6	1	4.8	ns
t _{PHZ} t _{PLZ}	Output Disable Time, Both Modes OE to xYx	1	6.4	—	5.2	1.7	5	ns
t _{PHZ} t _{PLZ}	Output Disable Time, Both Modes PAROE to PARI/O	1	3.2	—	3.8	1.2	3.8	ns
tsu	Set-up Time, Register Mode 1A-12A before CLK↑	1.7	—	1.9	—	1.45	—	ns
tsu	Set-up Time, Buffer Mode 1A to 10A before CLK↑	5.9	—	5.2	—	4.4	—	ns
tsu	Set-up Time, Register Mode APAR before CLK↑	1.2	—	1.5	—	1.3	—	ns
tsu	Set-up Time, Buffer Mode APAR before CLK↑	4.6	—	3.6	—	3.1	—	ns
tsu	Set-up Time, Both Modes PARI/O before CLK↑	2.4	—	2	—	1.7	—	ns
tsu	Set-up Time, Buffer Mode 11A/YERREN before CLK↑	2	—	1.9	—	1.6	—	ns
tsu	Set-up Time, Register Mode CLKEN before CLK↑	2.5	—	2.6	—	2.2	—	ns
th	Hold Time, Register Mode 1A-12A after CLK↑	0.4	—	0.25	—	0.55	—	ns
th	Hold Time, Buffer Mode 1A-10A after CLK↑	0.25	—	0.25	—	0.25	—	ns
th	Hold Time, Register Mode APAR after CLK↑	0.7	—	0.4	—	0.7	—	ns
th	Hold Time, Buffer Mode APAR after CLK↑	0.25	—	0.25	—	0.25	—	ns
th	Hold Time, Register Mode PARI/O after CLK↑	0.25	—	0.25	—	0.4	—	ns

SWITCHING CHARACTERISTICS ⁽¹⁾ (CONTINUED)

Symbol	Parameter	V _{CC} = 2.5V ± 0.2V		V _{CC} = 2.7V		V _{CC} = 3.3V ± 0.3V		Unit
		Min.	Max.	Min.	Max.	Min.	Max.	
t _H	Hold Time, Buffer Mode PARI/O after CLK↑	0.25	—	0.25	—	0.5	—	ns
t _H	Hold Time, Buffer Mode 11A/YERREN after CLK↑	0.25	—	0.25	—	0.4	—	ns
t _H	Hold Time, Register Mode CLKEN after CLK↑	0.25	—	0.5	—	0.4	—	ns
t _w	Pulse Width, CLK↑	3	—	3	—	3	—	ns
t _{SK(O)}	Output Skew ⁽³⁾	—	—	—	—	—	500	ps

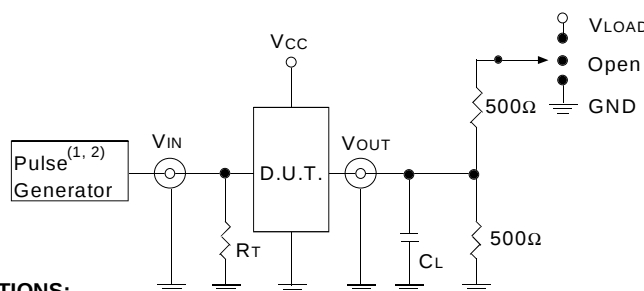
TEST CIRCUITS AND WAVEFORMS:

TEST CONDITIONS

Symbol	V _{CC} (1)= 3.3V±0.3V	V _{CC} (1)= 2.7V	V _{CC} (2)= 2.5V±0.2V	Unit
V _{LOAD}	6	6	2 x V _{CC}	V
V _{IH}	2.7	2.7	V _{CC}	V
V _T	1.5	1.5	V _{CC} / 2	V
V _{LZ}	300	300	150	mV
V _{HZ}	300	300	150	mV
C _L	50	50	30	pF

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TEST CIRCUITS FOR ALL OUTPUTS



DEFINITIONS:

C_L = Load capacitance: includes jig and probe capacitance.
R_T = Termination resistance: should be equal to Z_{OUT} of the Pulse Generator.

NOTES:

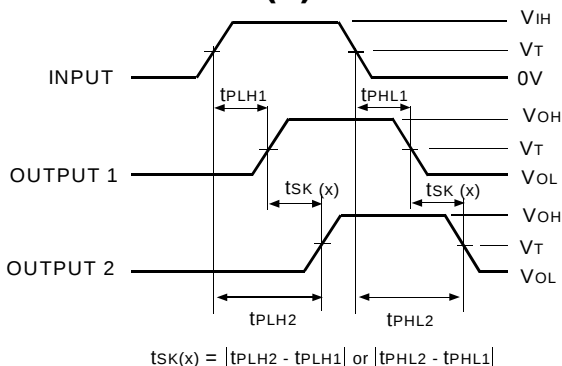
1. Pulse Generator for All Pulses: Rate ≤ 10MHz; t_r ≤ 2.5ns; t_r ≤ 2.5ns.
2. Pulse Generator for All Pulses: Rate ≤ 10MHz; t_r ≤ 2ns; t_r ≤ 2ns.

SWITCH POSITION:

Test	Switch
Open Drain Disable Low Enable Low	V _{LOAD}
Disable High Enable High	GND
All Other tests	Open

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OUTPUT SKEW - t_{SK} (x)



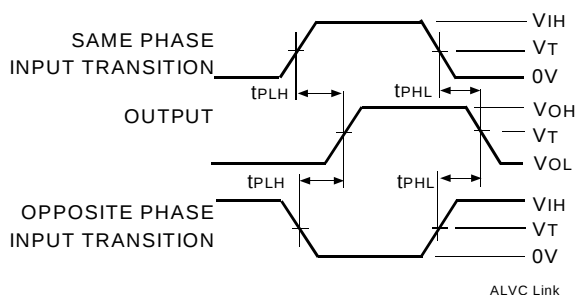
$$t_{SK}(x) = |t_{PLH2} - t_{PLH1}| \text{ or } |t_{PHL2} - t_{PHL1}|$$

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NOTES:

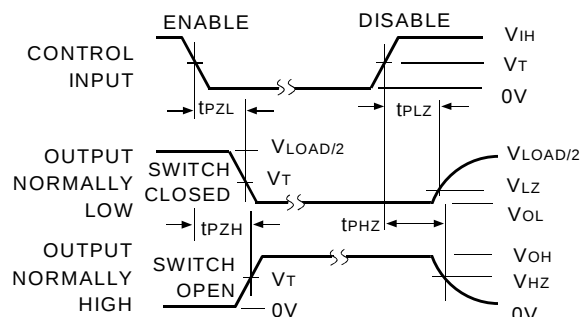
1. For t_{SK}(o) OUTPUT1 and OUTPUT2 are any two outputs.
2. For t_{SK}(b) OUTPUT1 and OUTPUT2 are in the same bank.

PROPAGATION DELAY



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ENABLE AND DISABLE TIMES

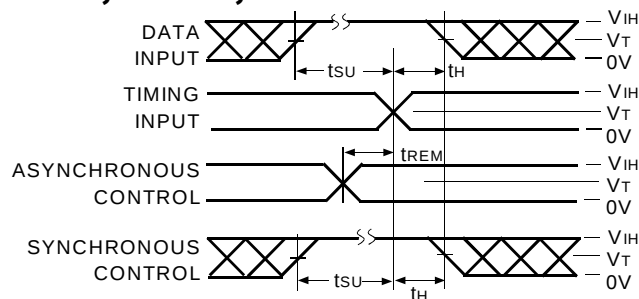


ALVC Link

NOTE:

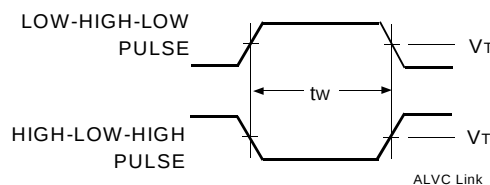
1. Diagram shown for input Control Enable-LOW and input Control Disable-HIGH.

SET-UP, HOLD, AND RELEASE TIMES



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PULSE WIDTH



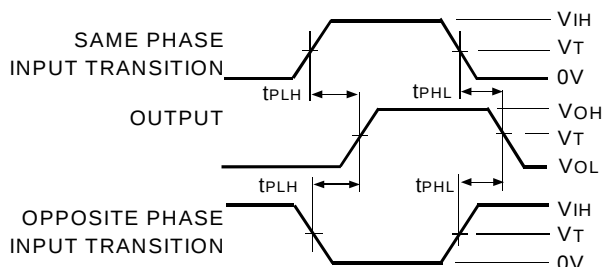
ALVC Link

TEST CIRCUITS AND WAVEFORMS:

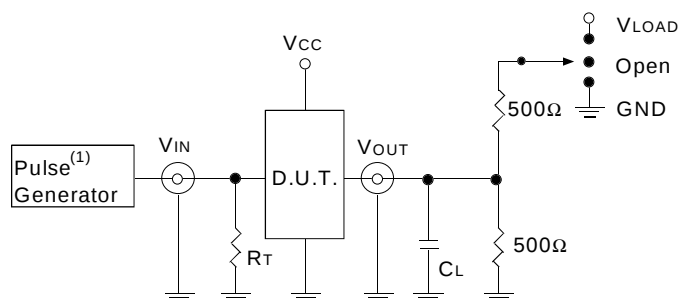
TEST CONDITIONS

Symbol	$V_{CC}^{(1)} = 2.5V \pm 0.2V$	Unit
V_{LOAD}	$2 \times V_{CC}$	V
V_{IH}	V_{CC}	V
V_T	$V_{CC}/2$	V
V_{LZ}	150	mV
V_{HZ}	150	mV
C_L	30	pF

PROPAGATION DELAY



TEST CIRCUITS FOR ALL OUTPUTS



DEFINITIONS:

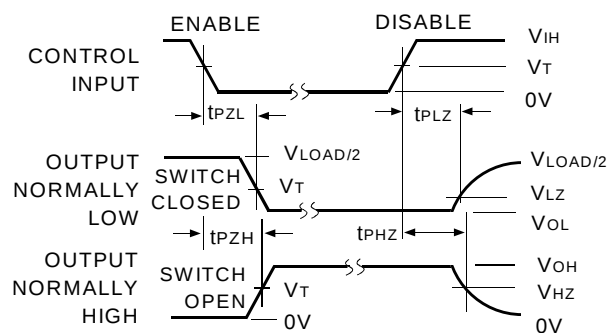
C_L = Load capacitance: includes jig and probe capacitance.

R_T = Termination resistance: should be equal to Z_{out} of the Pulse Generator.

NOTE:

1. Pulse Generator for All Pulses: Rate $\leq 10\text{MHz}$; $t_f \leq 2\text{ns}$; $t_r \leq 2\text{ns}$.

ENABLE AND DISABLE TIMES



NOTE:

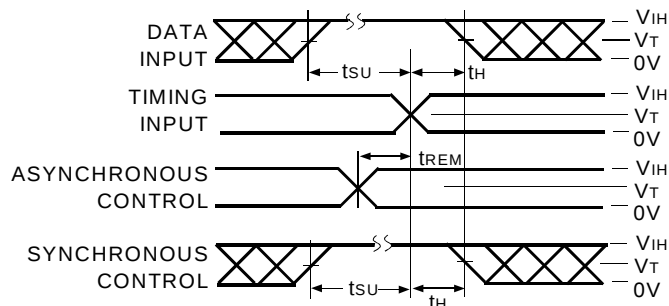
1. Diagram shown for input Control Enable-LOW and input Control Disable-HIGH.

SWITCH POSITION:

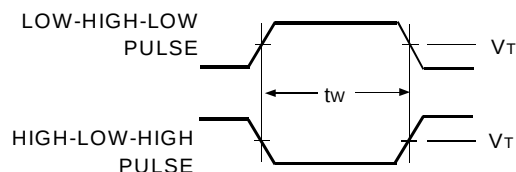
Test	Switch
Open Drain	V_{LOAD}
Disable Low	
Enable Low	
Disable High	GND
Enable High	
All Other tests	Open

NEW16link

SET-UP, HOLD, AND RELEASE TIMES

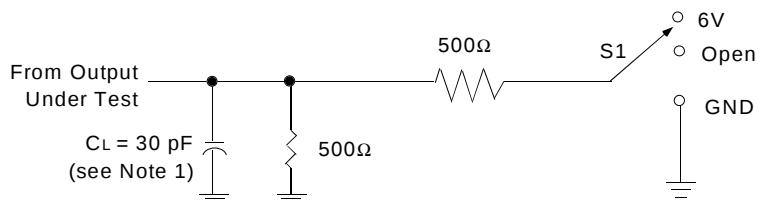


PULSE WIDTH

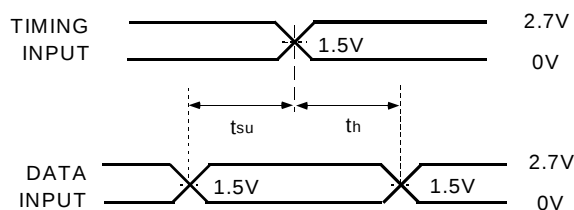


PARAMETER MEASUREMENT INFORMATION

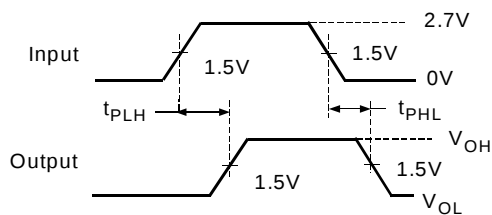
$V_{CC} = 2.7V$ AND $3.3V \pm 0.3V$



LOAD CIRCUIT



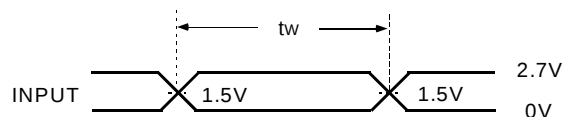
VOLTAGE WAVEFORMS SETUP AND HOLD TIMES



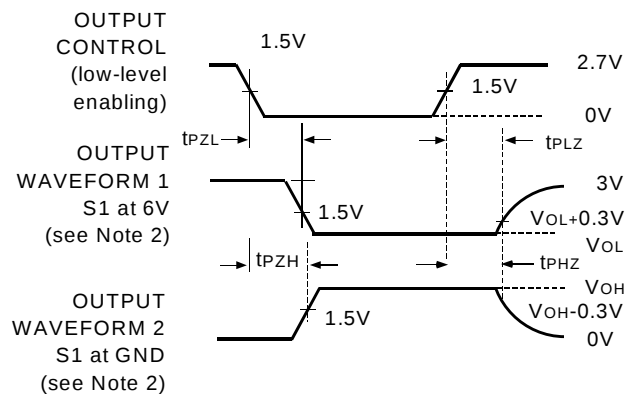
VOLTAGE WAVEFORMS PROPAGATION DELAY TIMES

TEST	S1
t_{pd}	Open
t_{PLZ}/t_{PZL}	6V
t_{PHZ}/t_{PZH}	GND

YERR	S1
t_{PHL} (see Note 8)	6V
t_{PLH} (see Note 9)	6V



VOLTAGE WAVEFORMS PULSE DURATION



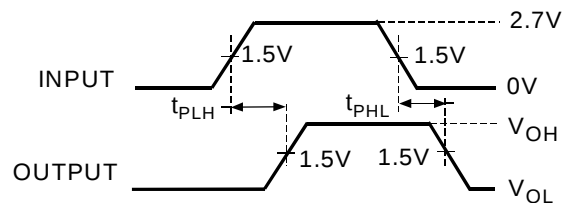
VOLTAGE WAVEFORMS ENABLE AND DISABLE TIMES

NOTES:

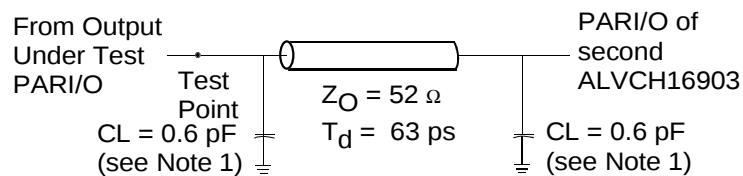
- C_L includes probe and jig capacitance.
- Waveform 1 is for an output with internal conditions such that the output is low except when disabled by the output control. Waveform 2 is for an output with internal conditions such that the output is high except when disabled by the output control.
- All input pulses are supplied by generators having the following characteristics: $PRR \leq 10 \text{ MHz}$, $Z_O = 50\Omega$, $t_r \leq 2 \text{ ns}$, $t_f \leq 2 \text{ ns}$.
- The outputs are measured one at a time with one transition per measurement.
- t_{PLZ} and t_{PHZ} are the same as t_{dis} .
- t_{PZL} and t_{PZH} are the same as t_{en} .
- t_{PLH} and t_{PHL} are the same as t_{pd} .
- t_{PHL} is measured at 1.5V.
- t_{PLH} is measured at $V_{OL} + 0.3V$.

LOAD CIRCUIT AND VOLTAGE WAVEFORMS

$V_{CC} = 2.7V$ AND $3.3V \pm 0.3V$



PARI/O LOAD CIRCUIT

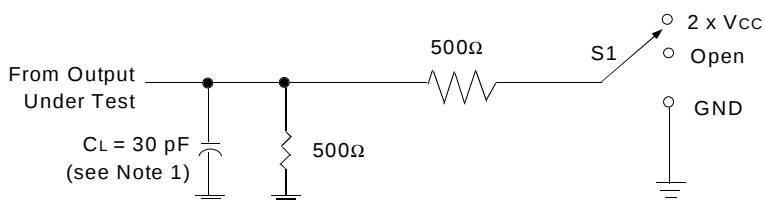


NOTE:

1. C_L includes probe and jig capacitance.

PARAMETER MEASUREMENT INFORMATION

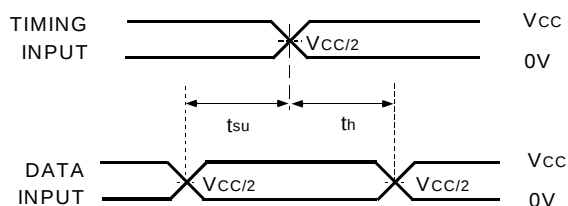
$$V_{CC} = 2.5V \pm 0.2V$$



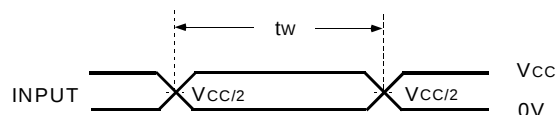
LOAD CIRCUIT

TEST	S1
t_{pd} t_{PLZ}/t_{PZL} t_{PHZ}/t_{PZH}	Open 2 x V_{CC} GND

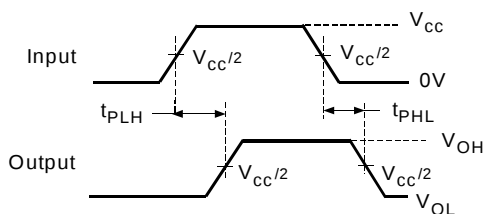
YERR	S1
t_{PHL} (see Note 8)	2 x V_{CC}
t_{PLH} (see Note 9)	2 x V_{CC}



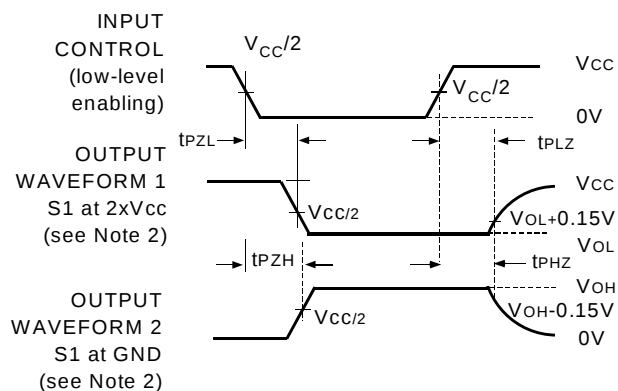
VOLTAGE WAVEFORMS SETUP AND HOLD TIMES



VOLTAGE WAVEFORMS PULSE DURATION



VOLTAGE WAVEFORMS PROPAGATION DELAY TIMES



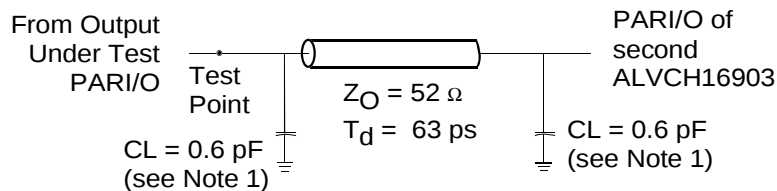
VOLTAGE WAVEFORMS ENABLE AND DISABLE TIMES

NOTES:

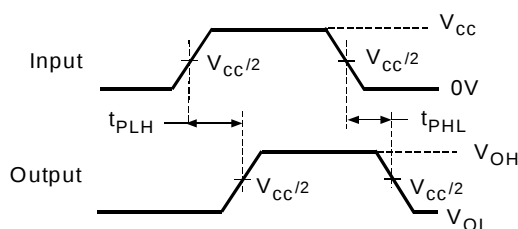
- C_L includes probe and jig capacitance.
- Waveform 1 is for an output with internal conditions such that the output is low except when disabled by the output control. Waveform 2 is for an output with internal conditions such that the output is high except when disabled by the output control.
- All input pulses are supplied by generators having the following characteristics: $PRR \leq 10 \text{ MHz}$, $Z_O = 50\Omega$, $t_r \leq 2 \text{ ns}$, $t_f \leq 2 \text{ ns}$.
- The outputs are measured one at a time with one transition per measurement.
- t_{PLZ} and t_{PHZ} are the same as t_{dis} .
- t_{PZL} and t_{PZH} are the same as t_{en} .
- t_{PLH} and t_{PHL} are the same as t_{pd} .
- t_{PHL} is measured at $V_{CC}/2$.
- t_{PLH} is measured at $V_{OL} + 0.15V$.

PARAMETER MEASUREMENT INFORMATION

$$V_{CC} = 2.5V \pm 0.2V$$



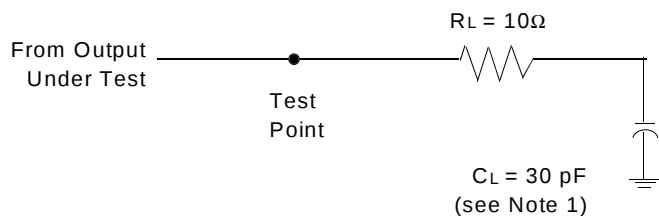
LOAD CIRCUIT



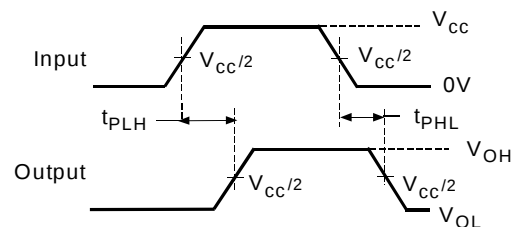
VOLTAGE WAVEFORMS PROPAGATION DELAY TIMES

NOTES:

1. C_L includes probe and jig capacitance.
2. All input pulses are supplied by generators having the following characteristics: $PRR \leq 10 \text{ MHz}$, $Z_o = 50 \Omega$, $t_r \leq 2 \text{ ns}$, $t_f \leq 2 \text{ ns}$.
3. t_{PLH} and t_{PHL} are the same as t_{pd} .



LOAD CIRCUIT



VOLTAGE WAVEFORMS PROPAGATION DELAY TIMES

NOTES:

1. C_L includes probe and jig capacitance.
2. All input pulses are supplied by generators having the following characteristics: $PRR \leq 10 \text{ MHz}$, $Z_o = 50 \Omega$, $t_r \leq 2 \text{ ns}$, $t_f \leq 2 \text{ ns}$.

ORDERING INFORMATION

IDT	XX	ALVC	X	XXX	XXX	XX	
	Temp. Range		Bus-Hold	Family	Device Type	Package	
						PV	Shrink Small Outline Package (SO56-1)
						PA	Thin Shrink Small Outline Package (SO56-2)
						PF	Thin Very Small Outline Package (SO56-3)
						903	12-Bit Universal Bus Driver with Parity Checker
						16	Double-Density with Resistors, $\pm 24\text{mA}$
						H	Bus-Hold
						74	-40°C to +85°C



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