3.3V CMOS 18-BIT UNIVERSAL BUS TRANSCEIVER WITH PARITY GENERATORS/ CHECKERS AND BUS-HOLD

IDT74ALVCH16901

FEATURES:

- 0.5 MICRON CMOS Technology
- Typical $t_{SK(0)}$ (Output Skew) < 250ps
- ESD > 2000V per MIL-STD-883, Method 3015; > 200V using machine model (C = 200pF, R = 0)
- 0.50mm pitch TSSOP package
- Extended commercial range of -40°C to +85°C
- V_{CC} = 3.3V ± 0.3V, Normal Range
- V_{CC} = 2.7V to 3.6V, Extended Range
- V_{CC} = 2.5V ± 0.2V
- CMOS power levels (0.4µW typ. static)
- Rail-to-Rail output swing for increased noise margin

Drive Features for ALVCH16901:

- High Output Drivers: ±24mA
- Suitable for heavy loads

APPLICATIONS:

- 3.3V High Speed Systems
- 3.3V and lower voltage computing systems

DESCRIPTION:

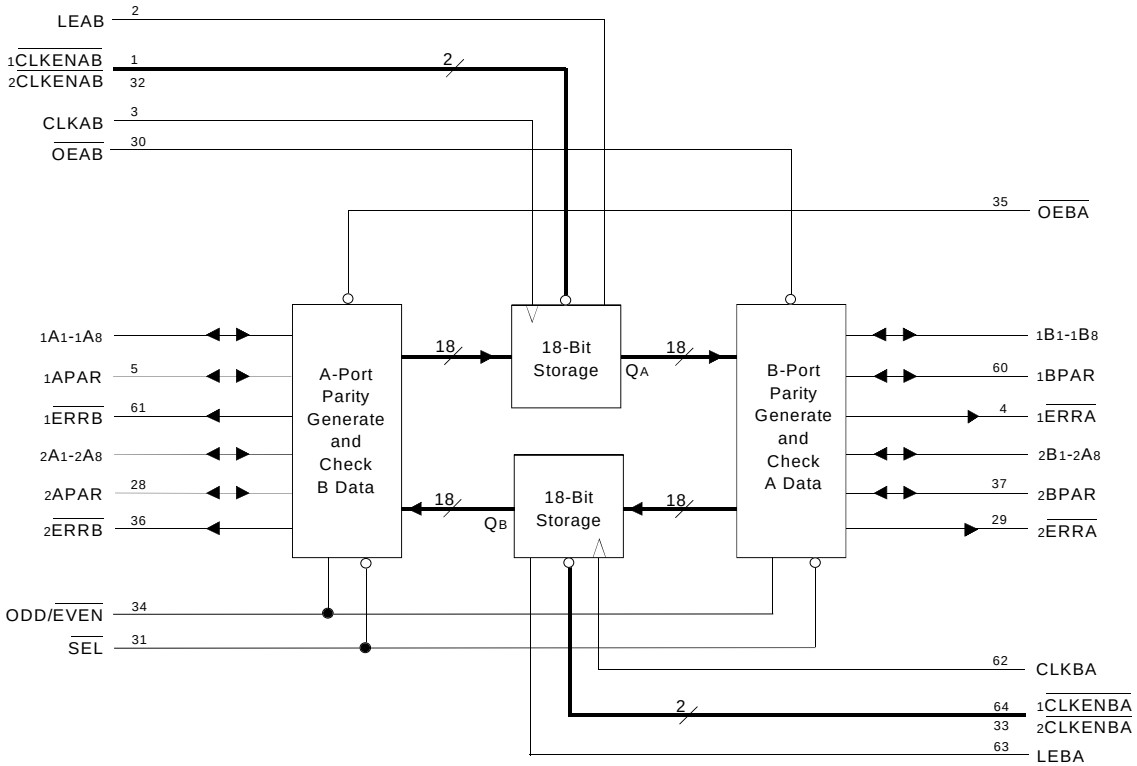
This 18-bit universal bus transceiver is built using advanced dual metal CMOS technology. The ALVCH16901 is a dual 9-bit to dual 9-bit parity transceiver with registers. The device can operate as a feed-through transceiver or it can generate/check parity from the two 8-bit data buses in either direction.

The ALVCH16901 features independent clock (CLKAB or CLKBA), latch-enable (LEAB or LEBA), and dual 9-bit clock enable ($\overline{\text{CLKENAB}}$ or $\overline{\text{CLKENBA}}$) inputs. It also provides parity-enable ($\overline{\text{SEL}}$) and parity-select (ODD/$\overline{\text{EVEN}}$) inputs and separate error-signal ($\overline{\text{ERRA}}$ and $\overline{\text{ERRB}}$) outputs for checking parity. The direction of data flow is controlled by $\overline{\text{OEAB}}$ and $\overline{\text{OEBA}}$. When $\overline{\text{SEL}}$ is low, the parity functions are enabled. When $\overline{\text{SEL}}$ is high, the parity functions are disabled and the device acts as an 18-bit registered transceiver.

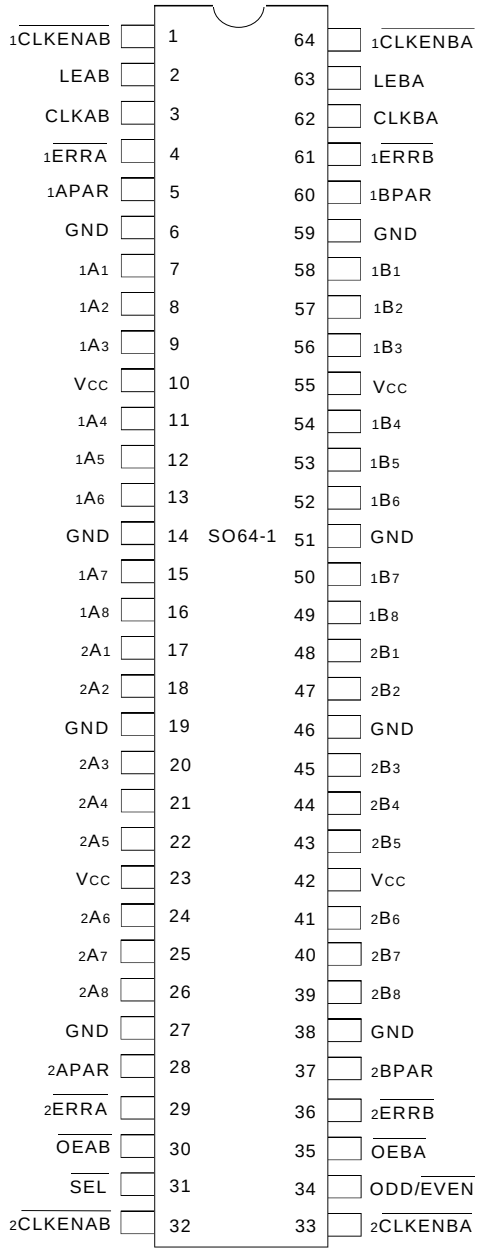
The ALVCH16901 has been designed with a ±24mA output driver. This driver is capable of driving a moderate to heavy load while maintaining speed performance.

The ALVCH16901 has "bus-hold" which retains the inputs' last state whenever the input bus goes to a high impedance. This prevents floating inputs and eliminates the need for pull-up/down resistors.

FUNCTIONAL BLOCK DIAGRAM



PIN CONFIGURATION



TSSOP/TVSOP
TOP VIEW

CAPACITANCE (T_A = +25°C, f = 1.0MHz)

Symbol	Parameter(1)	Conditions	Typ.	Max.	Unit
C_{IN}	Input Capacitance	V_{IN} = 0V	5	7	pF
C_{OUT}	Output Capacitance	V_{OUT} = 0V	7	9	pF
$C_{I/O}$	I/O Port Capacitance	V_{IN} = 0V	7	9	pF

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NOTE:
1. As applicable to the device type.

ABSOLUTE MAXIMUM RATING (1)

Symbol	Description	Max.	Unit
V_{TERM}(2)	Terminal Voltage with Respect to GND	– 0.5 to + 4.6	V
V_{TERM}(3)	Terminal Voltage with Respect to GND	– 0.5 to V_{CC} + 0.5	V
T_{STG}	Storage Temperature	– 65 to + 150	°C
I_{OUT}	DC Output Current	– 50 to + 50	mA
I_{IK}	Continuous Clamp Current, V_I < 0 or V_I > V_{CC}	± 50	mA
I_{OK}	Continuous Clamp Current, V_O < 0	– 50	mA
I_{CC} I_{SS}	Continuous Current through each V_{CC} or GND	±100	mA

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NOTES:
1. Stresses greater than those listed under ABSOLUTE MAXIMUM RATINGS may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect reliability.
2. V_{CC} terminals.
3. All terminals except V_{CC}.

PIN ENABLE

Pin Names	Description
$\overline{OEAB}$	A-to-B Output Enable Input (Active LOW)
$\overline{OEBA}$	B-to-A Output Enable Input (Active LOW)
LEAB	A-to-B Latch Enable Input
LEBA	B-to-A Latch Enable Input
$\overline{xCLKENAB}$	A-to-B 9-bit Clock Enables
$\overline{xCLKENBA}$	B-to-A 9-bit Clock Enables
CLKAB	A-to-B Clock Input
CLKBA	B-to-A Clock Input
$\overline{xERRA}$	A Error-Signal Outputs
$\overline{xERRB}$	B Error-Signal Outputs
xAPAR	A Port Parities
xBPAR	B Port Parities
ODD/$\overline{EVEN}$	Parity Select Input
$\overline{SEL}$	Parity Enables
xAx	A-to-B Data Inputs or B-to-A 3-State Outputs (1)
xBx	B-to-A Data Inputs or A-to-B 3-State Outputs (1)

NOTE:
1. These pins have “Bus-Hold.” All other pins are standard inputs, outputs, or I/Os.

FUNCTION TABLE (1, 2)

Inputs					Outputs
$\overline{CLKENAB}$	$\overline{OEAB}$	LEAB	CLKAB	xAx	xBx
X	H	X	X	X	Z
X	L	H	X	L	L
X	L	H	X	H	H
H	L	L	X	X	B_0(3)
L	L	L	↑	L	L
L	L	L	↑	H	H
L	L	L	L	X	B_0(3)
L	L	L	H	X	B_0(4)

NOTES:
1. H = HIGH Voltage Level
   L = LOW Voltage Level
   X = Don't Care
   ↑ = LOW-to-HIGH Transition
2. A-to-B data flow is shown. B-to-A data flow is similar but uses $\overline{OEBA}$, LEBA, and $\overline{CLKENBA}$.
3. Output level before the indicated steady-state conditions were established.
4. Output level before the indicated steady-state conditions were established, provided that CLKAB was LOW before LEAB went LOW.

PARITY ENABLE

Inputs			Operation or Function	
$\overline{SEL}$	$\overline{OEBA}$	$\overline{OEAB}$		
L	H	L	Parity is checked on port A and is generated on port B.	
L	L	H	Parity is checked on port B and is generated on port A.	
L	H	H	Parity is checked on port B and port A.	
L	L	L	Parity is generated on port A and B if device is in FF mode.	
H	L	L	Parity functions are	Q_A data to B, Q_B data to A
H	L	H	disabled; device acts as	Q_B data to A
H	H	L	a standard 18-bit	Q_A data to B
H	H	H	registered transceiver.	Isolation

PARITY

Inputs								Outputs			
$\overline{SEL}$	$\overline{OEBA}$	$\overline{OEAB}$	ODD/$\overline{EVEN}$	$\sum$ OF INPUTS A1–A8 = H	$\sum$ OF INPUTS B1–B8 = H	xAPAR	xBPAR	xAPAR	$\overline{xERRA}$	xBPAR	$\overline{xERRB}$
L	H	L	L	0, 2, 4, 6, 8	N/A	L	N/A	N/A	H	L	Z
L	H	L	L	1, 3, 5, 7	N/A	L	N/A	N/A	L	H	Z
L	H	L	L	0, 2, 4, 6, 8	N/A	H	N/A	N/A	L	L	Z
L	H	L	L	1, 3, 5, 7	N/A	H	N/A	N/A	H	H	Z
L	L	H	L	N/A	0, 2, 4, 6, 8	N/A	L	L	Z	N/A	H
L	L	H	L	N/A	1, 3, 5, 7	N/A	L	H	Z	N/A	L
L	L	H	L	N/A	0, 2, 4, 6, 8	N/A	H	L	Z	N/A	L
L	L	H	L	N/A	1, 3, 5, 7	N/A	H	H	Z	N/A	H
L	H	L	H	0, 2, 4, 6, 8	N/A	L	N/A	N/A	L	H	Z
L	H	L	H	1, 3, 5, 7	N/A	L	N/A	N/A	H	L	Z
L	H	L	H	0, 2, 4, 6, 8	N/A	H	N/A	N/A	H	H	Z
L	H	L	H	1, 3, 5, 7	N/A	H	N/A	N/A	L	L	Z
L	L	H	H	N/A	0, 2, 4, 6, 8	N/A	L	H	Z	N/A	L
L	L	H	H	N/A	1, 3, 5, 7	N/A	L	L	Z	N/A	H
L	L	H	H	N/A	0, 2, 4, 6, 8	N/A	H	H	Z	N/A	H
L	L	H	H	N/A	1, 3, 5, 7	N/A	H	L	Z	N/A	L
L	H	H	L	0, 2, 4, 6, 8	0, 2, 4, 6, 8	L	L	N/A	H	N/A	H
L	H	H	L	1, 3, 5, 7	1, 3, 5, 7	L	L	N/A	L	N/A	L
L	H	H	L	0, 2, 4, 6, 8	0, 2, 4, 6, 8	H	H	N/A	L	N/A	L
L	H	H	L	1, 3, 5, 7	1, 3, 5, 7	H	H	N/A	H	N/A	H
L	H	H	H	0, 2, 4, 6, 8	0, 2, 4, 6, 8	L	L	N/A	L	N/A	L
L	H	H	H	1, 3, 5, 7	1, 3, 5, 7	L	L	N/A	H	N/A	H
L	H	H	H	0, 2, 4, 6, 8	0, 2, 4, 6, 8	H	H	N/A	H	N/A	H
L	H	H	H	1, 3, 5, 7	1, 3, 5, 7	H	H	N/A	L	N/A	L
L	L	L	L	N/A	N/A	N/A	N/A	PE (1)	Z	PE (1)	Z
L	L	L	H	N/A	N/A	N/A	N/A	PO (2)	Z	PO (2)	Z

NOTES:
1. Parity output is set to the level so that the specific bus side is set to even parity.
2. Parity output is set to the level so that the specific bus side is set to odd parity.

DC ELECTRICAL CHARACTERISTICS OVER OPERATING RANGE

Following Conditions Apply Unless Otherwise Specified:

Operating Condition: TA = – 40°C to +85°C

Symbol	Parameter	Test Conditions		Min.	Typ.(1)	Max.	Unit
V_{IH}	Input HIGH Voltage Level	V_{CC} = 2.3V to 2.7V		1.7	—	—	V
		V_{CC} = 2.7V to 3.6V		2	—	—	
V_{IL}	Input LOW Voltage Level	V_{CC} = 2.3V to 2.7V		—	—	0.7	V
		V_{CC} = 2.7V to 3.6V		—	—	0.8	
I_{IH}	Input HIGH Current	V_{CC} = 3.6V	V_I = V_{CC}	—	—	± 5	µA
I_{IL}	Input LOW Current	V_{CC} = 3.6V	V_I = GND	—	—	± 5	
I_{OZH}	High Impedance Output Current	V_{CC} = 3.6V	V_O = V_{CC}	—	—	± 10	µA
I_{OZL}	(3-State Output pins)		V_O = GND	—	—	± 10	µA
V_{IK}	Clamp Diode Voltage	V_{CC} = 2.3V, I_{IN} = – 18mA		—	– 0.7	– 1.2	V
V_H	Input Hysteresis	V_{CC} = 3.3V		—	100	—	mV
I_{CCL} I_{CCH} I_{CCZ}	Quiescent Power Supply Current	V_{CC} = 3.6V V_{IN} = GND or V_{CC}		—	0.1	40	µA
ΔI_{CC}	Quiescent Power Supply Current Variation	One input at V_{CC} – 0.6V, other inputs at V_{CC} or GND		—	—	750	µA

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NOTE:
1. Typical values are at V_{CC} = 3.3V, +25°C ambient.

BUS-HOLD CHARACTERISTICS

Symbol	Parameter(1)	Test Conditions		Min.	Typ.(2)	Max.	Unit
I_{BHH}	Bus-Hold Input Sustain Current	V_{CC} = 3.0V	V_I = 2.0V	– 75	—	—	µA
I_{BHL}			V_I = 0.8V	75	—	—	
I_{BHH}	Bus-Hold Input Sustain Current	V_{CC} = 2.3V	V_I = 1.7V	– 45	—	—	µA
I_{BHL}			V_I = 0.7V	45	—	—	
I_{BHHO}	Bus-Hold Input Overdrive Current	V_{CC} = 3.6V	V_I = 0 to 3.6V	—	—	± 500	µA
I_{BHLO}							

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NOTES:
1. Pins with Bus-hold are identified in the pin description.
2. Typical values are at V_{CC} = 3.3V, +25°C ambient.

OUTPUT DRIVE CHARACTERISTICS

Symbol	Parameter	Test Conditions[1]		Min.	Max.	Unit
V_{OH}	Output HIGH Voltage	V_{CC} = 2.3V to 3.6V	I_{OH} = – 0.1mA	V_{CC} – 0.2	—	V
		V_{CC} = 2.3V	I_{OH} = – 6mA	2	—	
		V_{CC} = 2.3V	I_{OH} = – 12mA	1.7	—	
		V_{CC} = 2.7V		2.2	—	
		V_{CC} = 3.0V		2.4	—	
		V_{CC} = 3.0V	I_{OH} = – 24mA	2	—	
V_{OL}	Output LOW Voltage	V_{CC} = 2.3V to 3.6V	I_{OL} = 0.1mA	—	0.2	V
		V_{CC} = 2.3V	I_{OL} = 6mA	—	0.4	
			I_{OL} = 12mA	—	0.7	
		V_{CC} = 2.7V	I_{OL} = 12mA	—	0.4	
		V_{CC} = 3.0V	I_{OL} = 24mA	—	0.55	

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NOTE:

1. V_{IH} and V_{IL} must be within the min. or max. range shown in the DC ELECTRICAL CHARACTERISTICS OVER OPERATING RANGE table for the appropriate V_{CC} range. T_A = – 40°C to + 85°C.

OPERATING CHARACTERISTICS, T_A = 25°C

Symbol	Parameter	Test Conditions	V_{CC} = 2.5V ± 0.2V Typical	V_{CC} = 3.3V ± 0.3V Typical	Unit
C_{PD}	Power Dissipation Capacitance Outputs enabled	C_L = 0pF, f = 10Mhz	22	27	pF
C_{PD}	Power Dissipation Capacitance Outputs disabled		5	8	pF

SWITCHING CHARACTERISTICS (1)

Symbol	Parameter	Vcc = 2.5V ± 0.2V		Vcc = 2.7V		Vcc = 3.3V ± 0.3V		Unit
		Min.	Max.	Min.	Max.	Min.	Max.	
f_{MAX}		125	—	125	—	125	—	MHz
t_{PLH} t_{PHL}	Propagation Delay xAx to xBx or xBx to xAx	1	5.2	—	4.8	1	4.4	ns
t_{PLH} t_{PHL}	Propagation Delay xAx to xBPAR or xBx to xAPAR	2	8.9	—	7.6	2	6.7	ns
t_{PLH} t_{PHL}	Propagation Delay xAPAR to xBPAR or xBPAR to xAPAR	1	5.7	—	5.2	1	4.7	ns
t_{PLH} t_{PHL}	Propagation Delay xAPAR to $x\overline{ERRA}$ or xBPAR to $x\overline{ERRB}$	2	9.7	—	8.7	2	7.5	ns
t_{PLH} t_{PHL}	Propagation Delay ODD/$\overline{EVEN}$ to $x\overline{ERRB}$ or $x\overline{ERRA}$	1.5	8.7	—	7.9	1.5	6.8	ns
t_{PLH} t_{PHL}	Propagation Delay ODD/$\overline{EVEN}$ to xAPAR or xBPAR	1.5	8.3	—	7.6	1.5	6.5	ns
t_{PLH} t_{PHL}	Propagation Delay $\overline{SEL}$ to xAPAR or xBPAR	1	6.1	—	5.9	1	5.1	ns
t_{PLH} t_{PHL}	Propagation Delay LEBA to xAx or LEAB to xBx	1	6	—	5.5	1	4.8	ns
t_{PLH} t_{PHL}	Propagation Delay LEBA to xAPAR or LEAB to xBPAR (parity feed through)	1.5	6.7	—	6	1.5	5.3	ns
t_{PLH} t_{PHL}	Propagation Delay LEBA to xAPAR or LEAB to xBPAR (parity generated)	2.5	9.8	—	8.3	2	7.4	ns
t_{PLH} t_{PHL}	Propagation Delay LEBA to $x\overline{ERRB}$ or LEAB to $x\overline{ERRA}$	2.5	9.9	—	8.5	2	7.5	ns
t_{PLH} t_{PHL}	Propagation Delay CLKBA to xAx or CLKAB to xBx	1	6.4	—	5.8	1	5.1	ns
t_{PLH} t_{PHL}	Propagation Delay CLKBA to xAPAR or CLKAB to xBPAR (parity feed through)	1.5	7.1	—	6.3	1.5	5.6	ns
t_{PLH} t_{PHL}	Propagation Delay CLKBA to xAPAR or CLKAB to xBPAR (parity generated)	2.5	10.2	—	8.7	2	7.7	ns
t_{PLH} t_{PHL}	Propagation Delay CLKBA to $x\overline{ERRB}$ or CLKAB to x $\overline{ERRA}$	2.5	10.5	—	8.9	2	7.9	ns

(CONTINUED ON NEXT PAGE)

SWITCHING CHARACTERISTICS (CONTINUED)[1]

Symbol	Parameter	Vcc = 2.5V ± 0.2V		Vcc = 2.7V		Vcc = 3.3V ± 0.3V		Unit
		Min.	Max.	Min.	Max.	Min.	Max.	
t_{PZH} t_{PZL}	Output Enable Time $\overline{OEAB}$ or $\overline{OEBA}$ to xBx, xBPAR or xAx, xAPAR	1.4	6.3	—	6.1	1	5.3	ns
t_{PZH} t_{PZL}	Output Enable Time $\overline{OEAB}$ or $\overline{OEBA}$ to x$\overline{ERRA}$ or x$\overline{ERRB}$	1.4	6.2	—	5.5	1	4.9	ns
t_{PZH} t_{PZL}	Output Enable Time $\overline{SEL}$ to x$\overline{ERRA}$ or x$\overline{ERRB}$	1.4	6.7	—	6.5	1	5.5	ns
t_{PHZ} t_{PLZ}	Output Disable Time $\overline{OEAB}$ or $\overline{OEBA}$ to xBx, xBPAR or xAx, xAPAR	1.3	6.1	—	5.2	1.5	4.9	ns
t_{PHZ} t_{PLZ}	Output Disable Time $\overline{OEAB}$ or $\overline{OEBA}$ to x$\overline{ERRA}$ or x$\overline{ERRB}$	1.3	7.3	—	6.5	1	5.7	ns
t_{PHZ} t_{PLZ}	Output Disable Time $\overline{SEL}$ to x$\overline{ERRA}$ or x$\overline{ERRB}$	1.3	6.4	—	5.4	1.5	4.9	ns
t_{SU}	Set-up Time, HIGH or LOW, xAx, xAPAR or xBx, xBPAR before CLK↑	1.9	—	2	—	1.7	—	ns
t_{SU}	Set-up Time, HIGH or LOW, x$\overline{CLKENAB}$ or x$\overline{CLKENBA}$ before CLK↑	2.1	—	2.1	—	1.7	—	ns
t_{SU}	Set-up Time, HIGH or LOW, xAx, xAPAR or xBx, xBPAR before LE↓	1.4	—	1.3	—	1.2	—	ns
t_H	Hold Time, HIGH or LOW, xAx, xAPAR or xBx, xBPAR after CLK↑	0.4	—	0.4	—	0.5	—	ns
t_H	Hold Time, HIGH or LOW, x$\overline{CLKENAB}$ or x$\overline{CLKENBA}$ after CLK↑	0.5	—	0.5	—	0.7	—	ns
t_H	Hold Time, HIGH or LOW, xAx, xAPAR or xBx, xBPAR after LE↓	0.9	—	1.1	—	0.9	—	ns
t_W	Pulse Width LEAB or LEBA HIGH	3	—	3	—	3	—	ns
t_W	Pulse Width CLKAB or CLKBA HIGH or LOW	3	—	3	—	3	—	ns
$t_{SK}(o)$	Output Skew[2]	—	—	—	—	—	500	ps

NOTES:
1. See test circuits and waveforms. T_A = – 40°C to + 85°C.
2. Skew between any two outputs of the same package and switching in the same direction.

TEST CIRCUITS AND WAVEFORMS

TEST CONDITIONS

Symbol	$V_{CC}^{(1)}$= 3.3V±0.3V	$V_{CC}^{(1)}$= 2.7V	$V_{CC}^{(2)}$= 2.5V±0.2V	Unit
V_{LOAD}	6	6	2 x Vcc	V
V_{IH}	2.7	2.7	Vcc	V
V_T	1.5	1.5	Vcc / 2	V
V_{LZ}	300	300	150	mV
V_{HZ}	300	300	150	mV
C_L	50	50	30	pF

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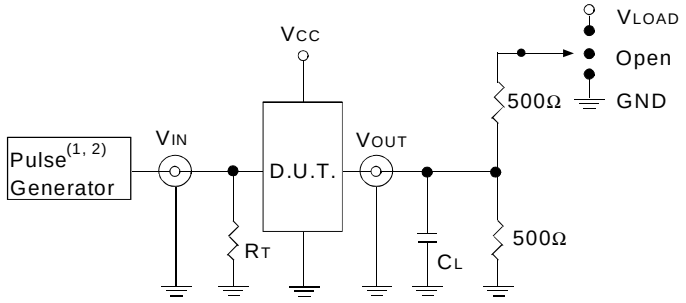
TEST CIRCUITS FOR ALL OUTPUTS



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DEFINITIONS:

C_L= Load capacitance: includes jig and probe capacitance.
R_T = Termination resistance: should be equal to Z_{OUT} of the Pulse Generator.

NOTES:

1. Pulse Generator for All Pulses: Rate ≤ 10MHz; t_F ≤ 2.5ns; t_R ≤ 2.5ns.
2. Pulse Generator for All Pulses: Rate ≤ 10MHz; t_F ≤ 2ns; t_R ≤ 2ns.

SWITCH POSITION

Test	Switch
Open Drain Disable Low Enable Low	V_{LOAD}
Disable High Enable High	GND
All Other tests	Open

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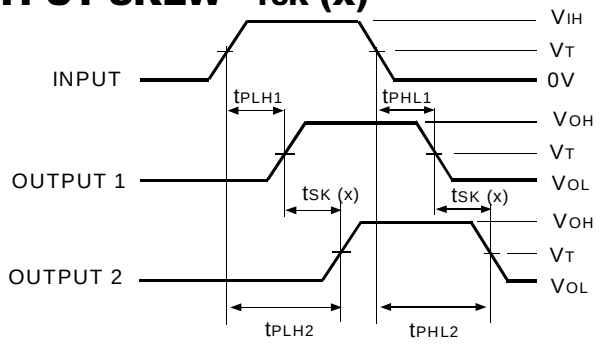
OUTPUT SKEW - t_{SK} (x)



$t_{SK(x)} = |t_{PLH2} - t_{PLH1}|$ or $|t_{PHL2} - t_{PHL1}|$

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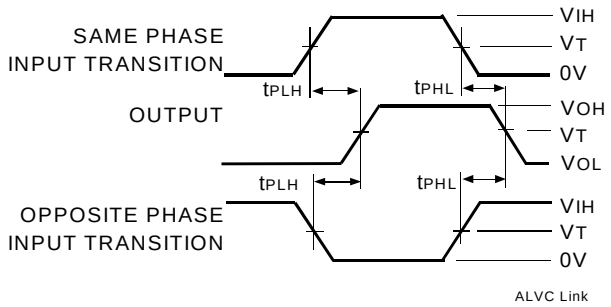
NOTES:

1. For t_{SK}(o) OUTPUT1 and OUTPUT2 are any two outputs.
2. For t_{SK}(b) OUTPUT1 and OUTPUT2 are in the same bank.

PROPAGATION DELAY



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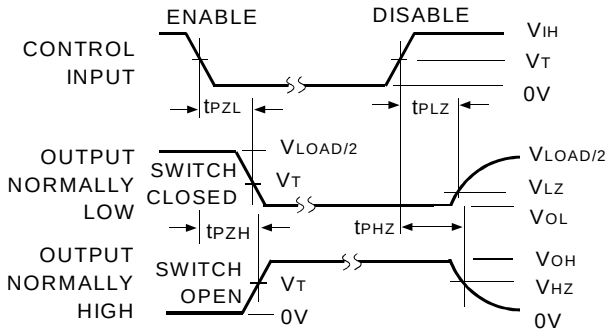
ENABLE AND DISABLE TIMES



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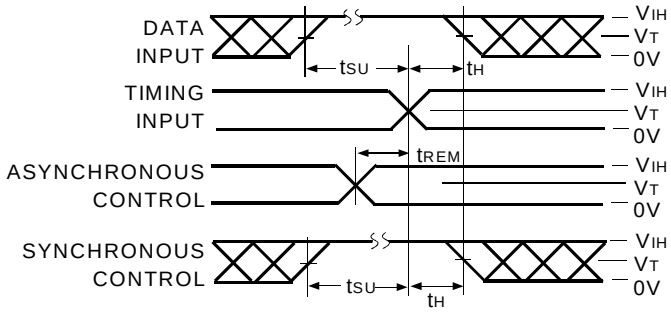
NOTE:

1. Diagram shown for input Control Enable-LOW and input Control Disable-HIGH.

SET-UP, HOLD, AND RELEASE TIMES



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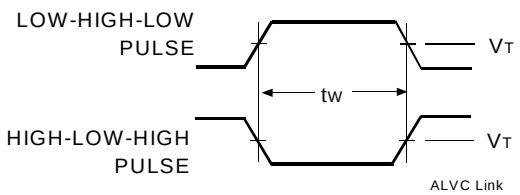
PULSE WIDTH



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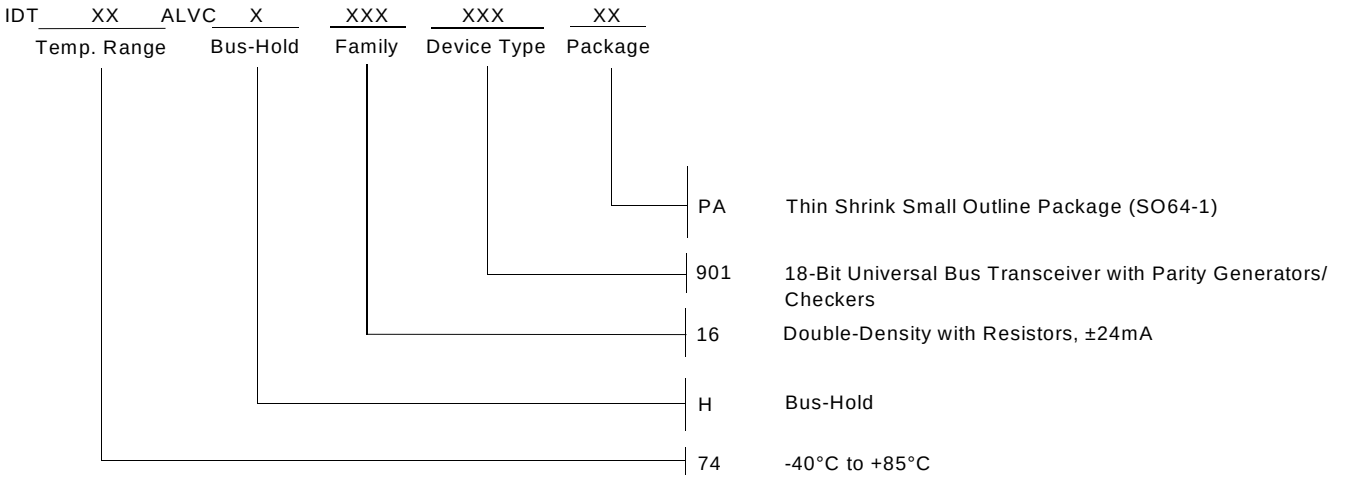
ORDERING INFORMATION



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