



3.3V CMOS 18-BIT BUS-INTERFACE FLIP-FLOP WITH 3-STATE OUTPUTS AND BUS-HOLD

IDT74ALVCH16823

FEATURES:

- 0.5 MICRON CMOS Technology
- Typical $t_{SK(0)}$ (Output Skew) < 250ps
- ESD > 2000V per MIL-STD-883, Method 3015;
> 200V using machine model (C = 200pF, R = 0)
- 0.635mm pitch SSOP, 0.50mm pitch TSSOP,
and 0.40mm pitch TVSOP packages
- Extended commercial range of -40°C to $+85^{\circ}\text{C}$
- $V_{CC} = 3.3\text{V} \pm 0.3\text{V}$, Normal Range
- $V_{CC} = 2.7\text{V}$ to 3.6V , Extended Range
- $V_{CC} = 2.5\text{V} \pm 0.2\text{V}$
- CMOS power levels (0.4μW typ. static)
- Rail-to-Rail output swing for increased noise margin

Drive Features for ALVCH16823:

- High Output Drivers: $\pm 24\text{mA}$
- Suitable for heavy loads

APPLICATIONS:

- 3.3V High Speed Systems
- 3.3V and lower voltage computing systems

DESCRIPTION:

This 18-bit bus-interface flip-flop is built using advanced dual metal CMOS technology. The ALVCH16823 features 3-state outputs designed specifically for driving highly capacitive or relatively low-impedance loads. The device is particularly suitable for implementing wider buffer

registers, I/O ports, bidirectional bus drivers with parity, and working registers.

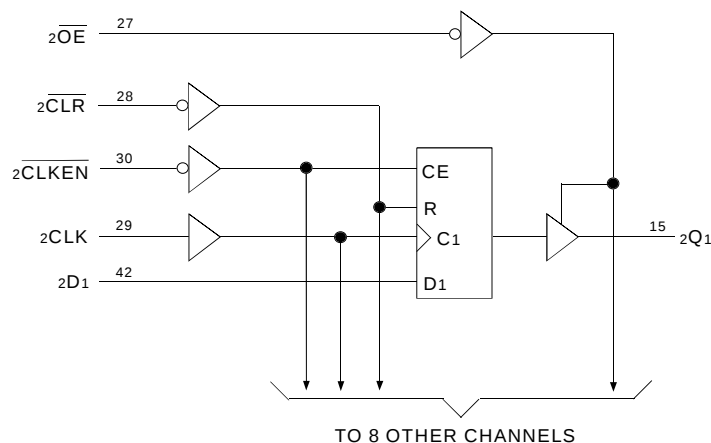
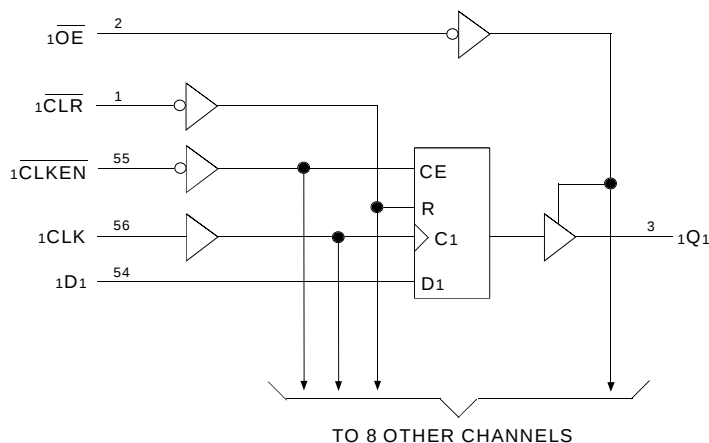
The ALVCH16823 can be used as two 9-bit flip-flops or one 18-bit flip-flop. With the clock-enable ($\overline{\text{CLKEN}}$) input low, the D-type flip-flops enter data on the low-to-high transitions of the clock. Taking $\overline{\text{CLKEN}}$ high disables the clock buffer, thus latching the outputs. Taking the clear ($\overline{\text{CLR}}$) input low causes the Q outputs to go low independently of the clock.

A buffered output-enable ($\overline{\text{OE}}$) input can be used to place the nine outputs in either a normal logic state (high or low logic levels) or a high-impedance state. In the high-impedance state, the outputs neither load nor drive the bus lines significantly. The high-impedance state and increased drive provide the capability to drive bus lines without need for interface or pullup components. The output-enable ($\overline{\text{OE}}$) input does not affect the internal operation of the flip-flops. Old data can be retained or new data can be entered while the outputs are in the high-impedance state.

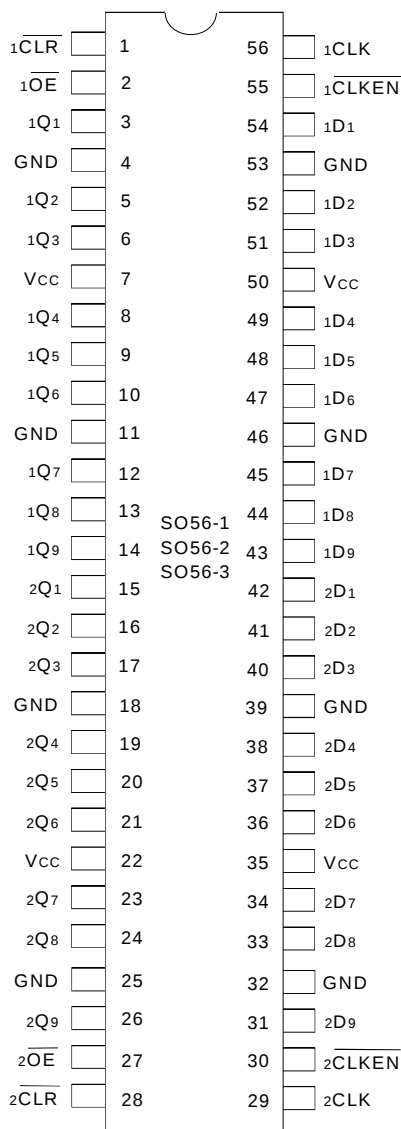
The ALVCH16823 has been designed with a $\pm 24\text{mA}$ output driver. This driver is capable of driving a moderate to heavy load while maintaining speed performance.

The ALVCH16823 has "bus-hold" which retains the inputs' last state whenever the input goes to a high impedance. This prevents floating inputs and eliminates the need for pull-up/down resistor.

Functional Block Diagram



PIN CONFIGURATION



SSOP/TSSOP/TVSOP
TOP VIEW

PIN DESCRIPTION

Pin Names	Description
xDx	Data Inputs ⁽¹⁾
xCLK	Clock Inputs
xCLKEN	Clock Enable Inputs
xQx	3-State Outputs
xOE	3-State Output Enable Inputs
xCLR	Clear Inputs

NOTE:

- These pins have "Bus-Hold." All other pins are standard inputs, outputs, or I/Os.

ABSOLUTE MAXIMUM RATING ⁽¹⁾

Symbol	Description	Max.	Unit
VTERM ⁽²⁾	Terminal Voltage with Respect to GND	– 0.5 to + 4.6	V
VTERM ⁽³⁾	Terminal Voltage with Respect to GND	– 0.5 to V _{CC} + 0.5	V
TSTG	Storage Temperature	– 65 to + 150	°C
IOUT	DC Output Current	– 50 to + 50	mA
I _{IK}	Continuous Clamp Current, V _I < 0 or V _I > V _{CC}	± 50	mA
I _{OK}	Continuous Clamp Current, V _O < 0	– 50	mA
I _{CC} I _{SS}	Continuous Current through each V _{CC} or GND	±100	mA

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NOTES:

- Stresses greater than those listed under ABSOLUTE MAXIMUM RATINGS may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect reliability.
- V_{CC} terminals.
- All terminals except V_{CC}.

CAPACITANCE (T_A = +25°C, f = 1.0MHz)

Symbol	Parameter ⁽¹⁾	Conditions	Typ.	Max.	Unit
C _{IN}	Input Capacitance	V _{IN} = 0V	5	7	pF
C _{OUT}	Output Capacitance	V _{OUT} = 0V	7	9	pF
C _{I/O}	I/O Port Capacitance	V _{IN} = 0V	7	9	pF

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NOTE:

- As applicable to the device type.

FUNCTION TABLE (each 9-bit flip-flop) ⁽¹⁾

Inputs					Output
xOE	xCLR	xCLKEN	xCLK	xDx	xQx
L	L	X	X	X	L
L	H	L	↑	H	H
L	H	L	↑	L	L
L	H	L	L	X	Q _o
L	H	H	X	X	Q _o
H	X	X	X	X	Z

NOTE:

- H = HIGH Voltage Level
L = LOW Voltage Level
X = Don't Care
Z = High-Impedance
↑ = LOW-to-HIGH Transition
Q_o = Indicates the previous state

DC ELECTRICAL CHARACTERISTICS OVER OPERATING RANGE

Following Conditions Apply Unless Otherwise Specified:

Operating Condition: TA = – 40°C to +85°C

Symbol	Parameter	Test Conditions		Min.	Typ. ⁽¹⁾	Max.	Unit
VIH	Input HIGH Voltage Level	VCC = 2.3V to 2.7V		1.7	—	—	V
		VCC = 2.7V to 3.6V		2	—	—	
VIL	Input LOW Voltage Level	VCC = 2.3V to 2.7V		—	—	0.7	V
		VCC = 2.7V to 3.6V		—	—	0.8	
IiH	Input HIGH Current	VCC = 3.6V	Vi = VCC	—	—	± 5	μA
IiL	Input LOW Current	VCC = 3.6V	Vi = GND	—	—	± 5	
IoZH IoZL	High Impedance Output Current (3-State Output pins)	VCC = 3.6V	Vo = VCC	—	—	± 10	μA
			Vo = GND	—	—	± 10	μA
VIK	Clamp Diode Voltage	VCC = 2.3V, IIN = – 18mA		—	– 0.7	– 1.2	V
VH	Input Hysteresis	VCC = 3.3V		—	100	—	mV
ICCL ICCH IC CZ	Quiescent Power Supply Current	VCC = 3.6V VIN = GND or VCC		—	0.1	40	μA
ΔIcc	Quiescent Power Supply Current Variation	One input at VCC – 0.6V, other inputs at VCC or GND		—	—	750	μA

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NOTE:

1. Typical values are at VCC = 3.3V, +25°C ambient.

BUS-HOLD CHARACTERISTICS

Symbol	Parameter ⁽¹⁾	Test Conditions		Min.	Typ. ⁽²⁾	Max.	Unit
IBHH IBHL	Bus-Hold Input Sustain Current	VCC = 3.0V	Vi = 2.0V	– 75	—	—	μA
			Vi = 0.8V	75	—	—	
IBHH IBHL	Bus-Hold Input Sustain Current	VCC = 2.3V	Vi = 1.7V	– 45	—	—	μA
			Vi = 0.7V	45	—	—	
IBHHO IBHLO	Bus-Hold Input Overdrive Current	VCC = 3.6V	Vi = 0 to 3.6V	—	—	± 500	μA

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NOTES:

1. Pins with Bus-hold are identified in the pin description.
2. Typical values are at VCC = 3.3V, +25°C ambient.

OUTPUT DRIVE CHARACTERISTICS

Symbol	Parameter	Test Conditions ⁽¹⁾		Min.	Max.	Unit
VOH	Output HIGH Voltage	VCC = 2.3V to 3.6V	IOH = – 0.1mA	VCC – 0.2	—	V
		VCC = 2.3V	IOH = – 6mA	2	—	
		VCC = 2.3V	IOH = – 12mA	1.7	—	
		VCC = 2.7V		2.2	—	
		VCC = 3.0V		2.4	—	
		VCC = 3.0V	IOH = – 24mA	2	—	
VOL	Output LOW Voltage	VCC = 2.3V to 3.6V	IOL = 0.1mA	—	0.2	V
		VCC = 2.3V	IOL = 6mA	—	0.4	
			IOL = 12mA	—	0.7	
		VCC = 2.7V	IOL = 12mA	—	0.4	
		VCC = 3.0V	IOL = 24mA	—	0.55	

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NOTE:

1. VIH and VIL must be within the min. or max. range shown in the DC ELECTRICAL CHARACTERISTICS OVER OPERATING RANGE table for the appropriate VCC range. TA = – 40°C to + 85°C.

OPERATING CHARACTERISTICS, TA = 25°C

Symbol	Parameter	Test Conditions	VCC = 2.5V ± 0.2V	VCC = 3.3V ± 0.3V	Unit
			Typical	Typical	
CPD	Power Dissipation Capacitance Outputs enabled	CL = 0pF, f = 10Mhz	27	30	pF
CPD	Power Dissipation Capacitance Outputs disabled		16	18	pF

SWITCHING CHARACTERISTICS ⁽¹⁾

Symbol	Parameter	V _{CC} = 2.5V ± 0.2V		V _{CC} = 2.7V		V _{CC} = 3.3V ± 0.3V		Unit
		Min.	Max.	Min.	Max.	Min.	Max.	
f _{MAX}		150	—	150	—	150	—	MHz
t _{PLH} t _{PHL}	Propagation Delay xCLK to xQx	1	5.8	—	5.2	1	4.5	ns
t _{PLH} t _{PHL}	Propagation Delay xCLR to xQx	1	5.4	—	5.2	1.2	4.6	ns
t _{PZH} t _{PZL}	Output Enable Time xOE to xQx	1	6	—	5.7	1	4.8	ns
t _{PHZ} t _{PLZ}	Output Disable Time xOE to xQx	1.1	5.4	—	4.7	1.3	4.5	ns
t _w	Pulse Width, xCLR LOW	3.3	—	3.3	—	3.3	—	ns
t _w	Pulse Width, xCLK HIGH or LOW	3.3	—	3.3	—	3.3	—	ns
t _{su}	Setup Time, xCLR inactive	0.7	—	0.7	—	0.8	—	ns
t _{su}	Setup Time, data LOW before xCLK↑	1.4	—	1.6	—	1.3	—	ns
t _{su}	Setup Time, data HIGH before xCLK↑	1.1	—	1.1	—	1	—	ns
t _{su}	Setup Time, xCLKEN LOW before xCLK↑	1.8	—	1.9	—	1.5	—	ns
t _h	Hold Time, data LOW after xCLK↑	0.4	—	0.5	—	0.5	—	ns
t _h	Hold Time, data HIGH after xCLK↑	0.7	—	0.1	—	0.8	—	ns
t _h	Hold Time, xCLKEN LOW after xCLK↑	0.2	—	0.3	—	0.4	—	ns
t _{sk(O)}	Output Skew ⁽²⁾	—	—	—	—	—	500	ps

NOTES:

1. See test circuits and waveforms. T_A = – 40°C to + 85°C.
2. Skew between any two outputs of the same package and switching in the same direction.

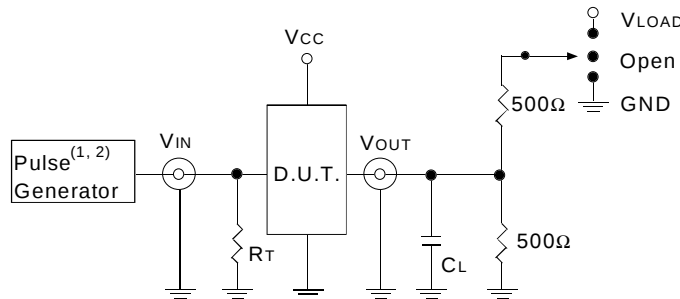
TEST CIRCUITS AND WAVEFORMS:

TEST CONDITIONS

Symbol	V _{CC} (1)= 3.3V±0.3V	V _{CC} (1)= 2.7V	V _{CC} (2)= 2.5V±0.2V	Unit
V _{LOAD}	6	6	2 x V _{CC}	V
V _{IH}	2.7	2.7	V _{CC}	V
V _T	1.5	1.5	V _{CC} / 2	V
V _{LZ}	300	300	150	mV
V _{HZ}	300	300	150	mV
C _L	50	50	30	pF

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TEST CIRCUITS FOR ALL OUTPUTS



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DEFINITIONS:

C_L = Load capacitance: includes jig and probe capacitance.

R_T = Termination resistance: should be equal to Z_{OUT} of the Pulse Generator.

NOTES:

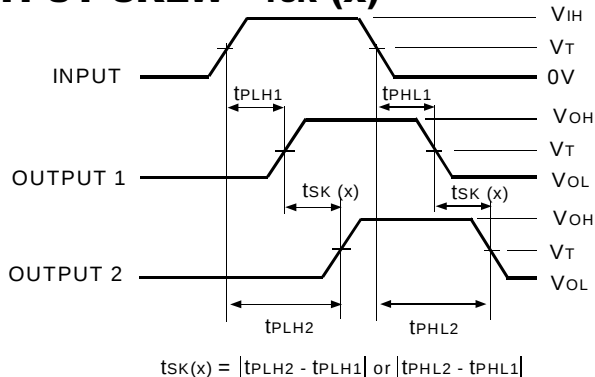
1. Pulse Generator for All Pulses: Rate ≤ 10MHz; t_r ≤ 2.5ns; t_r ≤ 2.5ns.
2. Pulse Generator for All Pulses: Rate ≤ 10MHz; t_r ≤ 2ns; t_r ≤ 2ns.

SWITCH POSITION

Test	Switch
Open Drain Disable Low Enable Low	V _{LOAD}
Disable High Enable High	GND
All Other tests	Open

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OUTPUT SKEW - t_{SK} (x)

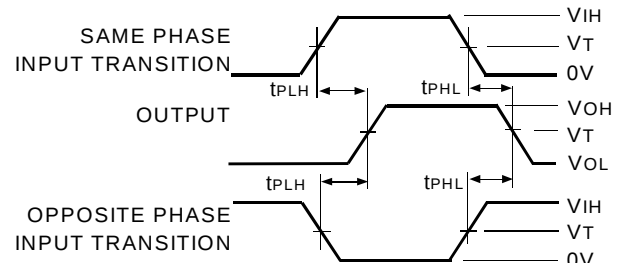


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NOTES:

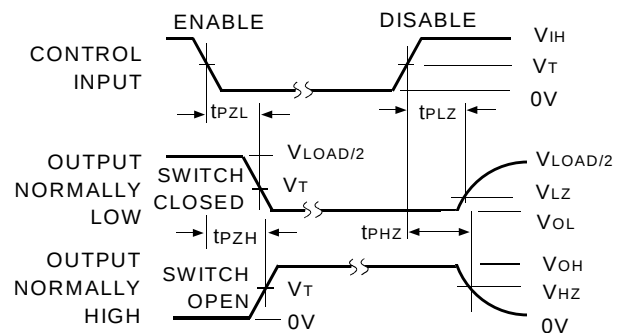
1. For t_{SK}(o) OUTPUT1 and OUTPUT2 are any two outputs.
2. For t_{SK}(b) OUTPUT1 and OUTPUT2 are in the same bank.

PROPAGATION DELAY



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ENABLE AND DISABLE TIMES

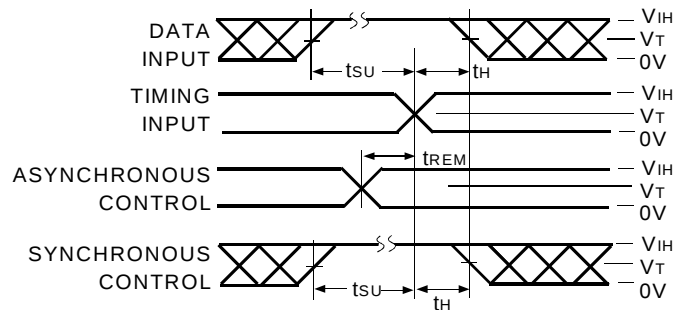


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NOTE:

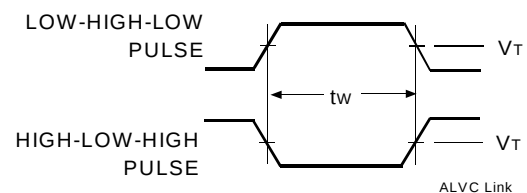
1. Diagram shown for input Control Enable-LOW and input Control Disable-HIGH.

SET-UP, HOLD, AND RELEASE TIMES



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PULSE WIDTH



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ORDERING INFORMATION

IDT	XX	ALVC	X	XXX	XXX	XX	
	Temp. Range		Bus-Hold	Family	Device Type	Package	
						PV	Shrink Small Outline Package (SO56-1)
						PA	Thin Shrink Small Outline Package (SO56-2)
						PF	Thin Very Small Outline Package (SO56-3)
					823		18-Bit Bus-Interface Flip-Flop with 3-State Outputs
				16			Double-Density with Resistors, $\pm 24\text{mA}$
			H				Bus-Hold
						74	-40°C to $+85^{\circ}\text{C}$



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