



## 3.3V CMOS 12-BIT TO 24-BIT REGISTERED BUS EXCHANGER WITH 3-STATE OUTPUTS AND BUS-HOLD

**IDT74ALVCH16269**

### FEATURES:

- 0.5 MICRON CMOS Technology
- Typical  $t_{SK(0)}$  (Output Skew) < 250ps
- ESD > 2000V per MIL-STD-883, Method 3015;  
> 200V using machine model (C = 200pF, R = 0)
- 0.635mm pitch SSOP, 0.50mm pitch TSSOP,  
and 0.40mm pitch TVSOP packages
- Extended commercial range of  $-40^{\circ}\text{C}$  to  $+85^{\circ}\text{C}$
- $V_{CC} = 3.3\text{V} \pm 0.3\text{V}$ , Normal Range
- $V_{CC} = 2.7\text{V}$  to  $3.6\text{V}$ , Extended Range
- $V_{CC} = 2.5\text{V} \pm 0.2\text{V}$
- CMOS power levels (0.4 $\mu\text{W}$  typ. static)
- Rail-to-Rail output swing for increased noise margin

### Drive Features for ALVCH16269:

- High Output Drivers:  $\pm 24\text{mA}$
- Suitable for heavy loads

### APPLICATIONS:

- 3.3V High Speed Systems
- 3.3V and lower voltage computing systems

### DESCRIPTION:

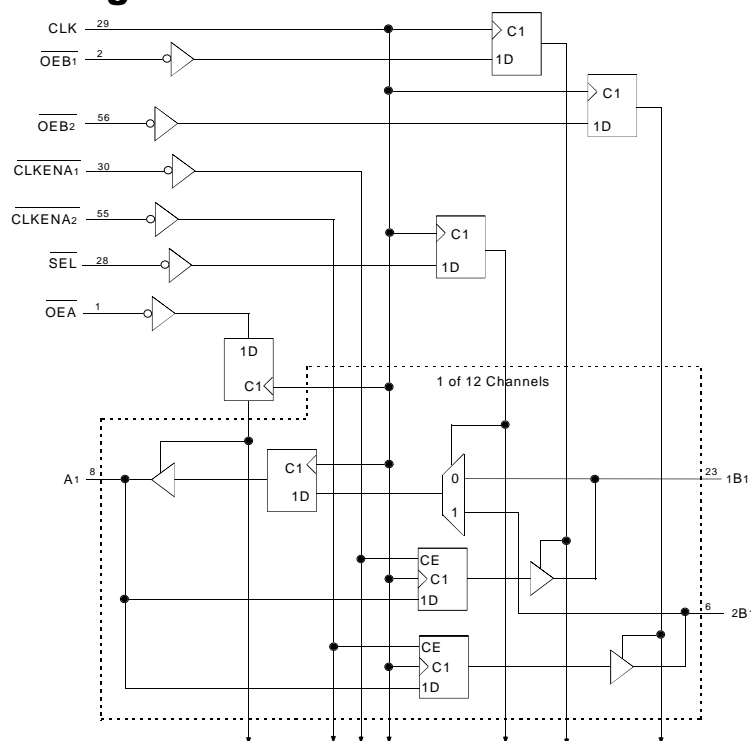
This 12-bit to 24-bit registered bus exchanger is used in applications in which two separate ports must be multiplexed onto, or demultiplexed from, a single port. It is particularly suitable as an interface between synchronous DRAMs and high-speed microprocessors.

Data is stored in the internal B-port registers on the low-to-high transition of the clock (CLK) input when the appropriate clock-enable ( $\overline{\text{CLKENA}}$ ) inputs are low. Proper control of these inputs allows two sequential 12-bit words to be presented as a 24-bit word on the B-port. For data transfer in the B-to-A direction, a single storage register is provided. The select SEL line selects 1B or 2B data for the A outputs. The register on the A output permits the fastest possible data transfer, thus extending the period during which the data is valid on the bus. The control terminals are registered so that all transactions are synchronous with CLK. Data flow is controlled by the active-low output enables ( $\overline{\text{OEA}}$ ,  $\overline{\text{OEB1}}$  and  $\overline{\text{OEB2}}$ ).

The ALVCH16269 has been designed with a  $\pm 24\text{mA}$  output driver. This driver is capable of driving a moderate to heavy load while maintaining speed performance.

The ALVCH16269 has "bus-hold" which retains the inputs' last state whenever the input goes to a high impedance. This prevents floating inputs and eliminates the need for pull-up/down resistors.

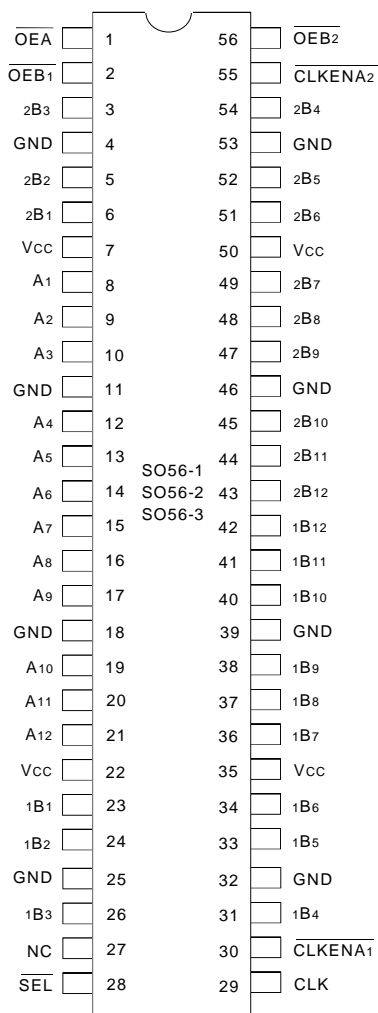
### Functional Block Diagram



**EXTENDED COMMERCIAL TEMPERATURE RANGE**

**MARCH 1999**

## PIN CONFIGURATION



SSOP/  
TSSOP/TVSOP  
TOP VIEW

## CAPACITANCE (T<sub>A</sub> = +25°C, f = 1.0MHz)

Symbol	Parameter <sup>(1)</sup>	Conditions	Typ.	Max.	Unit
C <sub>IN</sub>	Input Capacitance	V <sub>IN</sub> = 0V	5	7	pF
C <sub>OUT</sub>	Output Capacitance	V <sub>OUT</sub> = 0V	7	9	pF
C <sub>I/O</sub>	I/O Port Capacitance	V <sub>IN</sub> = 0V	7	9	pF

### NOTE:

- As applicable to the device type.

## ABSOLUTE MAXIMUM RATING <sup>(1)</sup>

Symbol	Description	Max.	Unit
V <sub>TERM</sub> <sup>(2)</sup>	Terminal Voltage with Respect to GND	- 0.5 to + 4.6	V
V <sub>TERM</sub> <sup>(3)</sup>	Terminal Voltage with Respect to GND	- 0.5 to V <sub>CC</sub> + 0.5	V
T <sub>STG</sub>	Storage Temperature	- 65 to + 150	°C
I <sub>OUT</sub>	DC Output Current	- 50 to + 50	mA
I <sub>IK</sub>	Continuous Clamp Current, V <sub>I</sub> < 0 or V <sub>I</sub> > V <sub>CC</sub>	± 50	mA
I <sub>OK</sub>	Continuous Clamp Current, V <sub>O</sub> < 0	- 50	mA
I <sub>CC</sub>	Continuous Current through each V <sub>CC</sub> or GND	± 100	mA

NEW16link

### NOTES:

- Stresses greater than those listed under ABSOLUTE MAXIMUM RATINGS may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect reliability.
- V<sub>CC</sub> terminals.
- All terminals except V<sub>CC</sub>.

## FUNCTION TABLE<sup>(1)</sup> OUTPUT ENABLE

Inputs			Outputs	
CLK	OEA	OEB <sub>x</sub>	A <sub>x</sub>	1B <sub>x</sub> , 2B <sub>x</sub>
↑	H	H	Z	Z
↑	H	L	Z	Active
↑	L	H	Active	Z
↑	L	L	Active	Active

## A-TO-B STORAGE (OEB = L)

Inputs			Outputs		
CLKENA <sub>1</sub>	CLKENA <sub>2</sub>	CLK	A <sub>x</sub>	1B <sub>x</sub> <sup>(2)</sup>	2B <sub>x</sub> <sup>(2)</sup>
H	H	X	X	1B <sub>0</sub> <sup>(2)</sup>	2B <sub>0</sub> <sup>(2)</sup>
L	X	↑	L	L	X
L	X	↑	H	H	X
X	L	↑	L	X	L
X	L	↑	H	X	H

## B-TO-A STORAGE (OEA = L)

Inputs				Outputs
CLK	SEL	1B <sub>x</sub>	2B <sub>x</sub>	A <sub>x</sub>
X	H	X	X	A <sub>0</sub> <sup>(2)</sup>
X	L	X	X	A <sub>0</sub> <sup>(2)</sup>
↑	H	L	X	L
↑	H	H	X	H
↑	L	X	L	L
↑	L	X	H	H

### NOTES:

- H = HIGH Voltage Level  
L = LOW Voltage Level  
X = Don't Care  
Z = High-Impedance  
↑ = LOW-to-HIGH Transition
- Output level before the indicated steady-state input conditions were established.

## PIN DESCRIPTION

Pin Names	I/O	Description
Ax(1:12)	I/O	Bidirectional Data Port A. Usually connected to the CPU's Address/Data bus. <sup>(1)</sup>
1Bx(1:12)	I/O	Bidirectional Data Port 1B. Usually connected to the even path or even bank of memory. <sup>(1)</sup>
2Bx(1:12)	I/O	Bidirectional Data Port 2B. Usually connected to the odd path or odd bank of memory. <sup>(1)</sup>
CLK	I	Clock Input
CLKENA1	I	Clock Enable Input for the A-1B Register. If $\overline{\text{CLKENA1}}$ is LOW during the rising edge of CLK, data will be clocked into register A-1B (Active LOW).
CLKENA2	I	Clock Enable Input for the A-2B Register. If $\overline{\text{CLKENA2}}$ is LOW during the rising edge of CLK, data will be clocked into register A-2B (Active LOW).
SEL	I	1B or 2B Port Selection. When HIGH during the rising edge of CLK, $\overline{\text{SEL}}$ enables data transfer from 1B Port to A Port. When LOW during the rising edge of CLK, $\overline{\text{SEL}}$ enables data transfer from 2B Port to A Port.
$\overline{\text{OEA}}$	I	Synchronous Output Enable for A Port (Active LOW)
$\overline{\text{OEB1}}$	I	Synchronous Output Enable for 1B Port (Active LOW)
$\overline{\text{OEB2}}$	I	Synchronous Output Enable for 2B Port (Active LOW)

### NOTE:

- These pins have "Bus-Hold." All other pins are standard inputs, outputs, or I/Os.

## DC ELECTRICAL CHARACTERISTICS OVER OPERATING RANGE

Following Conditions Apply Unless Otherwise Specified:

Operating Condition: TA = - 40°C to +85°C

Symbol	Parameter	Test Conditions	Min.	Typ. <sup>(1)</sup>	Max.	Unit
VIH	Input HIGH Voltage Level	VCC = 2.3V to 2.7V	1.7	—	—	V
		VCC = 2.7V to 3.6V	2	—	—	
VIL	Input LOW Voltage Level	VCC = 2.3V to 2.7V	—	—	0.7	V
		VCC = 2.7V to 3.6V	—	—	0.8	
IiH	Input HIGH Current	VCC = 3.6V VI = VCC	—	—	± 5	μA
IiL	Input LOW Current	VCC = 3.6V VI = GND	—	—	± 5	
IozH	High Impedance Output Current (3-State Output pins)	VCC = 3.6V VO = VCC	—	—	± 10	μA
IozL		VCC = 3.6V VO = GND	—	—	± 10	μA
Vik	Clamp Diode Voltage	VCC = 2.3V, IIN = - 18mA	—	- 0.7	- 1.2	V
VH	Input Hysteresis	VCC = 3.3V	—	100	—	mV
IcCL IcCH IcCZ	Quiescent Power Supply Current	VCC = 3.6V VIN = GND or VCC	—	0.1	40	μA
ΔIcc	Quiescent Power Supply Current Variation	One input at VCC - 0.6V, other inputs at VCC or GND	—	—	750	μA

NEW16link

### NOTE:

- Typical values are at VCC = 3.3V, +25°C ambient.

**BUS-HOLD CHARACTERISTICS**

Symbol	Parameter <sup>(1)</sup>	Test Conditions		Min.	Typ. <sup>(2)</sup>	Max.	Unit
IBHH IBHL	Bus-Hold Input Sustain Current	V <sub>CC</sub> = 3.0V	V <sub>I</sub> = 2.0V	– 75	—	—	μA
			V <sub>I</sub> = 0.8V	75	—	—	
IBHH IBHL	Bus-Hold Input Sustain Current	V <sub>CC</sub> = 2.3V	V <sub>I</sub> = 1.7V	– 45	—	—	μA
			V <sub>I</sub> = 0.7V	45	—	—	
IBHHO IBHLO	Bus-Hold Input Overdrive Current	V <sub>CC</sub> = 3.6V	V <sub>I</sub> = 0 to 3.6V	—	—	± 500	μA

NEW16link

**NOTES:**

1. Pins with Bus-hold are identified in the pin description.
2. Typical values are at V<sub>CC</sub> = 3.3V, +25°C ambient.

**OUTPUT DRIVE CHARACTERISTICS**

Symbol	Parameter	Test Conditions <sup>(1)</sup>		Min.	Max.	Unit
VOH	Output HIGH Voltage	V <sub>CC</sub> = 2.3V to 3.6V	I <sub>OH</sub> = – 0.1mA	V <sub>CC</sub> – 0.2	—	V
		V <sub>CC</sub> = 2.3V	I <sub>OH</sub> = – 6mA	2	—	
		V <sub>CC</sub> = 2.3V	I <sub>OH</sub> = – 12mA	1.7	—	
		V <sub>CC</sub> = 2.7V		2.2	—	
		V <sub>CC</sub> = 3.0V		2.4	—	
		V <sub>CC</sub> = 3.0V	I <sub>OH</sub> = – 24mA	2	—	
VOL	Output LOW Voltage	V <sub>CC</sub> = 2.3V to 3.6V	I <sub>OL</sub> = 0.1mA	—	0.2	V
		V <sub>CC</sub> = 2.3V	I <sub>OL</sub> = 6mA	—	0.4	
			I <sub>OL</sub> = 12mA	—	0.7	
		V <sub>CC</sub> = 2.7V	I <sub>OL</sub> = 12mA	—	0.4	
		V <sub>CC</sub> = 3.0V	I <sub>OL</sub> = 24mA	—	0.55	

NEW16link

**NOTE:**

1. V<sub>IH</sub> and V<sub>IL</sub> must be within the min. or max. range shown in the DC ELECTRICAL CHARACTERISTICS OVER OPERATING RANGE table for the appropriate V<sub>CC</sub> range. T<sub>A</sub> = – 40°C to + 85°C.

**OPERATING CHARACTERISTICS, T<sub>A</sub> = 25°C**

Symbol	Parameter	Test Conditions	V <sub>CC</sub> = 2.5V ± 0.2V	V <sub>CC</sub> = 3.3V ± 0.3V	Unit
			Typical	Typical	
CPD	Power Dissipation Capacitance per exchanger Outputs enabled	C <sub>L</sub> = 0pF, f = 10Mhz	87	120	pF
CPD	Power Dissipation Capacitance per exchanger Outputs disabled		80.5	118	pF

**SWITCHING CHARACTERISTICS (1)**

Symbol	Parameter	V <sub>CC</sub> = 2.5V ± 0.2V		V <sub>CC</sub> = 2.7V		V <sub>CC</sub> = 3.3V ± 0.3V		Unit
		Min.	Max.	Min.	Max.	Min.	Max.	
f <sub>MAX</sub>		135	—	135	—	135	—	MHz
t <sub>PLH</sub> t <sub>PHL</sub>	Propagation Delay CLK to xBx	1	8.2	—	7.3	1	6.2	ns
t <sub>PLH</sub> t <sub>PHL</sub>	Propagation Delay CLK to Ax	1	6.4	—	5.8	1	5	ns
t <sub>PZH</sub> t <sub>PZL</sub>	Output Enable Time Synchronous $\overline{OE}B$ : CLK to xBx	1	7.9	—	6.7	1	6.1	ns
t <sub>PZH</sub> t <sub>PZL</sub>	Output Enable Time Synchronous $\overline{OE}A$ : CLK to Ax	1	7.6	—	6.2	1	5.9	ns
t <sub>PHZ</sub> t <sub>PLZ</sub>	Output Disable Time Synchronous $\overline{OE}B$ : CLK to xBx	1	8.1	—	6.9	1	6.1	ns
t <sub>PHZ</sub> t <sub>PLZ</sub>	Output Disable Time Synchronous $\overline{OE}A$ : CLK to Ax	1	7.5	—	6.8	1	5.6	ns
t <sub>su</sub>	Setup Time, Ax data before CLK↑	2	—	2	—	1.7	—	ns
t <sub>su</sub>	Setup Time, Bx data before CLK↑	2.2	—	2.1	—	1.8	—	ns
t <sub>su</sub>	Setup Time, $\overline{SEL}$ before CLK↑	1.6	—	1.6	—	1.3	—	ns
t <sub>su</sub>	Setup Time, $\overline{CLKENA1}$ or $\overline{CLKENA2}$ before CLK↑	1	—	1.2	—	0.9	—	ns
t <sub>su</sub>	Setup Time, $\overline{OE}$ before CLK↑	1.5	—	1.6	—	1.3	—	ns
t <sub>h</sub>	Hold Time, Ax data after CLK↑	0.7	—	0.6	—	0.6	—	ns
t <sub>h</sub>	Hold Time, Bx data after CLK↑	0.7	—	0.6	—	0.6	—	ns
t <sub>h</sub>	Hold Time, $\overline{SEL}$ after CLK↑	1.1	—	0.7	—	0.7	—	ns
t <sub>h</sub>	Hold Time, $\overline{CLKENA1}$ or $\overline{CLKENA2}$ after CLK↑	1	—	0.8	—	1.1	—	ns
t <sub>h</sub>	Hold Time, $\overline{OE}$ after CLK↑	0.8	—	0.8	—	0.8	—	ns
t <sub>w</sub>	Pulse Width, CLK HIGH or LOW	3.3	—	3.3	—	3.3	—	ns
t <sub>sk(o)</sub>	Output Skew <sup>(2)</sup>	—	—	—	—	—	500	ps

**NOTES:**

1. See test circuits and waveforms. T<sub>A</sub> = –40°C to +85°C.
2. Skew between any two outputs of the same package and switching in the same direction.

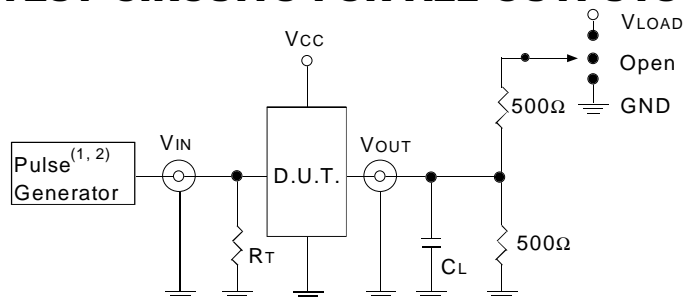
## TEST CIRCUITS AND WAVEFORMS

### TEST CONDITIONS

Symbol	V <sub>CC</sub> (1)= 3.3V±0.3V	V <sub>CC</sub> (1)= 2.7V	V <sub>CC</sub> (2)= 2.5V±0.2V	Unit
V <sub>LOAD</sub>	6	6	2 x V <sub>CC</sub>	V
V <sub>IH</sub>	2.7	2.7	V <sub>CC</sub>	V
V <sub>T</sub>	1.5	1.5	V <sub>CC</sub> / 2	V
V <sub>LZ</sub>	300	300	150	mV
V <sub>HZ</sub>	300	300	150	mV
C <sub>L</sub>	50	50	30	pF

NEW16link

### TEST CIRCUITS FOR ALL OUTPUTS



ALVC Link

#### DEFINITIONS:

C<sub>L</sub>= Load capacitance: includes jig and probe capacitance.

R<sub>T</sub>= Termination resistance: should be equal to Z<sub>OUT</sub> of the Pulse Generator.

#### NOTES:

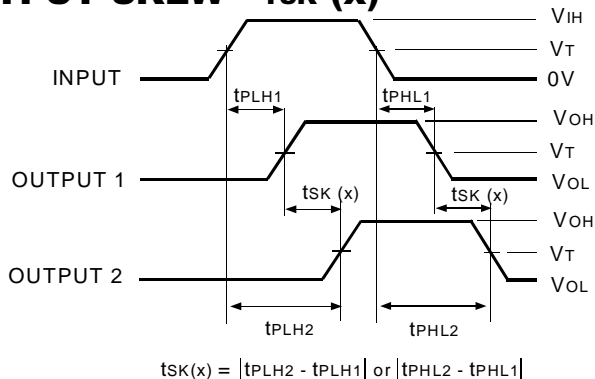
1. Pulse Generator for All Pulses: Rate ≤ 10MHz; t<sub>F</sub> ≤ 2.5ns; t<sub>R</sub> ≤ 2.5ns.
2. Pulse Generator for All Pulses: Rate ≤ 10MHz; t<sub>F</sub> ≤ 2ns; t<sub>R</sub> ≤ 2ns.

### SWITCH POSITION

Test	Switch
Open Drain Disable Low Enable Low	V <sub>LOAD</sub>
Disable High Enable High	GND
All Other tests	Open

NEW16link

### OUTPUT SKEW - t<sub>SK</sub> (x)



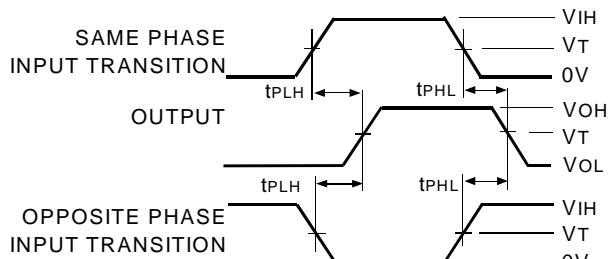
$$t_{SK}(x) = |t_{PLH2} - t_{PLH1}| \text{ or } |t_{PHL2} - t_{PHL1}|$$

ALVC Link

#### NOTES:

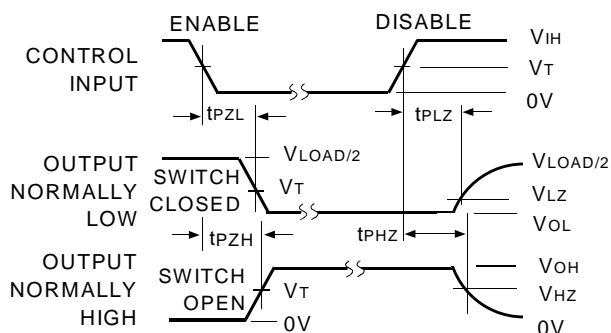
1. For t<sub>SK</sub>(o) OUTPUT1 and OUTPUT2 are any two outputs.
2. For t<sub>SK</sub>(b) OUTPUT1 and OUTPUT2 are in the same bank.

### PROPAGATION DELAY



ALVC Link

### ENABLE AND DISABLE TIMES

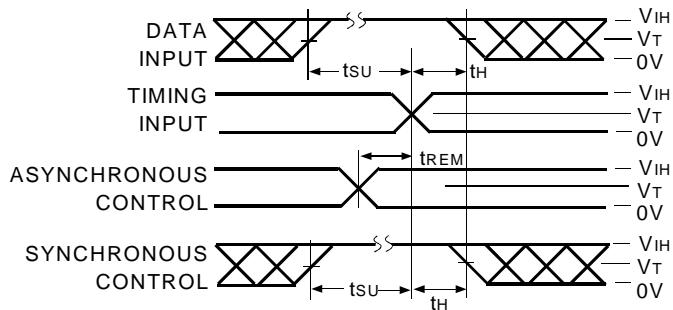


ALVC Link

#### NOTE:

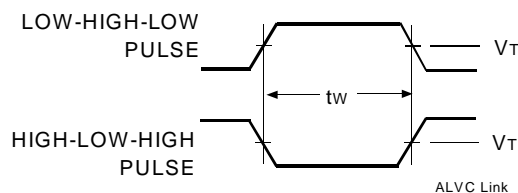
1. Diagram shown for input Control Enable-LOW and input Control Disable-HIGH.

### SET-UP, HOLD, AND RELEASE TIMES



ALVC Link

### PULSE WIDTH



ALVC Link

## ORDERING INFORMATION

IDT	XX	ALVC	X	XX	XXX	XX	
Temp. Range			Bus-Hold	Family	Device Type	Package	
						PV	Shrink Small Outline Package (SO56-1)
						PA	Thin Shrink Small Outline Package (SO56-2)
						PF	Thin Very Small Outline Package (SO56-3)
					269		12-Bit to 24-Bit Registered Bus Exchanger with 3-State Outputs
				16			Double-Density with Resistors, $\pm 24\text{mA}$
			H				Bus-Hold
						74	$-40^{\circ}\text{C}$ to $+85^{\circ}\text{C}$



**CORPORATE HEADQUARTERS**  
 2975 Stender Way  
 Santa Clara, CA 95054

**for SALES:**  
 800-345-7015 or 408-727-6116  
 fax: 408-492-8674  
[www.idt.com](http://www.idt.com)\*

\*To search for sales office near you, please click the sales button found on our home page or dial the 800# above and press 2.  
 The IDT logo is a registered trademark of Integrated Device Technology, Inc.