3.3V CMOS 16-BIT TRANSPARENT D-TYPE LATCH WITH 3-STATE OUTPUTS AND BUS-HOLD

IDT74ALVCH162373

FEATURES:

- 0.5 MICRON CMOS Technology
- Typical $t_{SK(0)}$ (Output Skew) < 250ps
- ESD > 2000V per MIL-STD-883, Method 3015; > 200V using machine model (C = 200pF, R = 0)
- 0.635mm pitch SSOP, 0.50mm pitch TSSOP, and 0.40mm pitch TVSOP packages
- Extended commercial range of – 40°C to + 85°C
- V_{CC} = 3.3V ± 0.3V, Normal Range
- V_{CC} = 2.7V to 3.6V, Extended Range
- V_{CC} = 2.5V ± 0.2V
- CMOS power levels (0.4µW typ. static)
- Rail-to-Rail output swing for increased noise margin

Drive Features for ALVCH162373:

- Balanced Output Drivers: ±12mA
- Low switching noise

APPLICATIONS:

- 3.3V High Speed Systems
- 3.3V and lower voltage computing systems

DESCRIPTION:

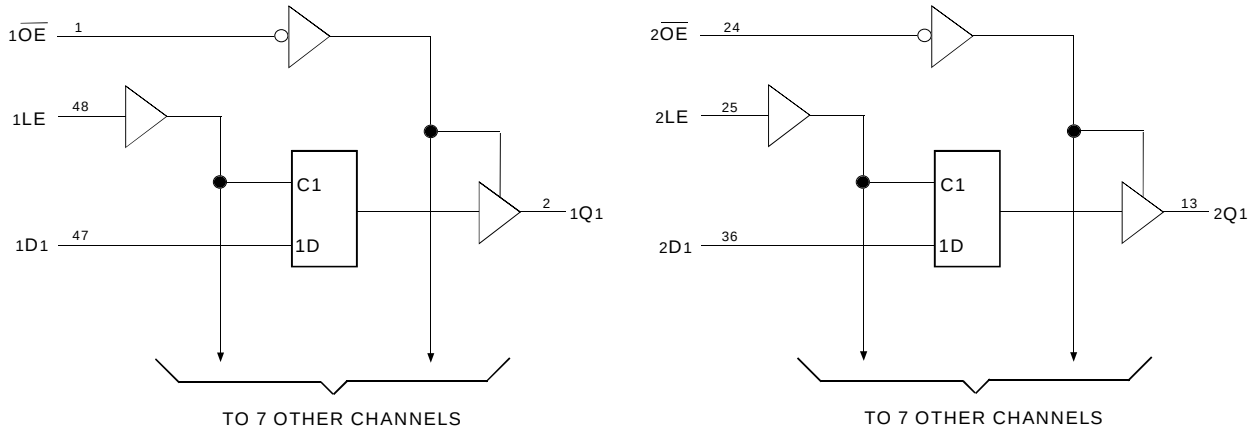
This 16-bit transparent D-type latch is built using advanced dual metal CMOS technology. The ALVCH162373 is particularly suitable for implementing buffer registers, I/O ports, bidirectional bus drivers, and working registers. This device can be used as two 8-bit latches or one16-bit latch. When the latch enable (LE) input is high, the Q outputs follow the data (D) inputs. When LE is taken low, the Q outputs are latched at the levels set up at the D inputs.

A buffered output-enable ($\overline{OE}$) can be used to place the eight outputs in either a normal logic state (high or low logic levels) or a high-impedance state. In the high-impedance state, the outputs neither load nor drive the bus lines significantly. The high-impedance state and the increased drive provide the capability to drive bus lines without need for interface or pullup components. $\overline{OE}$ does not affect internal operations of the latch. Old data can be retained or new data can be enetered while the outputs are in the high-impedance state.

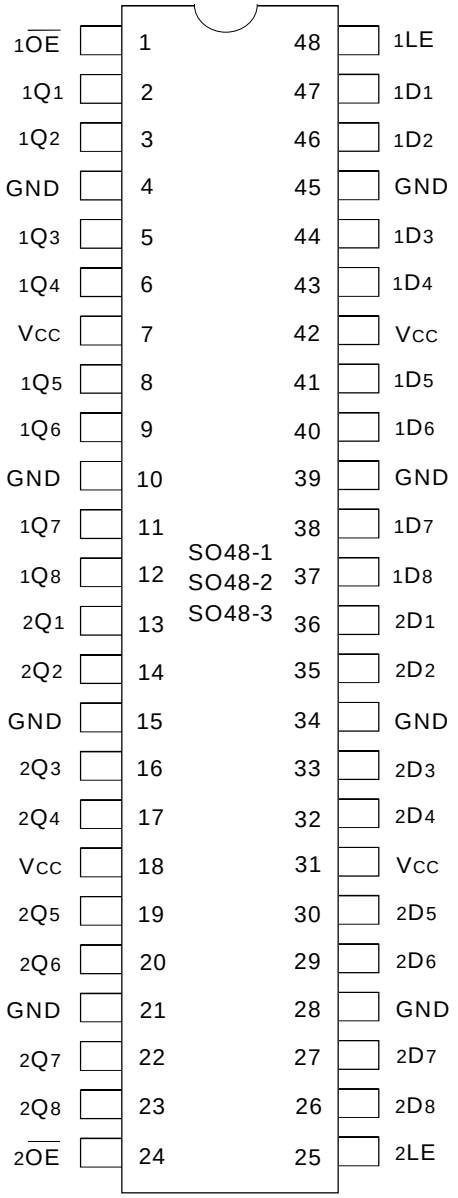
The ALVCH162373 has series resistors in the device output structure which will significantly reduce line noise when used with light loads. This driver has been designed to drive ±12mA at the designated threshold levels.

The ALVCH162373 has "bus-hold" which retains the inputs' last state whenever the input goes to a high impedance. This prevents floating inputs and eliminates the need for pull-up/down resistor.

Functional Block Diagram



PIN CONFIGURATION



SSOP/
TSSOP/TVSOP
TOP VIEW

PIN DESCRIPTION

Pin Names	Description
xDx	Data Inputs(1)
xLE	Latch Enable Inputs
xQx	3-State Outputs
x$\overline{OE}$	3-State Output Enable Input (Active LOW)

NOTE:
1. These pins have "Bus-Hold." All other pins are standard inputs, outputs, or I/Os.

ABSOLUTE MAXIMUM RATING (1)

Symbol	Description	Max.	Unit
V_{TERM}(2)	Terminal Voltage with Respect to GND	– 0.5 to + 4.6	V
V_{TERM}(3)	Terminal Voltage with Respect to GND	– 0.5 to V_{CC} + 0.5	V
T_{STG}	Storage Temperature	– 65 to + 150	°C
I_{OUT}	DC Output Current	– 50 to + 50	mA
I_{IK}	Continuous Clamp Current, $V_I < 0$ or $V_I > V_{CC}$	± 50	mA
I_{OK}	Continuous Clamp Current, $V_O < 0$	– 50	mA
I_{CC} I_{SS}	Continuous Current through each V_{CC} or GND	±100	mA

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NOTES:
1. Stresses greater than those listed under ABSOLUTE MAXIMUM RATINGS may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect reliability.
2. V_{CC} terminals.
3. All terminals except V_{CC}.

CAPACITANCE (T_A = +25°C, f = 1.0MHz)

Symbol	Parameter(1)	Conditions	Typ.	Max.	Unit
C_{IN}	Input Capacitance	V_{IN} = 0V	5	7	pF
C_{OUT}	Output Capacitance	V_{OUT} = 0V	7	9	pF
$C_{I/O}$	I/O Port Capacitance	V_{IN} = 0V	7	9	pF

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NOTE:
1. As applicable to the device type.

FUNCTION TABLE (each 8-bit section)(1)

Inputs			Outputs
x$\overline{OE}$	xLE	xDx	xQx
L	H	H	H
L	H	L	L
H	X	X	Z
L	L	X	Q_O

NOTE:
1. H = HIGH Voltage Level
   L = LOW Voltage Level
   X = Don't Care
   Z = High-Impedance
   Q_O = Level of Q before the indicated steady-state input conditions were established

DC ELECTRICAL CHARACTERISTICS OVER OPERATING RANGE

Following Conditions Apply Unless Otherwise Specified:

Operating Condition: TA = – 40°C to +85°C

Symbol	Parameter	Test Conditions		Min.	Typ.(1)	Max.	Unit
V_{IH}	Input HIGH Voltage Level	V_{CC} = 2.3V to 2.7V		1.7	—	—	V
		V_{CC} = 2.7V to 3.6V		2	—	—	
V_{IL}	Input LOW Voltage Level	V_{CC} = 2.3V to 2.7V		—	—	0.7	V
		V_{CC} = 2.7V to 3.6V		—	—	0.8	
I_{IH}	Input HIGH Current	V_{CC} = 3.6V	V_I = V_{CC}	—	—	± 5	µA
I_{IL}	Input LOW Current	V_{CC} = 3.6V	V_I = GND	—	—	± 5	
I_{OZH}	High Impedance Output Current	V_{CC} = 3.6V	V_O = V_{CC}	—	—	± 10	µA
I_{OZL}	(3-State Output pins)		V_O = GND	—	—	± 10	µA
V_{IK}	Clamp Diode Voltage	V_{CC} = 2.3V, I_{IN} = – 18mA		—	– 0.7	– 1.2	V
V_H	Input Hysteresis	V_{CC} = 3.3V		—	100	—	mV
I_{CCL} I_{CCH} I_{CCZ}	Quiescent Power Supply Current	V_{CC} = 3.6V V_{IN} = GND or V_{CC}		—	0.1	40	µA
ΔI_{CC}	Quiescent Power Supply Current Variation	One input at V_{CC} – 0.6V, other inputs at V_{CC} or GND		—	—	750	µA

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NOTE:
1. Typical values are at V_{CC} = 3.3V, +25°C ambient.

BUS-HOLD CHARACTERISTICS

Symbol	Parameter(1)	Test Conditions		Min.	Typ.(2)	Max.	Unit
I_{BHH}	Bus-Hold Input Sustain Current	V_{CC} = 3.0V	V_I = 2.0V	– 75	—	—	µA
I_{BHL}			V_I = 0.8V	75	—	—	
I_{BHH}	Bus-Hold Input Sustain Current	V_{CC} = 2.3V	V_I = 1.7V	– 45	—	—	µA
I_{BHL}			V_I = 0.7V	45	—	—	
I_{BHHO}	Bus-Hold Input Overdrive Current	V_{CC} = 3.6V	V_I = 0 to 3.6V	—	—	± 500	µA
I_{BHLO}							

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NOTES:
1. Pins with Bus-hold are identified in the pin description.
2. Typical values are at V_{CC} = 3.3V, +25°C ambient.

OUTPUT DRIVE CHARACTERISTICS

Symbol	Parameter	Test Conditions[1]		Min.	Max.	Unit
V_{OH}	Output HIGH Voltage	V_{CC} = 2.3V to 3.6V	I_{OH} = – 0.1mA	V_{CC} – 0.2	—	V
		V_{CC} = 2.3V	I_{OH} = – 4mA	1.9	—	
			I_{OH} = – 6mA	1.7	—	
		V_{CC} = 2.7V	I_{OH} = – 4mA	2.2	—	
			I_{OH} = – 8mA	2	—	
		V_{CC} = 3.0V	I_{OH} = – 6mA	2.4	—	
			I_{OH} = – 12mA	2	—	
V_{OL}	Output LOW Voltage	V_{CC} = 2.3V to 3.6V	I_{OL} = 0.1mA	—	0.2	V
		V_{CC} = 2.3V	I_{OL} = 4mA	—	0.4	
			I_{OL} = 6mA	—	0.55	
		V_{CC} = 2.7V	I_{OL} = 4mA	—	0.4	
			I_{OL} = 8mA	—	0.6	
		V_{CC} = 3.0V	I_{OL} = 6mA	—	0.55	
			I_{OL} = 12mA	—	0.8	

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NOTE:

1. V_{IH} and V_{IL} must be within the min. or max. range shown in the DC ELECTRICAL CHARACTERISTICS OVER OPERATING RANGE table for the appropriate V_{CC} range. T_A = – 40°C to + 85°C.

OPERATING CHARACTERISTICS, T_A = 25°C

Symbol	Parameter	Test Conditions	Vcc = 2.5V ± 0.2V Typical	Vcc = 3.3V ± 0.3V Typical	Unit
C_{PD}	Power Dissipation Capacitance Outputs enabled	C_L = 0pF, f = 10Mhz	19	22	pF
C_{PD}	Power Dissipation Capacitance Outputs disabled		4	5	pF

SWITCHING CHARACTERISTICS [1]

Symbol	Parameter	Vcc = 2.5V ± 0.2V		Vcc = 2.7V		Vcc = 3.3V ± 0.3V		Unit
		Min.	Max.	Min.	Max.	Min.	Max.	
t_{PLH} t_{PHL}	Propagation Delay xDx to xQx	1.5	5.3	1.5	4.5	1.5	4	ns
t_{PLH} t_{PHL}	Propagation Delay xLE to xQx	2	5.6	2	5	2	4	ns
t_{PZH} t_{PZL}	Output Enable Time $x\overline{OE}$ to xQx	1.5	6.5	1.5	6	1.5	5	ns
t_{PHZ} t_{PLZ}	Output Disable Time $x\overline{OE}$ to xQx	1.5	5.6	1.5	5.5	1.5	4.5	ns
t_{SU}	Setup Time, data before LE↓	2	—	2	—	2	—	ns
t_H	Hold Time, data after LE↓	1.5	—	1.5	—	1.5	—	ns
t_W	Pulse Duration, LE HIGH or LOW	3.3	—	3.3	—	3.3	—	ns
$t_{SK}(o)$	Output Skew[2]	—	—	—	—	—	500	ps

NOTES:

1. See test circuits and waveforms. T_A = – 40°C to + 85°C.
2. Skew between any two outputs of the same package and switching in the same direction.

TEST CIRCUITS AND WAVEFORMS:

TEST CONDITIONS

Symbol	$V_{CC}^{(1)}$= 3.3V±0.3V	$V_{CC}^{(1)}$= 2.7V	$V_{CC}^{(2)}$= 2.5V±0.2V	Unit
V_{LOAD}	6	6	2 x Vcc	V
V_{IH}	2.7	2.7	Vcc	V
V_T	1.5	1.5	Vcc / 2	V
V_{LZ}	300	300	150	mV
V_{HZ}	300	300	150	mV
C_L	50	50	30	pF

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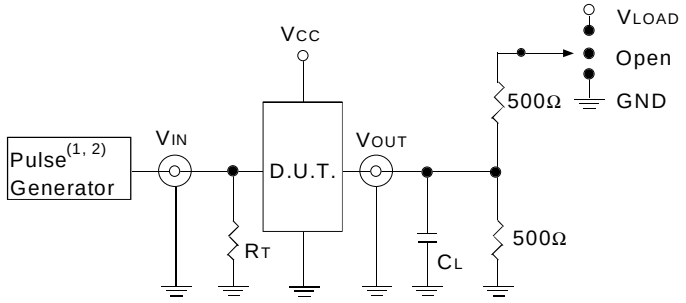
TEST CIRCUITS FOR ALL OUTPUTS



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DEFINITIONS:

C_L= Load capacitance: includes jig and probe capacitance.
R_T = Termination resistance: should be equal to Z_{OUT} of the Pulse Generator.

NOTES:

1. Pulse Generator for All Pulses: Rate ≤ 10MHz; t_F ≤ 2.5ns; t_R ≤ 2.5ns.
2. Pulse Generator for All Pulses: Rate ≤ 10MHz; t_F ≤ 2ns; t_R ≤ 2ns.

SWITCH POSITION

Test	Switch
Open Drain Disable Low Enable Low	V_{LOAD}
Disable High Enable High	GND
All Other tests	Open

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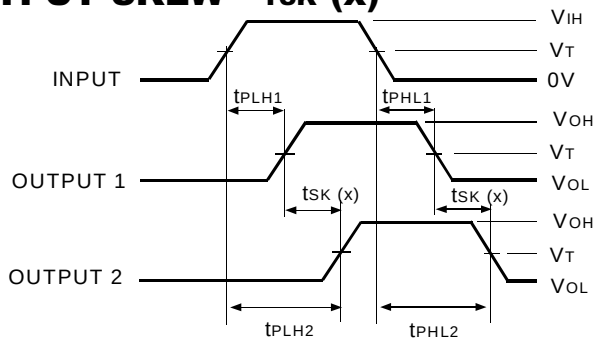
OUTPUT SKEW - t_{SK} (x)



$t_{SK(x)} = |t_{PLH2} - t_{PLH1}|$ or $|t_{PHL2} - t_{PHL1}|$

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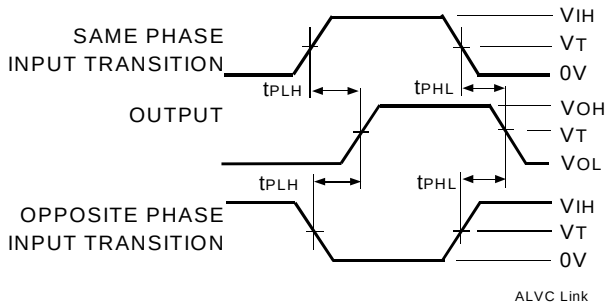
NOTES:

1. For t_{SK}(o) OUTPUT1 and OUTPUT2 are any two outputs.
2. For t_{SK}(b) OUTPUT1 and OUTPUT2 are in the same bank.

PROPAGATION DELAY



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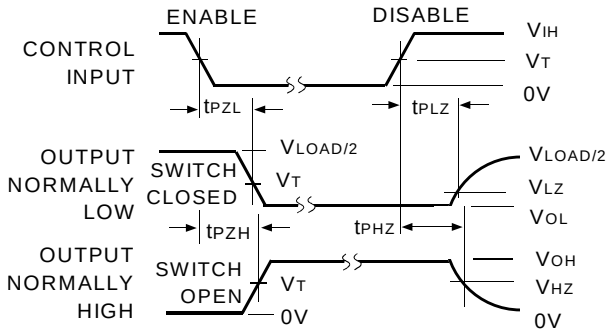
ENABLE AND DISABLE TIMES



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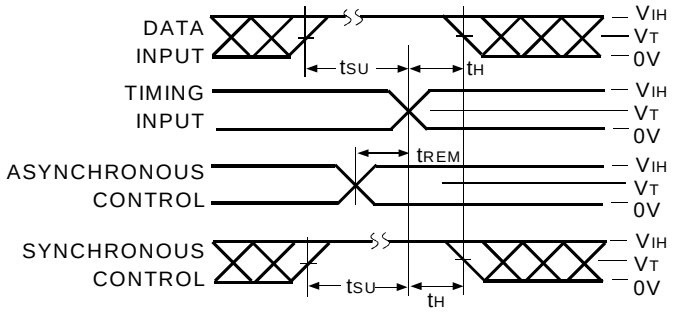
NOTE:

1. Diagram shown for input Control Enable-LOW and input Control Disable-HIGH.

SET-UP, HOLD, AND RELEASE TIMES



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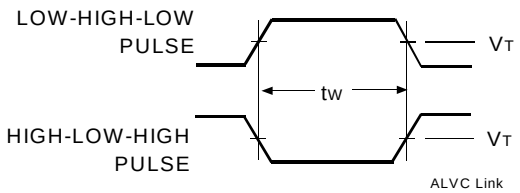
PULSE WIDTH



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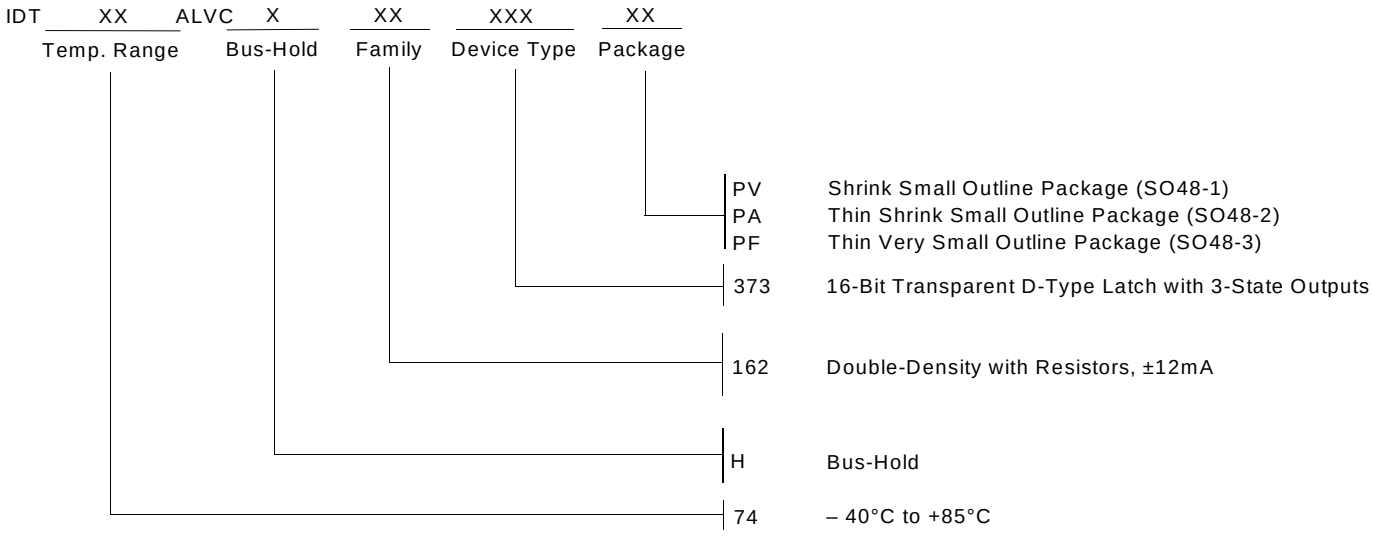
ORDERING INFORMATION



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