



3.3V CMOS SINGLE BUS BUFFER GATE WITH 3-STATE OUTPUTS

IDT74ALVC1G126

FEATURES:

- 0.5 MICRON CMOS Technology
- ESD > 2000V per MIL-STD-883, Method 3015;
> 200V using machine model (C = 200pF, R = 0)
- 0.65mm pitch PSOP package
- Extended commercial range of – 40°C to + 85°C
- $V_{CC} = 3.3V \pm 0.3V$, Normal Range
- $V_{CC} = 1.65V$ to 3.6V, Extended Range
- $V_{CC} = 2.5V \pm 0.2V$
- CMOS power levels (0.4μW typ. static)
- Rail-to-Rail output swing for increased noise margin

Drive Features for ALVC1G126:

- High Output Drivers: $\pm 24mA$
- Suitable for heavy loads

APPLICATIONS:

- 3.3V High Speed Systems
- 3.3V and lower voltage computing systems

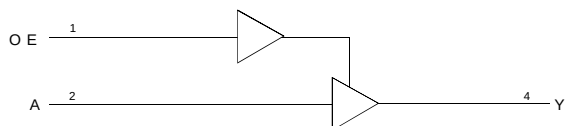
DESCRIPTION:

This single bus buffer gate is built using advanced dual metal CMOS technology. The ALVC1G126 is designed for 1.65V to 3.6V V_{CC} operation and features a single bus driver/line driver with a 3-state output. The output is disabled when output-enable (OE) input is low.

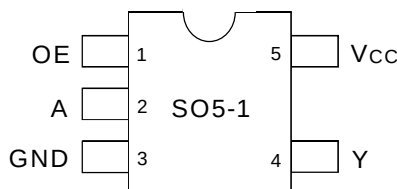
To ensure the high-impedance state during power up or power down, OE should be tied to GND through a pulldown resistor; the minimum value of the resistor is determined by the current-sourcing capability of the driver.

The ALVC1G126 has been designed with a $\pm 24mA$ output driver. This driver is capable of driving a moderate to heavy load while maintaining speed performance.

FUNCTIONAL BLOCK DIAGRAM



PIN CONFIGURATION



PSOP
TOP VIEW

PIN DESCRIPTION

Pin Names	Description
OE	Output-enable Input
A	Data Input
Y	3-State Output

FUNCTION TABLE (1)

Inputs		Output
OE	A	Y
H	H	H
H	L	L
L	X	Z

NOTE:

1. H = HIGH Voltage Level
L = LOW Voltage Level
X = Don't Care
Z = High-Impedance

ABSOLUTE MAXIMUM RATING (1)

Symbol	Description	Max.	Unit
V _{TERM} (2)	Terminal Voltage with Respect to GND	– 0.5 to + 4.6	V
V _{TERM} (3)	Terminal Voltage with Respect to GND	–0.5 to V _{CC} + 0.5	V
T _{STG}	Storage Temperature	– 65 to + 150	°C
I _{OUT}	DC Output Current	– 50 to + 50	mA
I _{IK}	Continuous Clamp Current, V _I < 0 or V _I > V _{CC}	± 50	mA
I _{OK}	Continuous Clamp Current, V _O < 0	– 50	mA
I _{CC}	Continuous Current through each V _{CC} or GND	±100	mA

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NOTES:

- Stresses greater than those listed under ABSOLUTE MAXIMUM RATINGS may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect reliability.
- V_{CC} terminals.
- All terminals except V_{CC}.

CAPACITANCE (T_A = +25°C, f = 1.0MHz)

Symbol	Parameter(1)	Conditions	Typ.	Max.	Unit
C _{IN}	Input Capacitance	V _{IN} = 0V	5	7	pF
C _{OUT}	Output Capacitance	V _{OUT} = 0V	7	9	pF
C _{I/O}	I/O Port Capacitance	V _{IN} = 0V	7	9	pF

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NOTE:

- As applicable to the device type.

DC ELECTRICAL CHARACTERISTICS OVER OPERATING RANGE

Following Conditions Apply Unless Otherwise Specified:

Operating Condition: T_A = – 40°C to +85°C, V_{CC} = 2.3V to 3.6V

Symbol	Parameter	Test Conditions		Min.	Typ.(1)	Max.	Unit
V _{IH}	Input HIGH Voltage Level	V _{CC} = 1.65V to 1.95V		0.65 x V _{CC}	—	—	V
		V _{CC} = 2.3V to 2.7V		1.7	—	—	
		V _{CC} = 2.7V to 3.6V		2	—	—	
V _{IL}	Input LOW Voltage Level	V _{CC} = 1.65V to 1.95V		—	—	0.35 x V _{CC}	V
		V _{CC} = 2.3V to 2.7V		—	—	0.7	
		V _{CC} = 2.7V to 3.6V		—	—	0.8	
I _{IH}	Input HIGH Current	V _{CC} = 3.6V	V _I = V _{CC}	—	—	± 5	μA
I _{IL}	Input LOW Current	V _{CC} = 3.6V	V _I = GND	—	—	± 5	
I _{OZH}	High Impedance Output Current (3-State Output pins)	V _{CC} = 3.6V	V _O = V _{CC}	—	—	± 10	μA
I _{OZL}			V _O = GND	—	—	± 10	μA
V _{IK}	Clamp Diode Voltage	V _{CC} = 2.3V, I _{IN} = – 18mA		—	– 0.7	– 1.2	V
V _H	Input Hysteresis	V _{CC} = 3.3V		—	100	—	mV
I _{CC1} I _{CC2} I _{CC3}	Quiescent Power Supply Current	V _{CC} = 3.6V V _{IN} = GND or V _{CC}		—	0.1	10	μA
ΔI _{CC}	Quiescent Power Supply Current Variation	One input at V _{CC} – 0.6V, other inputs at V _{CC} or GND		—	—	750	μA

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NOTE:

- Typical values are at V_{CC} = 3.3V, +25°C ambient.

OUTPUT DRIVE CHARACTERISTICS

Symbol	Parameter	Test Conditions ⁽¹⁾		Min.	Max.	Unit
VOH	Output HIGH Voltage	VCC = 1.65V to 3.6V	IOH = – 0.1mA	VCC – 0.2	—	V
		VCC = 1.65V	IOH = – 4mA	1.2		
		VCC = 2.3V	IOH = – 6mA	2	—	
		VCC = 2.3V	IOH = – 12mA	1.7	—	
		VCC = 2.7V		2.2	—	
		VCC = 3.0V		2.4	—	
		VCC = 3.0V	IOH = – 24mA	2	—	
VOL	Output LOW Voltage	VCC = 1.65V to 3.6V	IOL = 0.1mA	—	0.2	V
		VCC = 1.65V	IOL = 4mA		0.45	
		VCC = 2.3V	IOL = 6mA	—	0.4	
			IOL = 12mA	—	0.7	
		VCC = 2.7V	IOL = 12mA	—	0.4	
		VCC = 3.0V	IOL = 24mA	—	0.55	

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NOTE:

1. VIH and VIL must be within the min. or max. range shown in the DC ELECTRICAL CHARACTERISTICS OVER OPERATING RANGE table for the appropriate VCC range. TA = – 40°C to + 85°C.

OPERATING CHARACTERISTICS, TA = 25°C

Symbol	Parameter	Test Conditions	VCC = 1.8V ± 0.15V	VCC = 2.5V ± 0.2V	VCC = 3.3V ± 0.3V	Unit
			Typical	Typical	Typical	
CPD	Power Dissipation Capacitance Outputs enabled	CL = 0pF, f = 10Mhz	—	2.5	3	pF
CPD	Power Dissipation Capacitance Outputs disabled		—	0.5	0.5	pF

SWITCHING CHARACTERISTICS⁽¹⁾

Symbol	Parameter	VCC = 1.8V ± 0.15V		VCC = 2.5V ± 0.2V		VCC = 2.7V		VCC = 3.3V ± 0.3V		Unit
		Min.	Max.	Min.	Max.	Min.	Max.	Min.	Max.	
tPLH tPHL	Propagation Delay A to Y	—	7	1	3.1	—	3.1	1.1	2.8	ns
tPZH tPZL	Output Enable Time OE to Y	—	10	1.5	5.4	—	5.3	1.5	4.5	ns
tPHZ tPLZ	Output Disable Time OE to Y	—	9	1	4.1	—	4.4	1.7	4.2	ns

NOTE:

1. See test circuits and waveforms. TA = – 40°C to + 85°C.

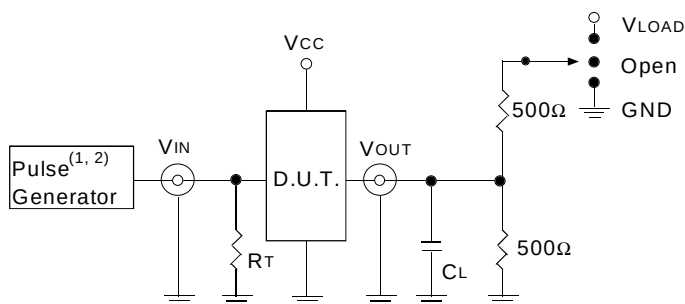
TEST CIRCUITS AND WAVEFORMS:

TEST CONDITIONS

Symbol	$V_{CC}^{(1)} = 3.3V \pm 0.3V$	$V_{CC}^{(1)} = 2.7V$	$V_{CC}^{(2)} = 2.5V \pm 0.2V$	Unit
V_{LOAD}	6	6	$2 \times V_{CC}$	V
V_{IH}	2.7	2.7	V_{CC}	V
V_T	1.5	1.5	$V_{CC} / 2$	V
V_{LZ}	300	300	150	mV
V_{HZ}	300	300	150	mV
C_L	50	50	30	pF

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TEST CIRCUITS FOR ALL OUTPUTS



DEFINITIONS:

C_L = Load capacitance: includes jig and probe capacitance.

R_T = Termination resistance: should be equal to Z_{OUT} of the Pulse Generator.

NOTES:

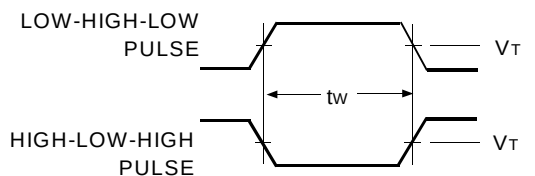
1. Pulse Generator for All Pulses: Rate $\leq 10\text{MHz}$; $t_F \leq 2.5\text{ns}$; $t_R \leq 2.5\text{ns}$.
2. Pulse Generator for All Pulses: Rate $\leq 10\text{MHz}$; $t_F \leq 2\text{ns}$; $t_R \leq 2\text{ns}$.

SWITCH POSITION

Test	Switch
Open Drain Disable Low Enable Low	V_{LOAD}
Disable High Enable High	GND
All Other tests	Open

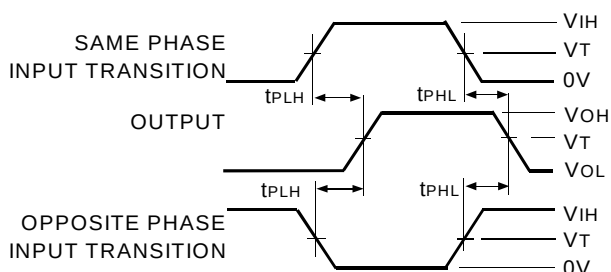
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PULSE WIDTH



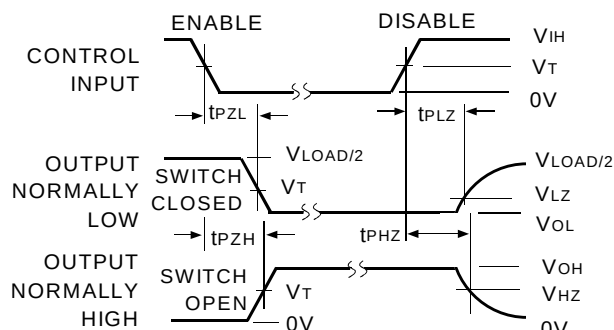
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PROPAGATION DELAY



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ENABLE AND DISABLE TIMES

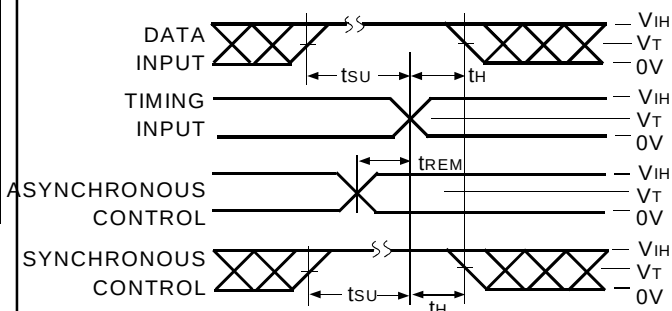


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NOTE:

1. Diagram shown for input Control Enable-LOW and input Control Disable-HIGH.

SET-UP, HOLD, AND RELEASE TIMES



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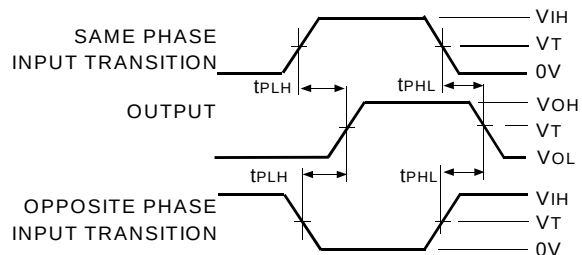
1.8V ± 0.15V TEST CIRCUITS AND WAVEFORMS:

TEST CONDITIONS

Symbol	V _{CC} (1) = 1.8V ± 0.15V	Unit
V _{LOAD}	2 x V _{CC}	V
V _{IH}	V _{CC}	V
V _T	V _{CC} / 2	V
V _{LZ}	150	mV
V _{HZ}	150	mV
C _L	30	pF

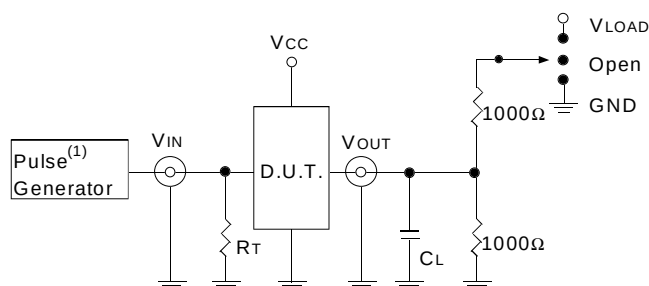
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PROPAGATION DELAY



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TEST CIRCUITS FOR ALL OUTPUTS



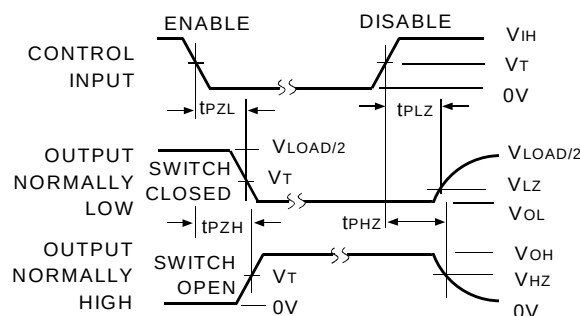
DEFINITIONS:

C_L = Load capacitance: includes jig and probe capacitance.
R_T = Termination resistance: should be equal to Z_{OUT} of the Pulse Generator.

NOTE:

1. Pulse Generator for All Pulses: Rate ≤ 10MHz; t_r ≤ 2ns; t_r ≤ 2ns.

ENABLE AND DISABLE TIMES



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NOTE:

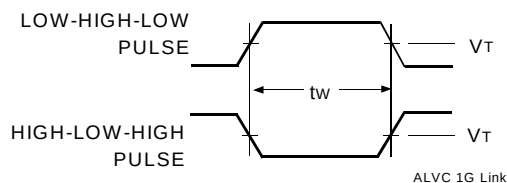
1. Diagram shown for input Control Enable-LOW and input Control Disable-HIGH.

SWITCH POSITION

Test	Switch
Open Drain Disable Low Enable Low	V _{LOAD}
Disable High Enable High	GND
All Other tests	Open

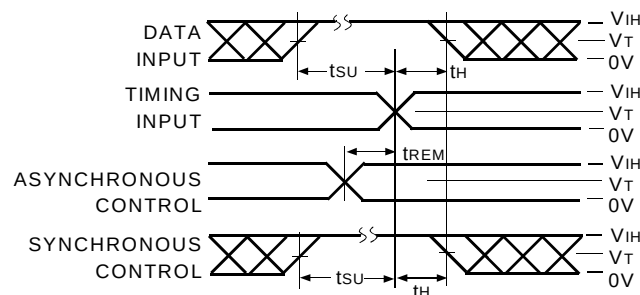
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PULSE WIDTH



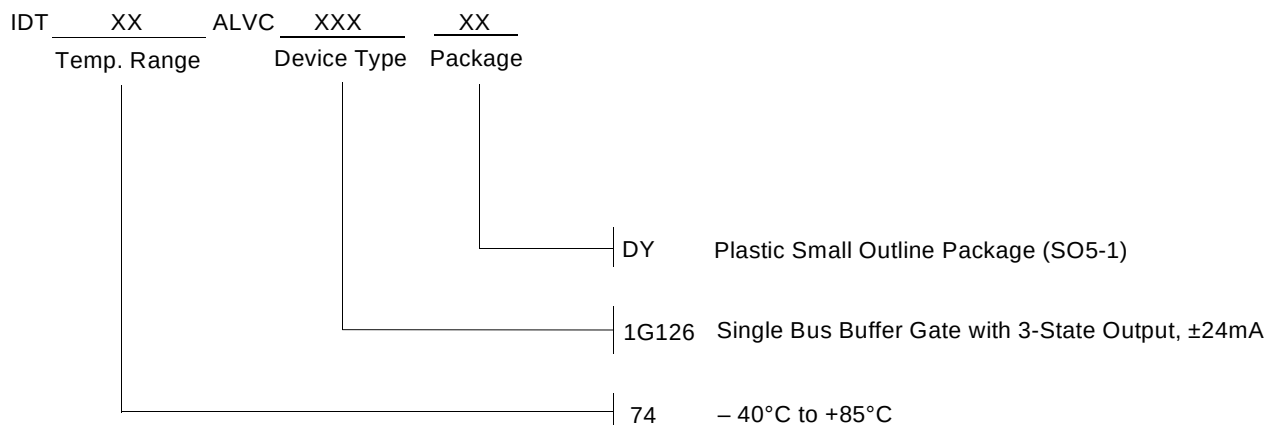
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SET-UP, HOLD, AND RELEASE TIMES



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ORDERING INFORMATION



PICOGATE-LOGIC (DY) PACKAGES

Due to their small size, PicoGate-Logic packages require more complex symbolization guidelines. IDT's 5-pin PSOP (DY) packaged devices utilize a three-symbol name rule. The first symbol denotes device technology, the second symbol denotes device function, and the third symbol denotes a wafer fab/assembly site code for internal tracking.

EXAMPLES:

1. A PicoGate-Logic device with package code LR* is an IDT74LVC1G79A.
2. A PicoGate-Logic device with package code GC* is an IDT74ALVC1G04.

PICOGATE-LOGIC (DY) PACKAGE SYMBOLIZATION GUIDELINES

TECHNOLOGY	CODE	FUNCTION	CODE
ALVC	G	00	A
ALVCH	J	02	B
LVC	L	04	C
LVCH ⁽¹⁾		U04	D
		06	T
		07	V
		08	E
		14	F
		32	G
		79	R
		86	H
		125	M
		126	N
		132	Y

NOTE:

1. Code to be determined.



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