3.3V CMOS 12-BIT TO 24-BIT MULTIPLEXED D-TYPE LATCH WITH 3-STATE OUTPUTS

IDT74ALVC16260

FEATURES:

- 0.5 MICRON CMOS Technology
- Typical $t_{SK(0)}$ (Output Skew) < 250ps
- ESD > 2000V per MIL-STD-883, Method 3015; > 200V using machine model (C = 200pF, R = 0)
- 0.635mm pitch SSOP, 0.50mm pitch TSSOP, and 0.40mm pitch TVSOP packages
- Extended commercial range of – 40°C to + 85°C
- V_{CC} = 3.3V ± 0.3V, Normal Range
- V_{CC} = 2.7V to 3.6V, Extended Range
- V_{CC} = 2.5V ± 0.2V
- CMOS power levels (0.4µW typ. static)
- Rail-to-Rail output swing for increased noise margin

Drive Features for ALVC16260:

- High Output Drivers: ±24mA
- Suitable for heavy loads

APPLICATIONS:

- 3.3V High Speed Systems
- 3.3V and lower voltage computing systems

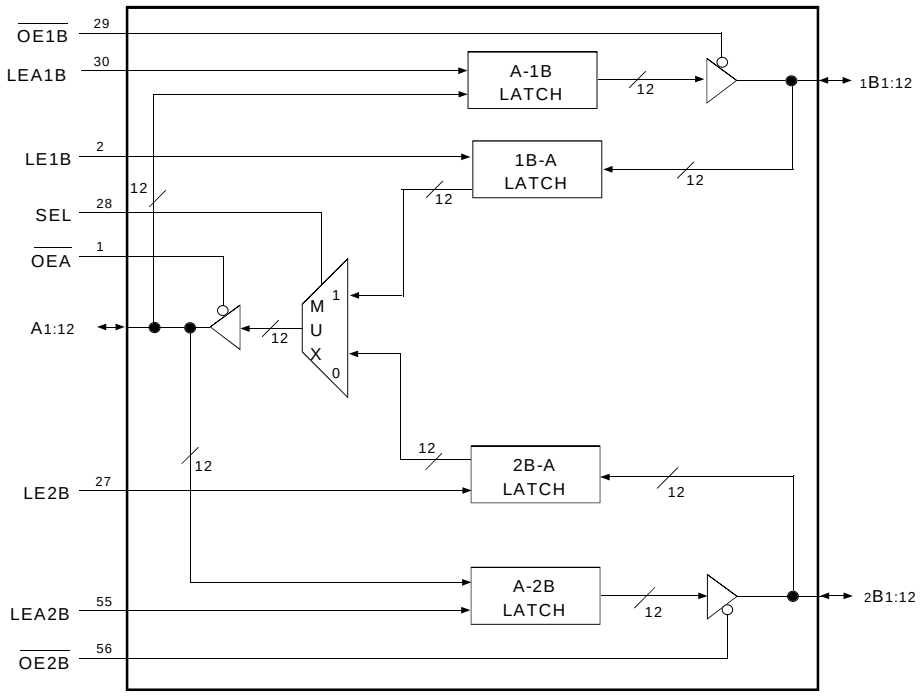
DESCRIPTION:

This 12-bit to 24-bit multiplexed D-type latch is built using advanced dual metal CMOS technology. The ALVC16260 is used in applications in which two separate data paths must be multiplexed onto, or demultiplexed from, a single data path. Typical applications include multiplexing and/or demultiplexing address and data information in microprocessor or bus-interface applications. This device also is useful in memory interleaving applications.

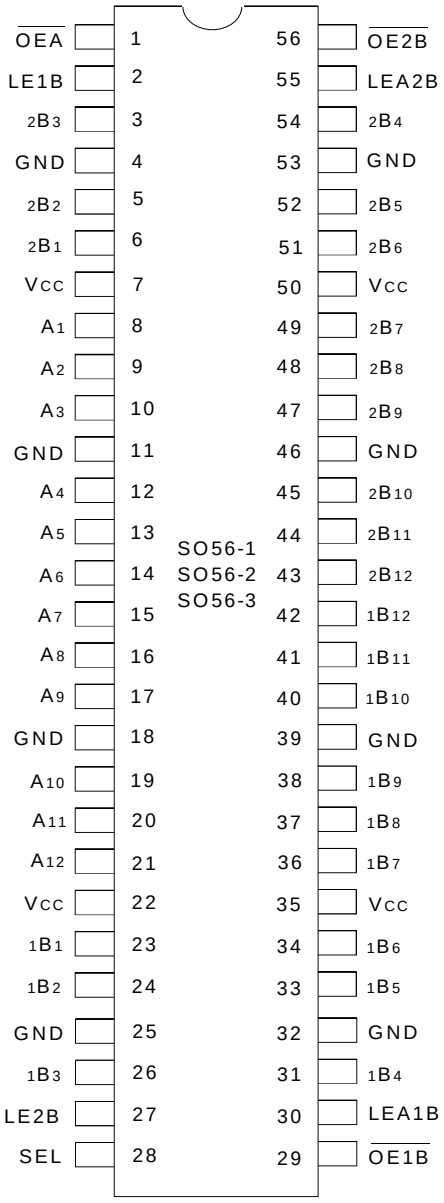
Three 12-bit I/O ports (A1-A12, 1B1-1B12, and 2B1-2B12) are available for address and/or data transfer. The output-enable ($\overline{OE1B}$, $\overline{OE2B}$, and $\overline{OEA}$) inputs control the bus transceiver functions. The $\overline{OE1B}$ and $\overline{OE2B}$ control signals also allow bank control in the A-to-B direction. Address and/or data information can be stored using the internal storage latches. The latch-enable (LE1B, LE2B, LEA1B, and LEA2B) inputs are used to control data storage. When the latch-enable input is high, the latch is transparent. When the latch-enable input goes low, the data present at the inputs is latched and remains latched until the latch-enable input is returned high.

The ALVC16260 has been designed with a ±24mA output driver. This driver is capable of driving a moderate to heavy load while maintaining speed performance.

Functional Block Diagram



PIN CONFIGURATION



SSOP/
TSSOP/ TVSOP
TOP VIEW

ABSOLUTE MAXIMUM RATING (1)

Symbol	Description	Max.	Unit
V_{TERM}(2)	Terminal Voltage with Respect to GND	– 0.5 to + 4.6	V
V_{TERM}(3)	Terminal Voltage with Respect to GND	– 0.5 to V_{CC} + 0.5	V
T_{STG}	Storage Temperature	– 65 to + 150	°C
I_{OUT}	DC Output Current	– 50 to + 50	mA
I_{IK}	Continuous Clamp Current, $V_I < 0$ or $V_I > V_{CC}$	± 50	mA
I_{OK}	Continuous Clamp Current, $V_O < 0$	– 50	mA
I_{CC} I_{SS}	Continuous Current through each V_{CC} or GND	±100	mA

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NOTES:
1. Stresses greater than those listed under ABSOLUTE MAXIMUM RATINGS may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect reliability.
2. V_{CC} terminals.
3. All terminals except V_{CC}.

CAPACITANCE (T_A = +25°C, f = 1.0MHz)

Symbol	Parameter(1)	Conditions	Typ.	Max.	Unit
C_{IN}	Input Capacitance	V_{IN} = 0V	5	7	pF
C_{OUT}	Output Capacitance	V_{OUT} = 0V	7	9	pF
$C_{I/O}$	I/O Port Capacitance	V_{IN} = 0V	7	9	pF

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NOTE:
1. As applicable to the device type.

FUNCTION TABLES (1)

B TO A ($\overline{OEB}$ = H)

Inputs						Output
1Bx	2Bx	SEL	LE1B	LE2B	$\overline{OEA}$	Ax
H	X	H	H	X	L	H
L	X	H	H	X	L	L
X	X	H	L	X	L	A_0(2)
X	H	L	X	H	L	H
X	L	L	X	H	L	L
X	X	L	X	L	L	A_0(2)
X	X	X	X	X	H	Z

FUNCTION TABLES (1) - Cont'd

A TO B ($\overline{OEA}$ = H)

Inputs					Outputs	
Ax	LEA1B	LEA2B	$\overline{OE1B}$	$\overline{OE2B}$	1Bx	2Bx
H	H	H	L	L	H	H
L	H	H	L	L	L	L
H	H	L	L	L	H	$2B_0$ (2)
L	H	L	L	L	L	$2B_0$ (2)
H	L	H	L	L	$1B_0$ (2)	H
L	L	H	L	L	$1B_0$ (2)	L
X	L	L	L	L	$1B_0$ (2)	$2B_0$ (2)
X	X	X	H	H	Z	Z
X	X	X	L	H	Active	Z
X	X	X	H	L	Z	Active
X	X	X	L	L	Active	Active

NOTES:
1. H = HIGH Voltage Level
   L = LOW Voltage Level
   X = Don't Care
   Z = High-Impedance
2. Output level before the indicated steady-state input conditions were established.

PIN DESCRIPTION

Signal	I/O	Description
Ax(1:12)	I/O	Bidirectional Data Port A. Usually connected to the CPU's Address/Data bus.
1Bx(1:12)	I/O	Bidirectional Data Port 1B. Connected to the even path or even bank of memory
2Bx(1:12)	I/O	Bidirectional Data Port 2B. Connected to the odd path or odd bank of memory.
LEA1B	I	Latch Enable Input for A-1B Latch. The Latch is open when LEA1B is HIGH. Data from the A-port is latched on the HIGH to LOW transition of LEA1B.
LEA2B	I	Latch Enable Input for A-2B Latch. The Latch is open when LEA2B is HIGH. Data from the A-port is latched on the HIGH to LOW transition of LEA2B.
LE1B	I	Latch Enable Input for 1B-A Latch. The Latch is open when LE1B is HIGH. Data from the 1B port is latched on the HIGH to LOW transition of LE1B.
LE2B	I	Latch Enable Input for 2B-A Latch. The Latch is open when LE2B is HIGH. Data from the 2B port is latched on the HIGH to LOW transition of LE2B.
SEL	I	1B or 2B Path Selection. When HIGH, SEL enables data transfer from 1B Port to A Port. When LOW, SEL enables data transfer from 2B Port to A Port.
$\overline{OEA}$	I	Output Enable for A Port (Active LOW).
$\overline{OE1B}$	I	Output Enable for 1B Port (Active LOW).
$\overline{OE2B}$	I	Output Enable for 2B Port (Active LOW).

DC ELECTRICAL CHARACTERISTICS OVER OPERATING RANGE

Following Conditions Apply Unless Otherwise Specified:

Operating Condition: TA = – 40° C to +85° C

Symbol	Parameter	Test Conditions		Min.	Typ.(1)	Max.	Unit
V_{IH}	Input HIGH Voltage Level	V_{CC} = 2.3V to 2.7V		1.7	—	—	V
		V_{CC} = 2.7V to 3.6V		2	—	—	
V_{IL}	Input LOW Voltage Level	V_{CC} = 2.3V to 2.7V		—	—	0.7	V
		V_{CC} = 2.7V to 3.6V		—	—	0.8	
I_{IH}	Input HIGH Current	V_{CC} = 3.6V	V_I = V_{CC}	—	—	± 5	µA
I_{IL}	Input LOW Current	V_{CC} = 3.6V	V_I = GND	—	—	± 5	
I_{OZH}	High Impedance Output Current	V_{CC} = 3.6V	V_O = V_{CC}	—	—	± 10	µA
I_{OZL}	(3-State Output pins)		V_O = GND	—	—	± 10	µA
V_{IK}	Clamp Diode Voltage	V_{CC} = 2.3V, I_{IN} = – 18mA		—	– 0.7	– 1.2	V
V_H	Input Hysteresis	V_{CC} = 3.3V		—	100	—	mV
I_{CCL} I_{CCH} I_{CCZ}	Quiescent Power Supply Current	V_{CC} = 3.6V V_{IN} = GND or V_{CC}		—	0.1	40	µA
ΔI_{CC}	Quiescent Power Supply Current Variation	One input at V_{CC} – 0.6V, other inputs at V_{CC} or GND		—	—	750	µA

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NOTE:

1. Typical values are at V_{CC} = 3.3V, +25°C ambient.

OUTPUT DRIVE CHARACTERISTICS

Symbol	Parameter	Test Conditions(1)		Min.	Max.	Unit
V_{OH}	Output HIGH Voltage	V_{CC} = 2.3V to 3.6V	I_{OH} = – 0.1mA	V_{CC} – 0.2	—	V
		V_{CC} = 2.3V	I_{OH} = – 6mA	2	—	
		V_{CC} = 2.3V	I_{OH} = – 12mA	1.7	—	
		V_{CC} = 2.7V		2.2	—	
		V_{CC} = 3.0V		2.4	—	
		V_{CC} = 3.0V	I_{OH} = – 24mA	2	—	
V_{OL}	Output LOW Voltage	V_{CC} = 2.3V to 3.6V	I_{OL} = 0.1mA	—	0.2	V
		V_{CC} = 2.3V	I_{OL} = 6mA	—	0.4	
			I_{OL} = 12mA	—	0.7	
		V_{CC} = 2.7V	I_{OL} = 12mA	—	0.4	
		V_{CC} = 3.0V	I_{OL} = 24mA	—	0.55	

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NOTE:

1. V_{IH} and V_{IL} must be within the min. or max. range shown in the DC ELECTRICAL CHARACTERISTICS OVER OPERATING RANGE table for the appropriate V_{CC} range. T_A = – 40°C to + 85°C.

OPERATING CHARACTERISTICS, T_A = 25°C

Symbol	Parameter	Test Conditions	VCC = 2.5V ± 0.2V Typical	VCC = 3.3V ± 0.3V Typical	Unit
C_{PD}	Power Dissipation Capacitance per latch Outputs enabled	CL = 0pF, f = 10Mhz	37	41	pF
C_{PD}	Power Dissipation Capacitance per latch Outputs disabled		4	7	pF

SWITCHING CHARACTERISTICS(1)

Symbol	Parameter	VCC = 2.5V ± 0.2V		VCC = 2.7V		VCC = 3.3V ± 0.3V		Unit
		Min.	Max.	Min.	Max.	Min.	Max.	
t_{PLH} t_{PHL}	Propagation Delay AX to 1BX or Ax to 2BX	1	5.4	—	5.1	1.2	4.3	ns
t_{PLH} t_{PHL}	Propagation Delay 1BX to AX or 2BX to AX	1	5.4	—	5.1	1.2	4.3	ns
t_{PLH} t_{PHL}	Propagation Delay LEXB to AX	1	5.6	—	5.2	1	4.4	ns
t_{PLH} t_{PHL}	Propagation Delay LEA1B to 1BX or LEA2B to 2BX	1	5.6	—	5.2	1	4.4	ns
t_{PLH} t_{PHL}	Propagation Delay SEL to AX	1	6.9	—	6.6	1.1	5.6	ns
t_{PZH} t_{PZL}	Output Enable Time $\overline{OEA}$ to AX, $\overline{OE1B}$ to 1BX, or $\overline{OE2B}$ to 2BX	1	6.7	—	6.4	1	5.4	ns
t_{PHZ} t_{PLZ}	Output Disable Time $\overline{OEA}$ to AX, $\overline{OE1B}$ to 1BX, or $\overline{OE2B}$ to 2BX	1	5.7	—	5	1.3	4.6	ns
t_{SU}	Setup Time, data before LE1B, LE2B, LEA1B, LEA2B	1.4	—	1.1	—	1.1	—	ns
t_H	Hold Time, data after LE1B, LE2B, LEA1B, LEA2B	1.6	—	1.9	—	1.5	—	ns
t_W	Pulse Duration, LE1B, LE2B, LEA1B, or LEA2B HIGH	3.3	—	3.3	—	3.3	—	ns
$t_{SK(o)}$	Output Skew(2)	—	—	—	—	—	500	ps

NOTES:
1. See test circuits and waveforms. T_A = – 40°C to + 85°C.
2. Skew between any two outputs of the same package and switching in the same direction.

TEST CIRCUITS AND WAVEFORMS

TEST CONDITIONS

Symbol	$V_{CC}^{(1)}$= 3.3V±0.3V	$V_{CC}^{(1)}$= 2.7V	$V_{CC}^{(2)}$= 2.5V±0.2V	Unit
V_{LOAD}	6	6	2 x Vcc	V
V_{IH}	2.7	2.7	Vcc	V
V_T	1.5	1.5	Vcc / 2	V
V_{LZ}	300	300	150	mV
V_{HZ}	300	300	150	mV
C_L	50	50	30	pF

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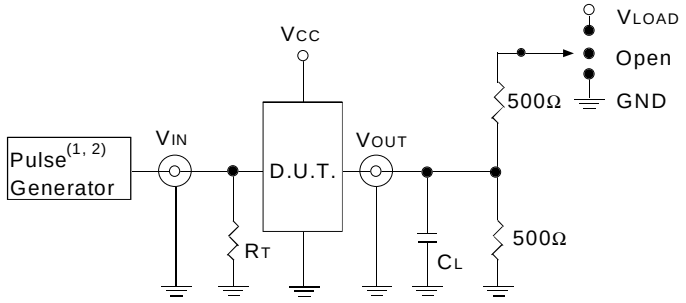
TEST CIRCUITS FOR ALL OUTPUTS



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DEFINITIONS:

C_L= Load capacitance: includes jig and probe capacitance.
R_T = Termination resistance: should be equal to Z_{OUT} of the Pulse Generator.

NOTES:

1. Pulse Generator for All Pulses: Rate ≤ 10MHz; t_F ≤ 2.5ns; t_R ≤ 2.5ns.
2. Pulse Generator for All Pulses: Rate ≤ 10MHz; t_F ≤ 2ns; t_R ≤ 2ns.

SWITCH POSITION

Test	Switch
Open Drain Disable Low Enable Low	V_{LOAD}
Disable High Enable High	GND
All Other tests	Open

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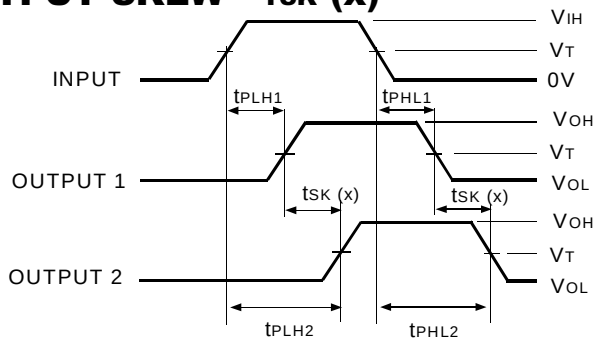
OUTPUT SKEW - t_{SK} (x)



$t_{SK(x)} = |t_{PLH2} - t_{PLH1}|$ or $|t_{PHL2} - t_{PHL1}|$

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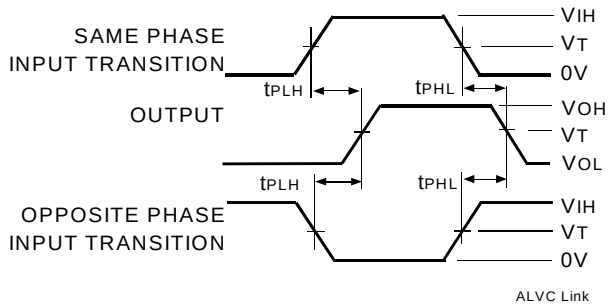
NOTES:

1. For t_{SK}(o) OUTPUT1 and OUTPUT2 are any two outputs.
2. For t_{SK}(b) OUTPUT1 and OUTPUT2 are in the same bank.

PROPAGATION DELAY



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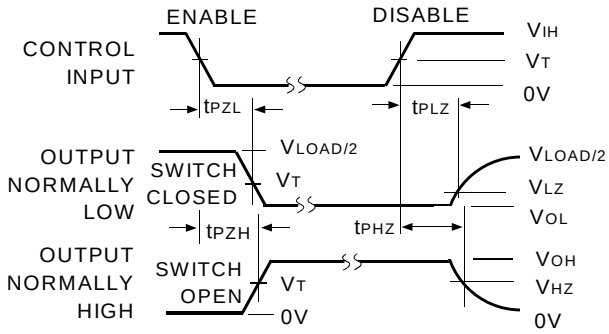
ENABLE AND DISABLE TIMES



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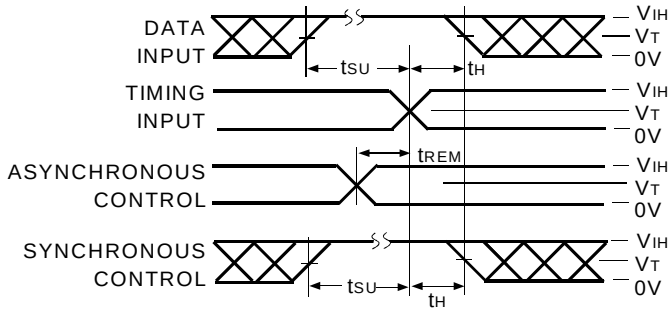
NOTE:

1. Diagram shown for input Control Enable-LOW and input Control Disable-HIGH.

SET-UP, HOLD, AND RELEASE TIMES



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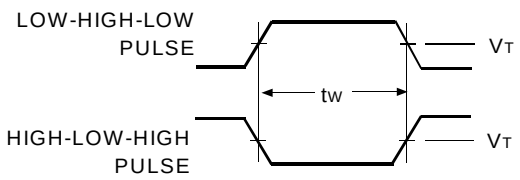
PULSE WIDTH



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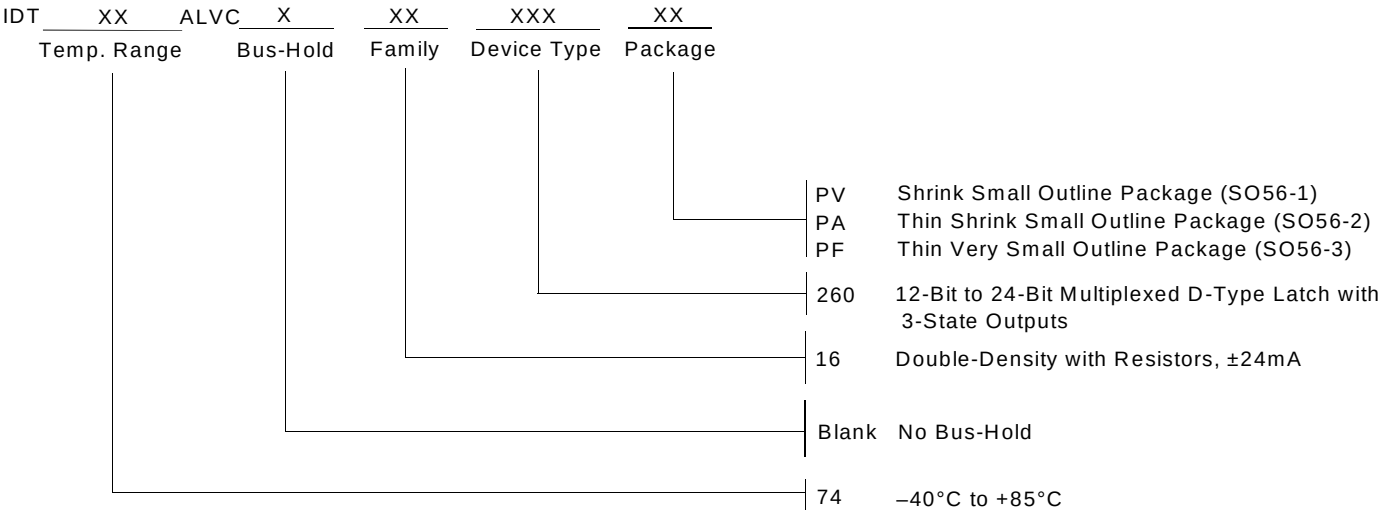
ORDERING INFORMATION



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