



16-BIT PARALLEL CMOS MULTIPLIERS

IDT7217L

FEATURES:

- 16 x 16 parallel multiplier with double precision product
- 16ns clocked multiply time
- Low power consumption: 120mA
- Produced with advanced submicron CMOS high performance technology
- IDT7217L requires a single clock with register enables, making it pin- and function compatible with AMD Am29517
- Configured for easy array expansion
- User-controlled option for transparent output register mode
- Round control for rounding the MSP
- Input and output directly TTL-compatible
- Three-state output
- Available in PLCC
- Speeds available: L16/20/25/35/45/55/65

DESCRIPTION:

The IDT7217 is a high-speed, low-power 16 x 16-bit multiplier, ideal for fast, real time digital signal processing applications. Utilization of a

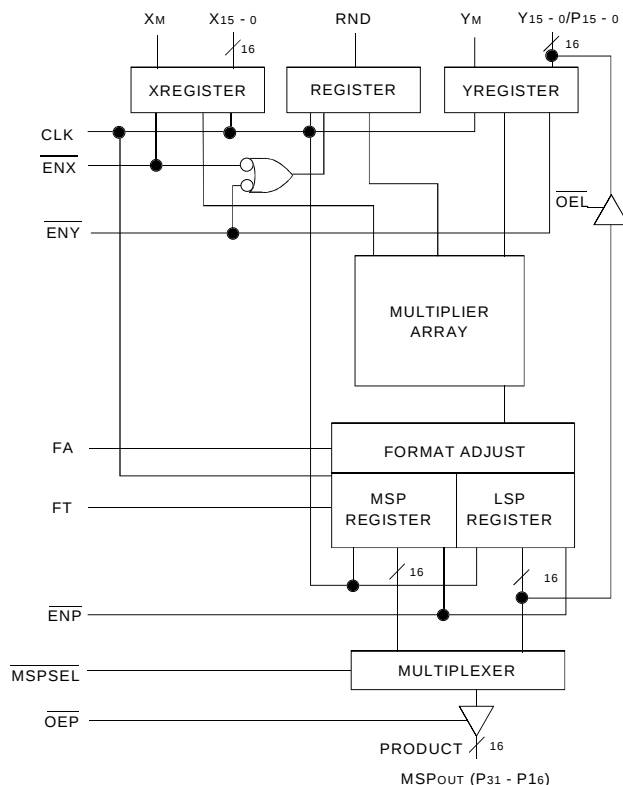
modified Booths algorithm and IDT's high-performance, submicron CMOS technology, has achieved speeds comparable to bipolar (20ns max.), at 1/10 the power consumption.

The IDT7217 is ideal for applications requiring high-speed multiplication such as fast Fourier transform analysis, digital filtering, graphic display systems, speech synthesis and recognition and in any system requirement where multiplication speeds of a mini/microcomputer are inadequate.

All input registers, as well as LSP and MSP output registers, use the same positive edge-triggered D-type flip-flop. The IDT7217 has only a single clock input (CLK) and three register enables. $\overline{\text{ENX}}$ and $\overline{\text{ENY}}$ control the two input registers, while $\overline{\text{ENP}}$ controls the entire product.

The IDT7217 offers additional flexibility with the FA control and $\overline{\text{MSPSEL}}$ functions. The FA control formats the output for two's complement by shifting the MSP up one bit and then repeating the sign bit in the MSB of the LSP. The $\overline{\text{MSPSEL}}$ low selects the MSP to be available at the product output port, while a high selects the LSP to be available. Keeping this pin low will ensure compatibility with the TRW MPY016H.

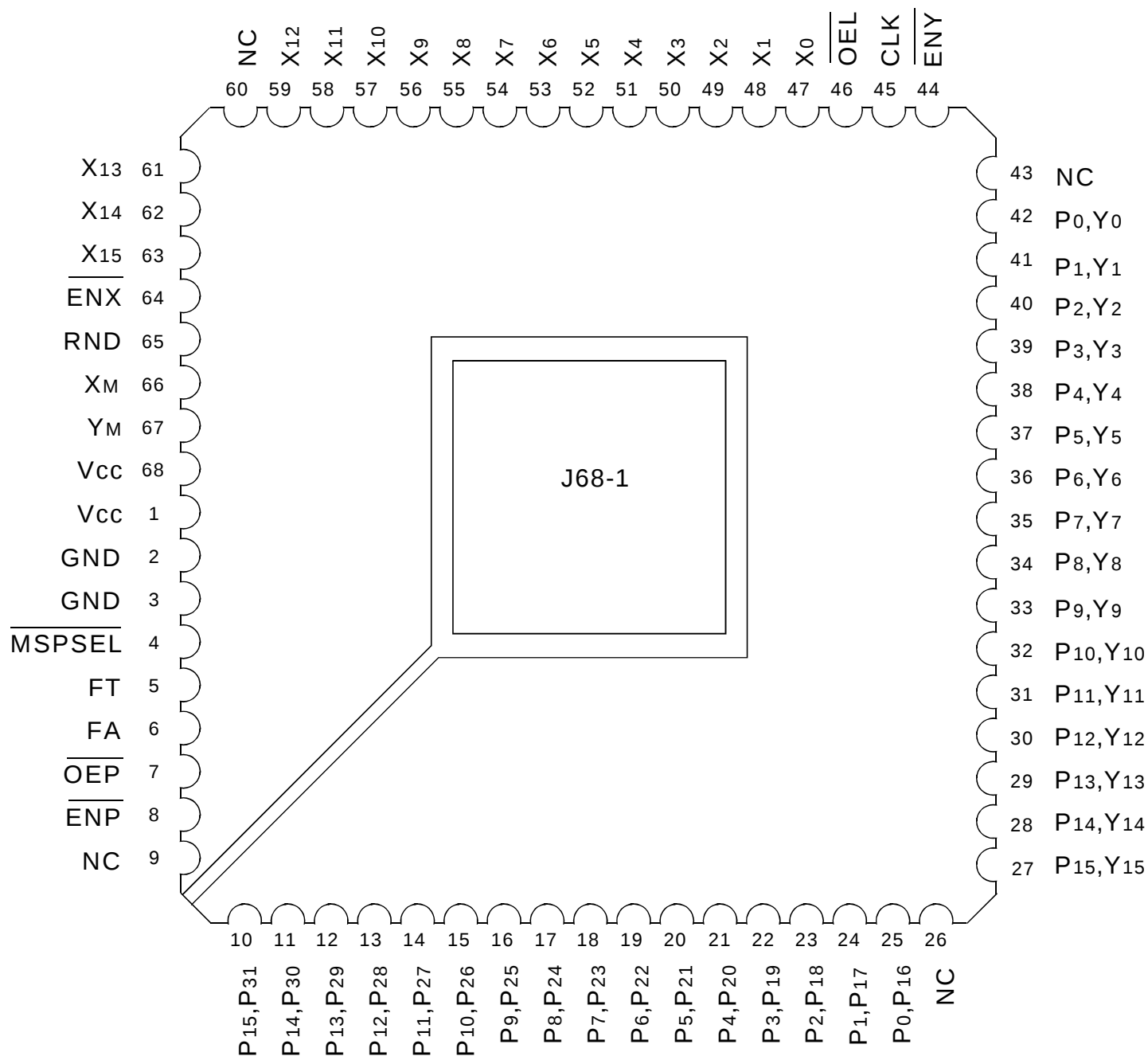
FUNCTIONAL BLOCK DIAGRAM



COMMERCIAL TEMPERATURE RANGE

APRIL 2001

PIN CONFIGURATION



PLCC
TOP VIEW

ABSOLUTE MAXIMUM RATINGS⁽¹⁾

Symbol	Rating	Max.	Unit
V _{CC}	Power Supply Voltage	-0.5 to +7	V
V _{TERM}	Terminal Voltage with Respect to GND	V _{CC} + 0.5	V
T _A	Operating Temperature	0 to +70	°C
T _{BIAS}	Temperature Under Bias	-55 to +125	°C
T _{STG}	Storage Temperature	-55 to +125	°C
I _{OUT}	DC Output Current	50	mA

NOTE:

- Stresses greater than those listed under ABSOLUTE MAXIMUM RATINGS may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect reliability.

CAPACITANCE (T_A = +25°C, f = 1.0MHz)

Symbol	Parameter ⁽¹⁾	Conditions	Max.	Unit
C _{IN}	Input Capacitance	V _{IN} = 0V	10	pF
C _{OUT}	Output Capacitance	V _{OUT} = 0V	12	pF

NOTE:

- This parameter is sampled and not 100% tested.

PIN DESCRIPTION

Pin Name	I/O	Description
X ₀ - X ₁₅	I	Data Inputs
Y ₀ - Y ₁₅ / P ₀ - P ₁₅	I/O	Y ₀ - Y ₁₅ are data inputs P ₀ - P ₁₅ are LSP register output, enabled when $\overline{OEL} = 0$
P ₁₆ - P ₃₁	O	Data Output (LSP or MSP)
$\overline{OEL}$	I	Output enable control for LSP (least significant product). When LOW enables P ₀ - P ₁₅ . When HIGH P ₀ - P ₁₅ tristated.
$\overline{OEP}$	I	Output enable control for MSP (most significant product). When LOW enables P ₁₆ - P ₃₁ . When HIGH P ₁₆ - P ₃₁ tristated.
X _M , Y _M	I	Mode control for each data word. LOW designates unsigned data input and HIGH designates two's complement.
RND	I	"Round" control for rounding of MSP. When HIGH, 1 is added to the most significant bit of LSP. This signal is affected by the state of FA pin. When FA = 1 and RND = 1, 1 is added to the 2 ⁻¹⁵ bit (P ₁₅). When RND = 1 and FA = 0, 1 is added to the 2 ⁻¹⁶ bit (P ₁₄). The RND input is registered. It is clocked on the rising edge of CLK. Rounding always occurs in the positive direction which may introduce a systematic bias.
$\overline{MSPSEL}$	I	When LOW, MSP is output on P ₁₆ - P ₃₁ lines. When HIGH, LSP is output on P ₁₆ - P ₃₁ .
FA	I	Format adjust control. When HIGH, a full 32 bit product is selected. When LOW, a left shifted 31 bit product is selected with the sign bit replicated in the LSP. FA is normally HIGH, except for certain fractional two's complement applications (see multiplier input / output formats).
FT	I	Flow through control. When HIGH, both MSP and LSP registers are by-passed.
CLK	I	X, Y, RND, LSP and MSP register clock input.
$\overline{ENX}$	I	X register clock enable. Also enables RND register clock.
$\overline{ENY}$	I	Y register clock enable. Also enables RND register clock.

DC ELECTRICAL CHARACTERISTICS OVER OPERATING RANGE

Following Conditions Apply Unless Otherwise Specified:

Commercial: $T_A = 0^\circ\text{C}$ to $+70^\circ\text{C}$, $V_{CC} = 5\text{V} \pm 10\%$

Symbol	Parameter	Test Conditions ⁽¹⁾	Min.	Typ. ⁽¹⁾	Max.	Unit
V_{IH}	Input High Voltage	Guaranteed Logic High Level	2	—	—	V
V_{IL}	Input Low Voltage	Guaranteed Logic Low Level	—	—	0.8	V
I_{LI}	Input Leakage Current	$V_{CC} = \text{Max.}$, $V_{IN} = 0$ to V_{CC}	—	—	10	μA
I_{LO}	Output Leakage Current	$V_{CC} = \text{Max.}$, $\overline{OE} = 2\text{V}$, $V_{OUT} = 0$ to V_{CC}	—	—	10	μA
I_{CC}	Operating Power Supply Current	$V_{CC} = \text{Max.}$, Outputs Disabled, $f = 10\text{MHz}$ ⁽²⁾	—	40	80	mA
I_{CCQ1}	Quiescent Power Supply Current	$V_{IN} \geq V_{IH}$, $V_{IN} \leq V_{IL}$	—	20	40	mA
I_{CCQ2}	Quiescent Power Supply Current	$V_{IN} \geq V_{CC} - 0.2\text{V}$, $V_{IN} \leq 0.2\text{V}$	—	4	20	mA
$I_{CC}/f^{(2,3)}$	Increase in Power Supply Current	$V_{CC} = \text{Max.}$, Outputs Disabled	—	—	4	mA/MHz
V_{OH}	Output HIGH Voltage	$V_{CC} = \text{Min.}$, $I_{OH} = -2\text{mA}$	2.4	—	—	V
$V_{OL}^{(4)}$	Output LOW Voltage	$V_{CC} = \text{Min.}$, $I_{OL} = 8\text{mA}$	—	—	0.4	V
I_{OS}	Output Short Circuit Current	$V_{CC} = \text{Max.}$, $V_O = \text{GND}$	-20	—	-120	mA

NOTES:

1. Typical implies $V_{CC} = 5\text{V}$ and $T_A = +25^\circ\text{C}$.

2. I_{CC} is measured at 10MHz and $V_{IN} = 0$ to 3V. For frequencies greater than 10MHz, the following equation is used for the commercial range:

$I_{CC} = 80 + 4(f - 10)\text{mA}$; for the military range, $I_{CC} = 100 + 6(f - 10)$. f = operating frequency in MHz and $f = 1/t_{MC}$.

3. For frequencies greater than 10MHz, guaranteed by design, not production tested.

4. $I_{OL} = 4\text{mA}$ for $t_{MC} > 65\text{ns}$.

AC ELECTRICAL CHARACTERISTICS

Following Conditions Apply Unless Otherwise Specified:

Commercial: $T_A = 0^\circ\text{C}$ to $+70^\circ\text{C}$, $V_{CC} = 5\text{V} \pm 10\%$

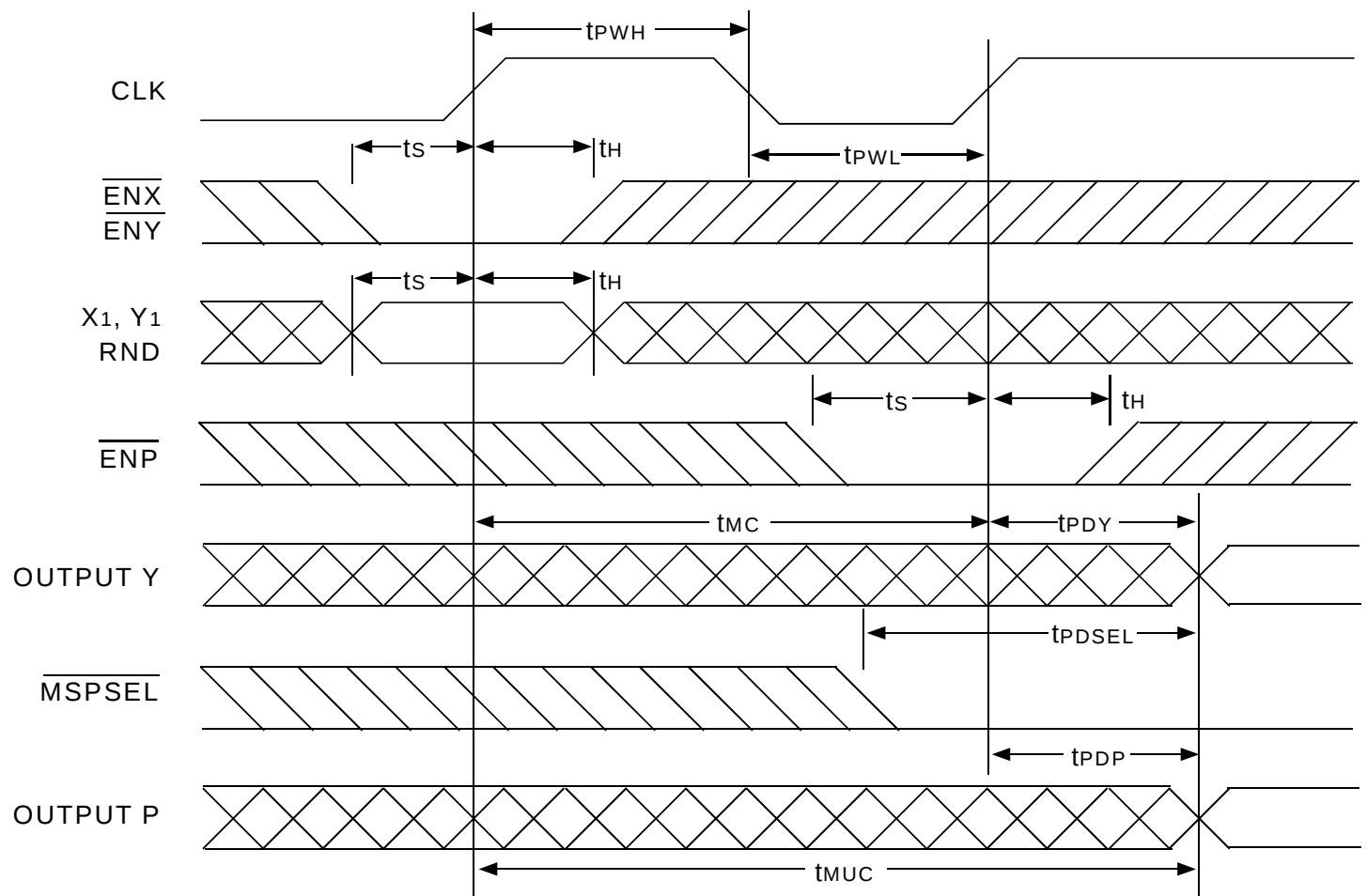
Symbol	Parameter	7217L16		7217L20		7217L25		7217L35		Unit
		Min.	Max.	Min.	Max.	Min.	Max.	Min.	Max.	
t _{MUC}	Unclocked Multiply Time ⁽⁴⁾	2	25	2	30	2	38	2	55	ns
t _{MC}	Clocked Multiply Time ⁽⁴⁾	2	16	2	20	2	25	2	35	ns
t _S	X, Y, RND Set-up Time	10	—	11	—	12	—	12	—	ns
t _H	X, Y, RND Hold Time	1	—	1	—	2	—	3	—	ns
t _{PWH}	Clock Pulse Width HIGH	7	—	9	—	10	—	10	—	ns
t _{PWL}	Clock Pulse Width LOW	7	—	9	—	10	—	10	—	ns
t _{PDSEL}	MSPSEL to Product Out ⁽⁴⁾	2	15	2	18	2	20	2	25	ns
t _{PDP}	Output Clock to P ⁽⁴⁾	2	15	2	18	2	20	2	25	ns
t _{PDY}	Output Clock to Y ⁽⁴⁾	2	15	2	18	2	20	2	25	ns
t _{ENA}	3-State Enable Time	—	15	—	18	—	20	—	25	ns
t _{DIS}	3-State Disable Time ⁽²⁾	—	15	—	18	—	20	—	22	ns
t _S	Clock Enable Set-up Time	9	—	10	—	10	—	10	—	ns
t _H	Clock Enable Hold Time	0	—	0	—	2	—	3	—	ns

Symbol	Parameter	7217L45		7217L55		7217L65		Unit
		Min.	Max.	Min.	Max.	Min.	Max.	
t _{MUC}	Unclocked Multiply Time ⁽⁴⁾	2	65	2	75	2	85	ns
t _{MC}	Clocked Multiply Time ⁽⁴⁾	2	45	2	55	2	65	ns
t _S	X, Y, RND Set-up Time	15	—	20	—	20	—	ns
t _H	X, Y, RND Hold Time	3	—	3	—	3	—	ns
t _{PWH}	Clock Pulse Width HIGH	15	—	15	—	15	—	ns
t _{PWL}	Clock Pulse Width LOW	15	—	20	—	20	—	ns
t _{PDSEL}	MSPSEL to Product Out ⁽⁴⁾	2	25	2	25	2	30	ns
t _{PDP}	Output Clock to P ⁽⁴⁾	2	25	2	30	2	30	ns
t _{PDY}	Output Clock to Y ⁽⁴⁾	2	25	2	30	2	30	ns
t _{ENA}	3-State Enable Time	—	25	—	30	—	35	ns
t _{DIS}	3-State Disable Time ⁽²⁾	—	22	—	25	—	25	ns
t _S	Clock Enable Set-up Time	10	—	10	—	10	—	ns
t _H	Clock Enable Hold Time	3	—	3	—	3	—	ns

NOTES:

1. To ensure that the correct product is entered in the output registers, new data may not be entered into the registers before the output registers have been clocked.
2. Transition is measured $\pm 500\text{mV}$ from steady state voltage.
3. Guaranteed by design, not production tested.
4. Minimum propagation delay times are guaranteed, not production tested.

TIMING DIAGRAM



BINARY POINT

X15	X14	X13	X12	X11	X10	X9	X8	X7	X6	X5	X4	X3	X2	X1	X0	SIGNAL
-2^0	2^{-1}	2^{-2}	2^{-3}	2^{-4}	2^{-5}	2^{-6}	2^{-7}	2^{-8}	2^{-9}	2^{-10}	2^{-11}	2^{-12}	2^{-13}	2^{-14}	2^{-15}	DIGITAL VALUE

Y15	Y14	Y13	Y12	Y11	Y10	Y9	Y8	Y7	Y6	Y5	Y4	Y3	Y2	Y1	Y0	SIGNAL
-2^0	2^{-1}	2^{-2}	2^{-3}	2^{-4}	2^{-5}	2^{-6}	2^{-7}	2^{-8}	2^{-9}	2^{-10}	2^{-11}	2^{-12}	2^{-13}	2^{-14}	2^{-15}	DIGITAL VALUE

P31	P30	P29	P28	P27	P26	P25	P24	P23	P22	P21	P20	P19	P18	P17	P16	P15	P14	P13	P12	P11	P10	P9	P8	P7	P6	P5	P4	P3	P2	P1	P0	SIGNAL
-2^0	2^{-1}	2^{-2}	2^{-3}	2^{-4}	2^{-5}	2^{-6}	2^{-7}	2^{-8}	2^{-9}	2^{-10}	2^{-11}	2^{-12}	2^{-13}	2^{-14}	2^{-15}	2^0	2^{-16}	2^{-17}	2^{-18}	2^{-19}	2^{-20}	2^{-21}	2^{-22}	2^{-23}	2^{-24}	2^{-25}	2^{-26}	2^{-27}	2^{-28}	2^{-29}	2^{-30}	DIGITAL VALUE
MSP																LSP																FA = 0

P31	P30	P29	P28	P27	P26	P25	P24	P23	P22	P21	P20	P19	P18	P17	P16	P15	P14	P13	P12	P11	P10	P9	P8	P7	P6	P5	P4	P3	P2	P1	P0	SIGNAL
-2^1	2^0	2^{-1}	2^{-2}	2^{-3}	2^{-4}	2^{-5}	2^{-6}	2^{-7}	2^{-8}	2^{-9}	2^{-10}	2^{-11}	2^{-12}	2^{-13}	2^{-14}	2^{-15}	2^{-16}	2^{-17}	2^{-18}	2^{-19}	2^{-20}	2^{-21}	2^{-22}	2^{-23}	2^{-24}	2^{-25}	2^{-26}	2^{-27}	2^{-28}	2^{-29}	2^{-30}	DIGITAL VALUE
MSP																LSP																FA = 1

Fractional Two's Complement Notation

BINARY POINT

X15	X14	X13	X12	X11	X10	X9	X8	X7	X6	X5	X4	X3	X2	X1	X0	SIGNAL
-2^0	2^{-1}	2^{-2}	2^{-3}	2^{-4}	2^{-5}	2^{-6}	2^{-7}	2^{-8}	2^{-9}	2^{-10}	2^{-11}	2^{-12}	2^{-13}	2^{-14}	2^{-15}	DIGITAL VALUE

Y15	Y14	Y13	Y12	Y11	Y10	Y9	Y8	Y7	Y6	Y5	Y4	Y3	Y2	Y1	Y0	SIGNAL
2^{-1}	2^{-2}	2^{-3}	2^{-4}	2^{-5}	2^{-6}	2^{-7}	2^{-8}	2^{-9}	2^{-10}	2^{-11}	2^{-12}	2^{-13}	2^{-14}	2^{-15}	2^{-16}	DIGITAL VALUE

=	P31	P30	P29	P28	P27	P26	P25	P24	P23	P22	P21	P20	P19	P18	P17	P16	P15	P14	P13	P12	P11	P10	P9	P8	P7	P6	P5	P4	P3	P2	P1	P0	SIGNAL
	2 ⁻¹	2 ⁻²	2 ⁻³	2 ⁻⁴	2 ⁻⁵	2 ⁻⁶	2 ⁻⁷	2 ⁻⁸	2 ⁻⁹	2 ⁻¹⁰	2 ⁻¹¹	2 ⁻¹²	2 ⁻¹³	2 ⁻¹⁴	2 ⁻¹⁵	2 ⁻¹⁶	2 ⁻¹⁷	2 ⁻¹⁸	2 ⁻¹⁹	2 ⁻²⁰	2 ⁻²¹	2 ⁻²²	2 ⁻²³	2 ⁻²⁴	2 ⁻²⁵	2 ⁻²⁶	2 ⁻²⁷	2 ⁻²⁸	2 ⁻²⁹	2 ⁻³⁰	2 ⁻³¹	2 ⁻³²	DIGITAL VALUE
	MSP																LSP																FA = 1
																																	MANDATORY

Fractional Unsigned Magnitude Notation

* In this format an overflow occurs in the attempted multiplication of the two's complement number 1,000...0 with 1,000.0 yielding an erroneous product of -1 in the fraction case and -2^{30} in the integer case.

BINARY POINT

X15	X14	X13	X12	X11	X10	X9	X8	X7	X6	X5	X4	X3	X2	X1	X0	SIGNAL (TWO'S COMPONENT) DIGITAL VALUE
-2 ⁰	2 ⁻¹	2 ⁻²	2 ⁻³	2 ⁻⁴	2 ⁻⁵	2 ⁻⁶	2 ⁻⁷	2 ⁻⁸	2 ⁻⁹	2 ⁻¹⁰	2 ⁻¹¹	2 ⁻¹²	2 ⁻¹³	2 ⁻¹⁴	2 ⁻¹⁵	

X																SIGNAL (UNSIGNED MAGNITUDE) DIGITAL VALUE
Y15	Y14	Y13	Y12	Y11	Y10	Y9	Y8	Y7	Y6	Y5	Y4	Y3	Y2	Y1	Y0	
2 ⁻¹	2 ⁻²	2 ⁻³	2 ⁻⁴	2 ⁻⁵	2 ⁻⁶	2 ⁻⁷	2 ⁻⁸	2 ⁻⁹	2 ⁻¹⁰	2 ⁻¹¹	2 ⁻¹²	2 ⁻¹³	2 ⁻¹⁴	2 ⁻¹⁵	2 ⁻¹⁶	

P31	P30	P29	P28	P27	P26	P25	P24	P23	P22	P21	P20	P19	P18	P17	P16	P15	P14	P13	P12	P11	P10	P9	P8	P7	P6	P5	P4	P3	P2	P1	P0	SIGNAL DIGITAL VALUE FA = 1
-2 ⁰	2 ⁻¹	2 ⁻²	2 ⁻³	2 ⁻⁴	2 ⁻⁵	2 ⁻⁶	2 ⁻⁷	2 ⁻⁸	2 ⁻⁹	2 ⁻¹⁰	2 ⁻¹¹	2 ⁻¹²	2 ⁻¹³	2 ⁻¹⁴	2 ⁻¹⁵	2 ⁻¹⁶	2 ⁻¹⁷	2 ⁻¹⁸	2 ⁻¹⁹	2 ⁻²⁰	2 ⁻²¹	2 ⁻²²	2 ⁻²³	2 ⁻²⁴	2 ⁻²⁵	2 ⁻²⁶	2 ⁻²⁷	2 ⁻²⁸	2 ⁻²⁹	2 ⁻³⁰	2 ⁻³¹	

LSP

MSP

MANDATORY

Fractional Mixed Mode Notation

BINARY POINT

X15	X14	X13	X12	X11	X10	X9	X8	X7	X6	X5	X4	X3	X2	X1	X0	SIGNAL DIGITAL VALUE
-2 ⁻¹⁵	2 ⁻¹⁴	2 ⁻¹³	2 ⁻¹²	2 ⁻¹¹	2 ⁻¹⁰	2 ⁻⁹	2 ⁻⁸	2 ⁻⁷	2 ⁻⁶	2 ⁻⁵	2 ⁻⁴	2 ⁻³	2 ⁻²	2 ⁻¹	2 ⁰	

X																SIGNAL DIGITAL VALUE
Y15	Y14	Y13	Y12	Y11	Y10	Y9	Y8	Y7	Y6	Y5	Y4	Y3	Y2	Y1	Y0	
-2 ⁻¹⁵	2 ⁻¹⁴	2 ⁻¹³	2 ⁻¹²	2 ⁻¹¹	2 ⁻¹⁰	2 ⁻⁹	2 ⁻⁸	2 ⁻⁷	2 ⁻⁶	2 ⁻⁵	2 ⁻⁴	2 ⁻³	2 ⁻²	2 ⁻¹	2 ⁰	

LSP

MSP

FA = 0

P31	P30	P29	P28	P27	P26	P25	P24	P23	P22	P21	P20	P19	P18	P17	P16	P15	P14	P13	P12	P11	P10	P9	P8	P7	P6	P5	P4	P3	P2	P1	P0	SIGNAL DIGITAL VALUE FA = 1
-2 ⁻³⁰	2 ⁻²⁹	2 ⁻²⁸	2 ⁻²⁷	2 ⁻²⁶	2 ⁻²⁵	2 ⁻²⁴	2 ⁻²³	2 ⁻²²	2 ⁻²¹	2 ⁻²⁰	2 ⁻¹⁹	2 ⁻¹⁸	2 ⁻¹⁷	2 ⁻¹⁶	2 ⁻¹⁵	2 ⁻¹⁴	2 ⁻¹³	2 ⁻¹²	2 ⁻¹¹	2 ⁻¹⁰	2 ⁻⁹	2 ⁻⁸	2 ⁻⁷	2 ⁻⁶	2 ⁻⁵	2 ⁻⁴	2 ⁻³	2 ⁻²	2 ⁻¹	2 ⁰		

LSP

MSP

Integer Two's Complement Notation

* In this format an overflow occurs in the attempted multiplication of the two's complement number 1,000...0 with 1,000.0 yielding an erroneous product of -1 in the fraction case and -2⁻³⁰ in the integer case.

BINARY POINT

X15	X14	X13	X12	X11	X10	X9	X8	X7	X6	X5	X4	X3	X2	X1	X0	SIGNAL
2 ¹⁵	2 ¹⁴	2 ¹³	2 ¹²	2 ¹¹	2 ¹⁰	2 ⁹	2 ⁸	2 ⁷	2 ⁶	2 ⁵	2 ⁴	2 ³	2 ²	2 ¹	2 ⁰	DIGITAL VALUE

X

Y15	Y14	Y13	Y12	Y11	Y10	Y9	Y8	Y7	Y6	Y5	Y4	Y3	Y2	Y1	Y0	SIGNAL
2 ¹⁵	2 ¹⁴	2 ¹³	2 ¹²	2 ¹¹	2 ¹⁰	2 ⁹	2 ⁸	2 ⁷	2 ⁶	2 ⁵	2 ⁴	2 ³	2 ²	2 ¹	2 ⁰	DIGITAL VALUE

P31	P30	P29	P28	P27	P26	P25	P24	P23	P22	P21	P20	P19	P18	P17	P16	P15	P14	P13	P12	P11	P10	P9	P8	P7	P6	P5	P4	P3	P2	P1	P0	SIGNAL
2 ³¹	2 ³⁰	2 ²⁹	2 ²⁸	2 ²⁷	2 ²⁶	2 ²⁵	2 ²⁴	2 ²³	2 ²²	2 ²¹	2 ²⁰	2 ¹⁹	2 ¹⁸	2 ¹⁷	2 ¹⁶	2 ¹⁵	2 ¹⁴	2 ¹³	2 ¹²	2 ¹¹	2 ¹⁰	2 ⁹	2 ⁸	2 ⁷	2 ⁶	2 ⁵	2 ⁴	2 ³	2 ²	2 ¹	2 ⁰	DIGITAL VALUE
																FA = 1																MANDATORY

MSP

LSP

Integer Unsigned Magnitude Notation

BINARY POINT

X15	X14	X13	X12	X11	X10	X9	X8	X7	X6	X5	X4	X3	X2	X1	X0	SIGNAL
-2 ¹⁵	2 ¹⁴	2 ¹³	2 ¹²	2 ¹¹	2 ¹⁰	2 ⁹	2 ⁸	2 ⁷	2 ⁶	2 ⁵	2 ⁴	2 ³	2 ²	2 ¹	2 ⁰	TWO'S COMPLEMENT) DIGITAL VALUE

SIGNAL (UNSIGNED MAGNITUDE)
DIGITAL VALUE

Y15	Y14	Y13	Y12	Y11	Y10	Y9	Y8	Y7	Y6	Y5	Y4	Y3	Y2	Y1	Y0	SIGNAL
2 ¹⁵	2 ¹⁴	2 ¹³	2 ¹²	2 ¹¹	2 ¹⁰	2 ⁹	2 ⁸	2 ⁷	2 ⁶	2 ⁵	2 ⁴	2 ³	2 ²	2 ¹	2 ⁰	(UNSIGNED MAGNITUDE) DIGITAL VALUE

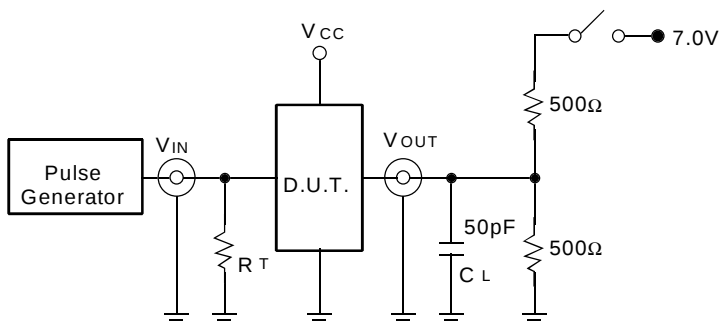
X

P31	P30	P29	P28	P27	P26	P25	P24	P23	P22	P21	P20	P19	P18	P17	P16	P15	P14	P13	P12	P11	P10	P9	P8	P7	P6	P5	P4	P3	P2	P1	P0	SIGNAL
-2 ³¹	2 ³⁰	2 ²⁹	2 ²⁸	2 ²⁷	2 ²⁶	2 ²⁵	2 ²⁴	2 ²³	2 ²²	2 ²¹	2 ²⁰	2 ¹⁹	2 ¹⁸	2 ¹⁷	2 ¹⁶	2 ¹⁵	2 ¹⁴	2 ¹³	2 ¹²	2 ¹¹	2 ¹⁰	2 ⁹	2 ⁸	2 ⁷	2 ⁶	2 ⁵	2 ⁴	2 ³	2 ²	2 ¹	2 ⁰	DIGITAL VALUE
																FA = 1																MANDATORY

MSP

LSP

Integer Mixed Mode Notation



AC Test Circuit

AC TEST CONDITIONS

Input Pulse Levels	GND to 3V
Input Rise/Fall Times	3ns
Input Timing Reference Labels	1.5V
Output Reference Levels	1.5V
Output Load	See Figure 1

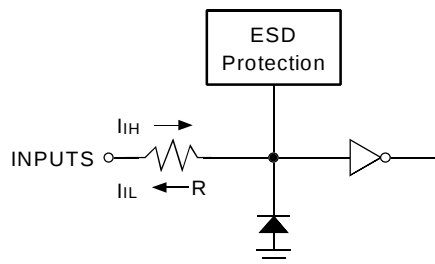
SWITCH POSITION

Test	Switch
Disable Low	Closed
Enable Low	Closed
All Other Tests	Open

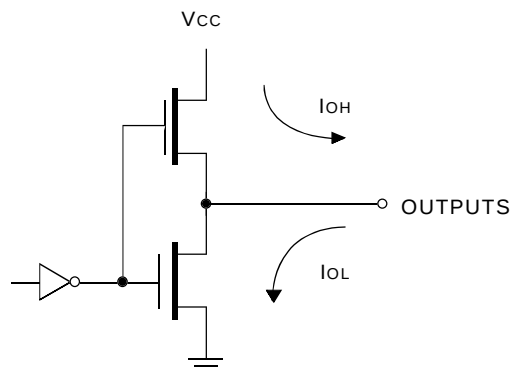
DEFINITIONS:

C_L = Load capacitance: includes jig and probe capacitance.

R_T = Termination resistance: should be equal to Z_{OUT} of the Pulse Generator.

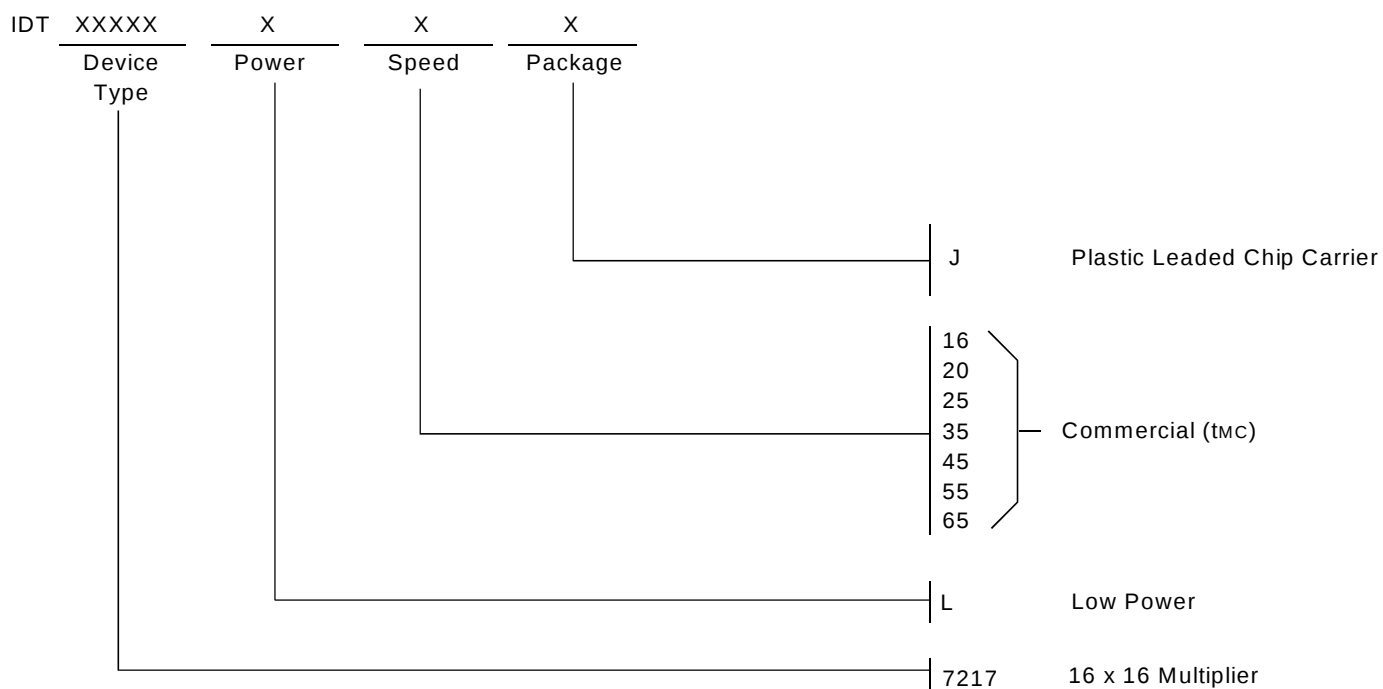


Input Interface Circuit



Output Interface Circuit

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