16-BIT PARALLEL CMOS MULTIPLIERS

IDT7216L

FEATURES:

- **16 x 16 parallel multiplier with double precision product**
- **16ns clocked multiply time**
- **Low power consumption: 120mA**
- **Produced with advanced submicron CMOS high performance technology**
- **IDT7216L is pin- and function compatible with TRW MPY016H/K and AMD Am29516**
- **Configured for easy array expansion**
- **User-controlled option for transparent output register mode**
- **Round control for rounding the MSP**
- **Input and output directly TTL-compatible**
- **Three-state output**
- **Available in PLCC**
- **Speeds available: L16/20/25/35/45/55/65**

DESCRIPTION:

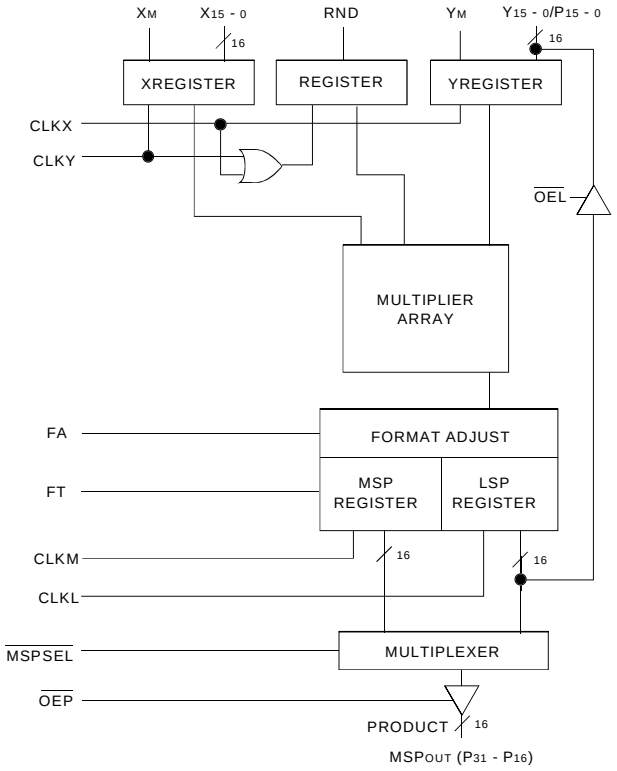
The IDT7216 is a high-speed, low-power 16 x 16-bit multiplier, ideal for fast, real time digital signal processing applications. Utilization of a modified Booths algorithm and IDT's high-performance, submicron CMOS technology, has achieved speeds comparable to bipolar (20ns max.), at 1/10 the power consumption.

The IDT7216 is ideal for applications requiring high-speed multiplication such as fast Fourier transform analysis, digital filtering, graphic display systems, speech synthesis and recognition and in any system requirement where multiplication speeds of a mini/microcomputer are inadequate.

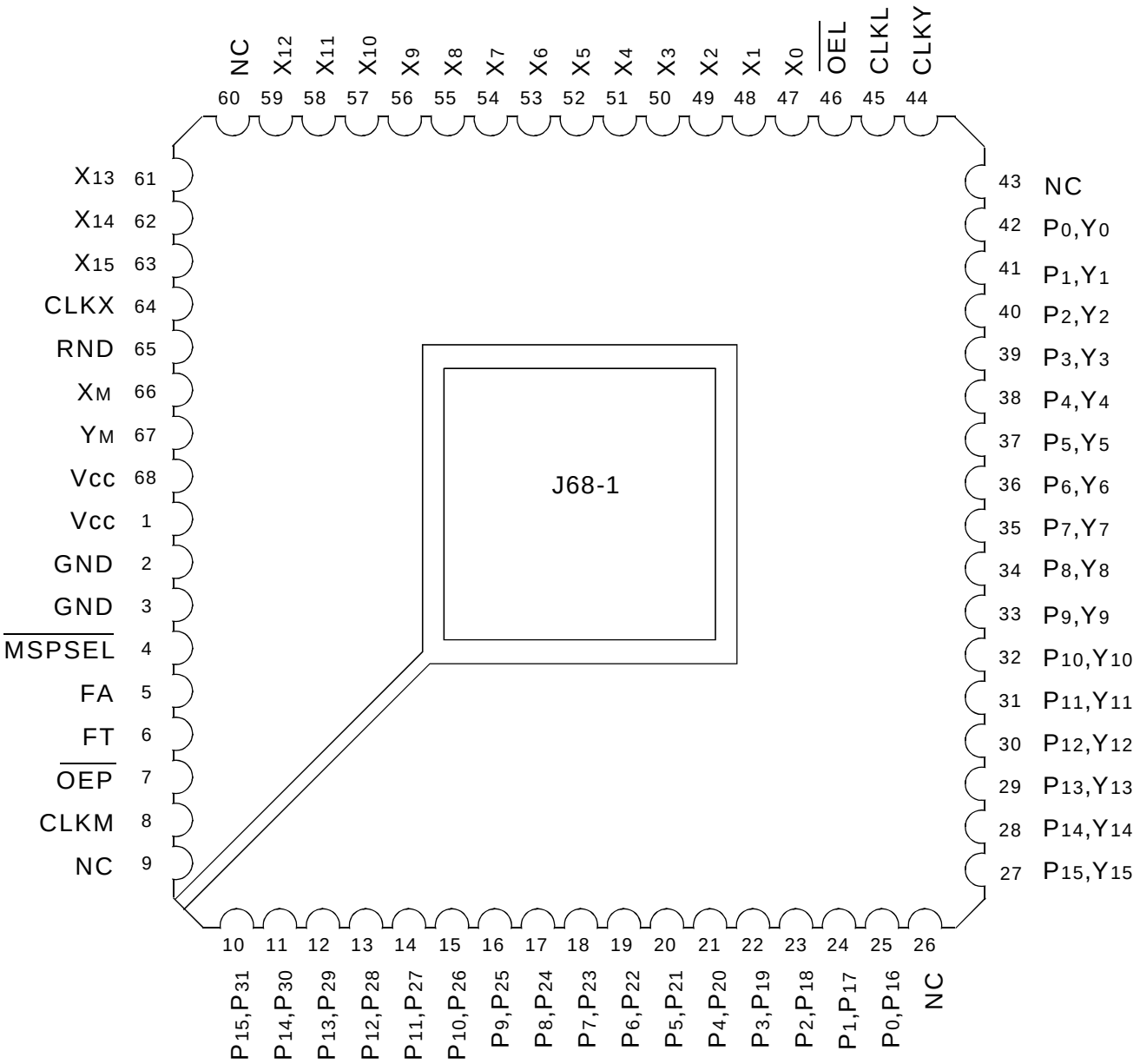
All input registers, as well as LSP and MSP output registers, use the same positive edge-triggered D-type flip-flop. In the IDT7216, there are independent clocks (CLKX, CLKY, CLKM, CLKL) associated with each of these registers.

The IDT7216 offers additional flexibility with the FA control and $\overline{\text{MSPSEL}}$ functions. The FA control formats the output for two's complement by shifting the MSP up one bit and then repeating the sign bit in the MSB of the LSP. The $\overline{\text{MSPSEL}}$ low selects the MSP to be available at the product output port, while a high selects the LSP to be available. Keeping this pin low will ensure compatibility with the TRW MPY016H.

FUNCTIONAL BLOCK DIAGRAM



PIN CONFIGURATION



PLCC
TOP VIEW

ABSOLUTE MAXIMUM RATINGS(1)

Symbol	Description	Max	Unit
V_{CC}	Power Supply Voltage	–0.5 to +7	V
V_{TERM}	Terminal Voltage with Respect to GND	V_{CC} + 0.5	V
T_A	Operating Temperature	0 to +70	° C
T_{BIAS}	Temperature Under Bias	–55 to +125	° C
T_{STG}	Storage Temperature	–55 to +125	° C
I_{OUT}	DC Output Current	50	mA

NOTE:
1. Stresses greater than those listed under ABSOLUTE MAXIMUM RATINGS may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect reliability.

CAPACITANCE (T_A = +25°C, F = 1.0MHz)

Symbol	Parameter(1)	Conditions	Max.	Unit
C_{IN}	Input Capacitance	V_{IN} = 0V	10	pF
C_{OUT}	Output Capacitance	V_{OUT} = 0V	12	pF

NOTE:
1. This parameter is sampled and not 100% tested.

PIN DESCRIPTION

Pin Name	I/O	Description
X_0 - X_{15}	I	Data Inputs
Y_0 - Y_{15}/ P_0 - P_{15}	I/O	Y_0 - Y_{15} are data inputs P_0 - P_{15} are LSP register output, enabled when $\overline{OEL}$ = 0
P_{16} - P_{31}	O	Data Output (LSP or MSP)
$\overline{OEL}$	I	Output enable control for LSP (least significant product). When LOW enables P_0 - P_{15}. When HIGH P_0 - P_{15} tristated.
$\overline{OEP}$	I	Output enable control for MSP (most significant product). When LOW enables P_{16} - P_{31}. When HIGH P_{16} - P_{31} tristated.
X_M, Y_M	I	Mode control for each data word. LOW designates unsigned data input and HIGH designates two's complement.
RND	I	"Round" control for rounding of MSP. When HIGH, 1 is added to the most significant bit of LSP. This signal is affected by the state of FA pin. When FA = 1 and RND = 1, 1 is added to the 2^{-15} bit (P_{15}). When RND = 1 and FA = 0, 1 is added to the 2^{-16} bit (P_{14}). The RND input is registered. It is clocked on the rising edge of the logical OR of CLKX and CLKY. Rounding always occurs in the positive direction which may introduce a systematic bias.
$\overline{MSPSEL}$	I	When LOW, MSP is output on P_{16} - P_{31} lines. When HIGH, LSP is output on P_{16} - P_{31}.
FA	I	Format adjust control. When HIGH, a full 32 bit product is selected. When LOW, a left shifted 31 bit product is selected with the sign bit replicated in the LSP. FA is normally HIGH, except for certain fractional two's complement applications (see multiplier input / output formats).
FT	I	Flow through control. When HIGH, both MSP and LSP registers are by-passed.
CLKX	I	X register clock input. Also clocks RND register.
CLKY	I	Y register clock input. Also clocks RND register.
CLKL	I	LSP register clock input.
CLKM	I	MSP register clock input.

DC ELECTRICAL CHARACTERISTICS OVER OPERATING RANGE

Following Conditions Apply Unless Otherwise Specified:
Commercial: T_A = 0°C to +70°C, V_{CC} = 5V ± 10%

Symbol	Parameter	Test Conditions[1]	Min.	Typ.[1]	Max.	Unit
V_{IH}	Input HIGH Voltage	Guaranteed Logic HIGH Level	2	—	—	V
V_{IL}	Input LOW Voltage	Guaranteed Logic LOW Level	—	—	0.8	V
I_{LI}	Input Leakage Current	V_{CC} = Max., V_{IN} = 0 to V_{CC}	—	—	10	µA
I_{LO}	Output Leakage Current	V_{CC} = Max., $\overline{OE}$ = 2V, V_{OUT} = 0 to V_{CC}	—	—	10	µA
I_{CC}	Operating Power Supply Current	V_{CC} = Max., Outputs Disabled, f = 10MHz[2]	—	40	80	mA
I_{CCQ1}	Quiescent Power Supply Current	$V_{IN} \geq V_{IH}$, $V_{IN} \leq V_{IL}$	—	20	40	mA
I_{CCQ2}	Quiescent Power Supply Current	$V_{IN} \geq V_{CC}$ - 0.2V, $V_{IN} \leq$ 0.2V	—	4	20	mA
I_{CC}/f[2,3]	Increase in Power Supply Current	V_{CC} = Max., Outputs Disabled	—	—	4	mA/MHz
V_{OH}	Output HIGH Voltage	V_{CC} = Min., I_{OH} = –2mA	2.4	—	—	V
V_{OL}[4]	Output LOW Voltage	V_{CC} = Min., I_{OL} = 8mA	—	—	0.4	V
I_{OS}	Output Short Circuit Current	V_{CC} = Max., V_O = GND	-20	—	-120	mA

NOTES:
1. Typical implies V_{CC} = 5V and T_A = +25°C.
2. I_{CC} is measured at 10MHz and V_{IN} = 0 to 3V. For frequencies greater than 10MHz, the following equation is used for the commercial range: I_{CC} = 80+ 4(f –10)mA; for the military range, I_{CC} = 100 + 6(f –10). f = operating frequency in MHz and f = 1/t_{MC}.
3. For frequencies greater than 10MHz, guaranteed by design, not production tested.
4. I_{OL} = 4mA for t_{MC} >65ns.

AC ELECTRICAL CHARACTERISTICS

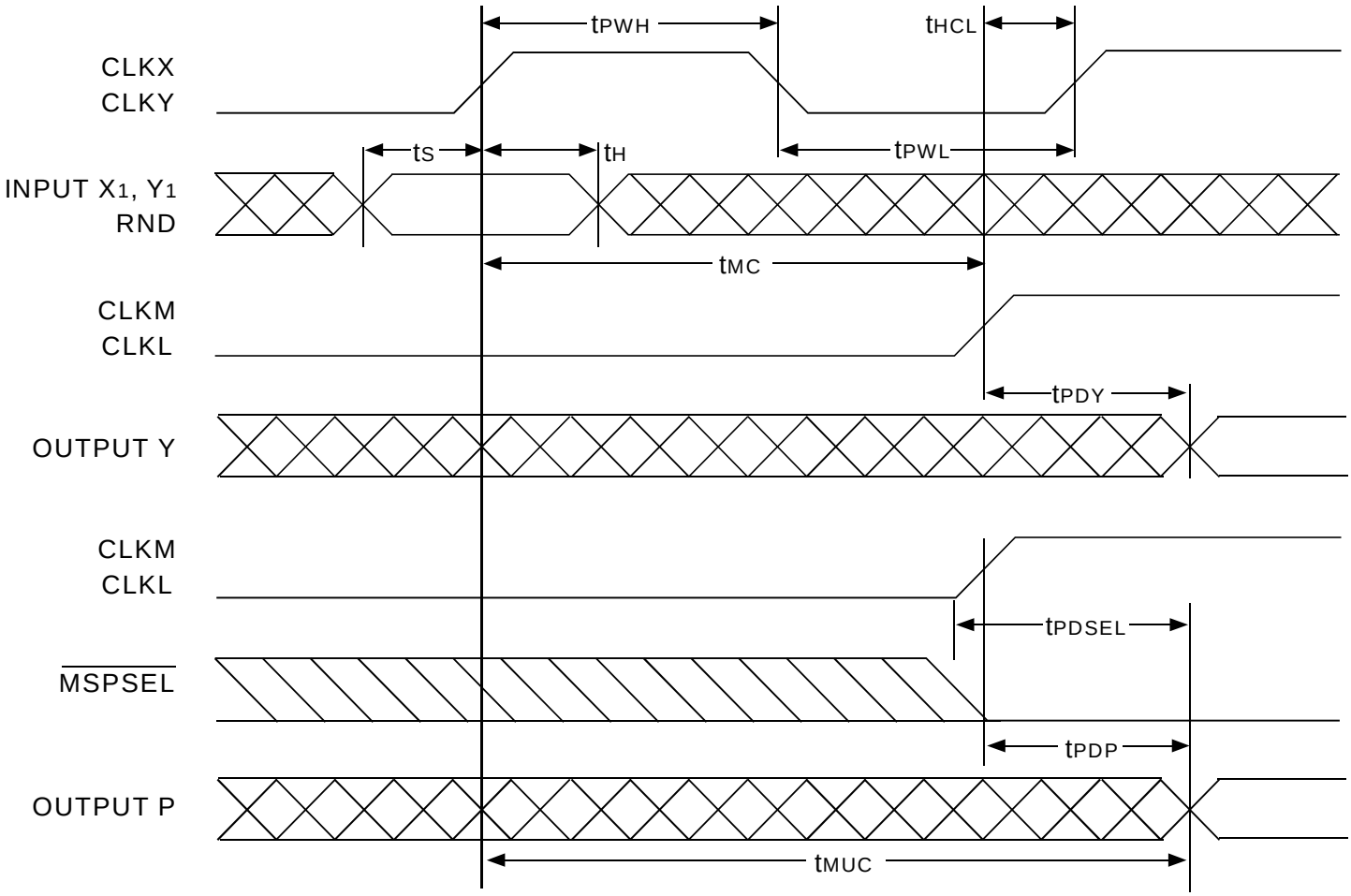
Following Conditions Apply Unless Otherwise Specified:
Commercial: T_A = 0°C to +70°C, V_{CC} = 5V ± 10%

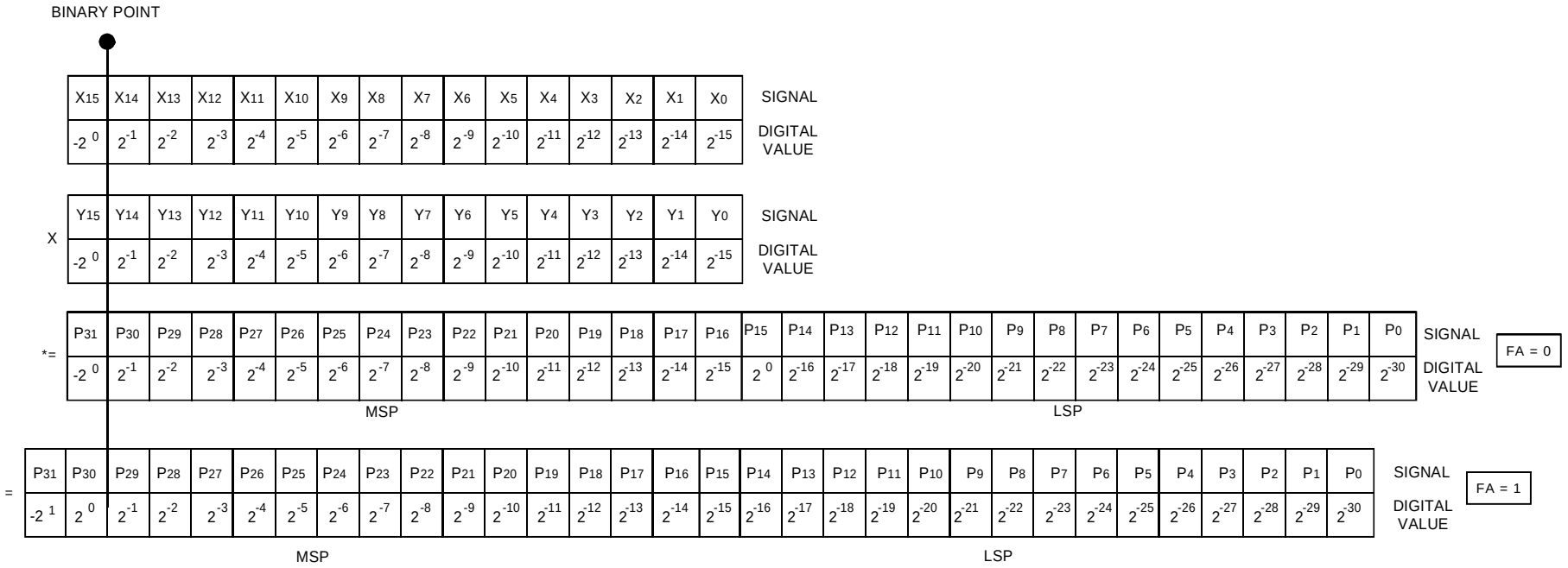
Symbol	Parameter	7216L16		7216L20		7216L25		7216L35		Unit
		Min.	Max.	Min.	Max.	Min.	Max.	Min.	Max.	
t_{MUC}	Unclocked Multiply Time[4]	2	25	2	30	2	38	2	55	ns
t_{MC}	Clocked Multiply Time[4]	2	16	2	20	2	25	2	35	ns
t_S	X, Y, RND Set-up Time	10	—	11	—	12	—	12	—	ns
t_H	X, Y, RND Hold Time	1	—	1	—	2	—	3	—	ns
t_{PWH}	Clock Pulse Width HIGH	7	—	9	—	10	—	10	—	ns
t_{PWL}	Clock Pulse Width LOW	7	—	9	—	10	—	10	—	ns
t_{PDSEL}	$\overline{\text{MSPSEL}}$ to Product Out[4]	2	15	2	18	2	20	2	25	ns
t_{PDP}	Output Clock to P[4]	2	15	2	18	2	20	2	25	ns
t_{PDY}	Output Clock to Y[4]	2	15	2	18	2	20	2	25	ns
t_{ENA}	3-State Enable Time	—	15	—	18	—	20	—	25	ns
t_{DIS}	3-State Disable Time[2]	—	15	—	18	—	20	—	22	ns
t_{HCL}	Clock LOW Hold Time CLKXY Relative to CLKML [1,3]	0	—	0	—	0	—	0	—	ns

Symbol	Parameter	7216L45		7216L55		7216L65		Unit
		Min.	Max.	Min.	Max.	Min.	Max.	
t_{MUC}	Unclocked Multiply Time[4]	2	65	2	75	2	85	ns
t_{MC}	Clocked Multiply Time[4]	2	45	2	55	2	65	ns
t_S	X, Y, RND Set-up Time	15	—	20	—	20	—	ns
t_H	X, Y, RND Hold Time	3	—	3	—	3	—	ns
t_{PWH}	Clock Pulse Width HIGH	15	—	15	—	15	—	ns
t_{PWL}	Clock Pulse Width LOW	15	—	20	—	20	—	ns
t_{PDSEL}	$\overline{\text{MSPSEL}}$ to Product Out[4]	2	25	2	25	2	30	ns
t_{PDP}	Output Clock to P[4]	2	25	2	30	2	30	ns
t_{PDY}	Output Clock to Y[4]	2	25	2	30	2	30	ns
t_{ENA}	3-State Enable Time	—	25	—	30	—	35	ns
t_{DIS}	3-State Disable Time[2]	—	22	—	25	—	25	ns
t_{HCL}	Clock LOW Hold Time CLKXY Relative to CLKML [1,3]	0	—	0	—	0	—	ns

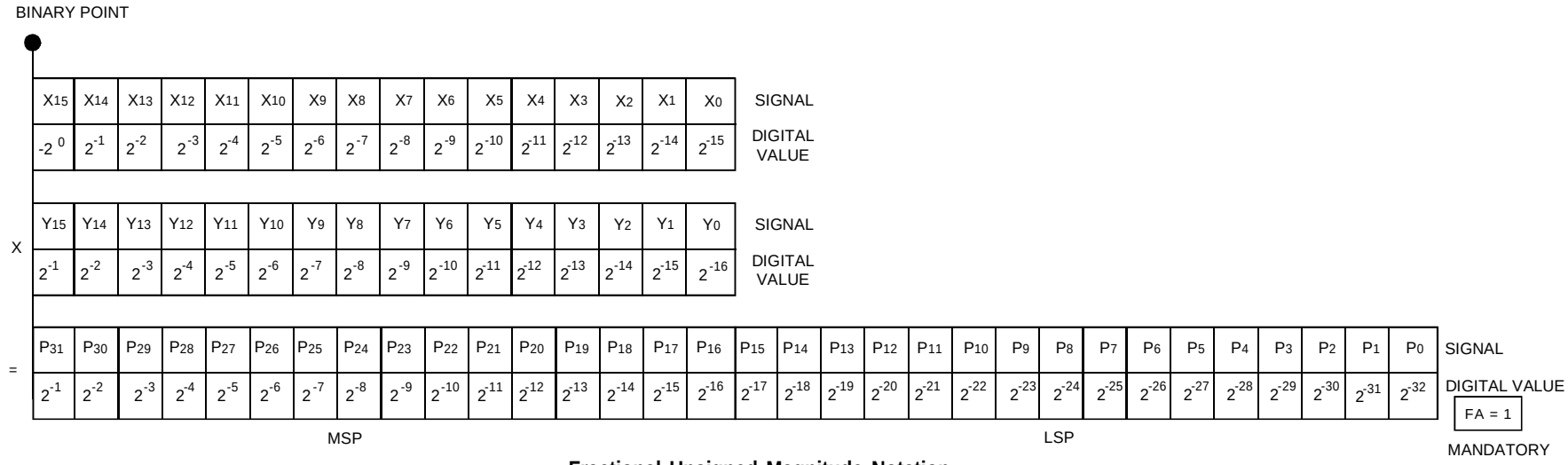
NOTES:
1. To ensure that the correct product is entered in the output registers, new data may not be entered into the registers before the output registers have been clocked.
2. Transition is measured ±500mV from steady state voltage.
3. Guaranteed by design, not production tested.
4. Minimum propagation delay times are guaranteed, not production tested.

TIMING DIAGRAM



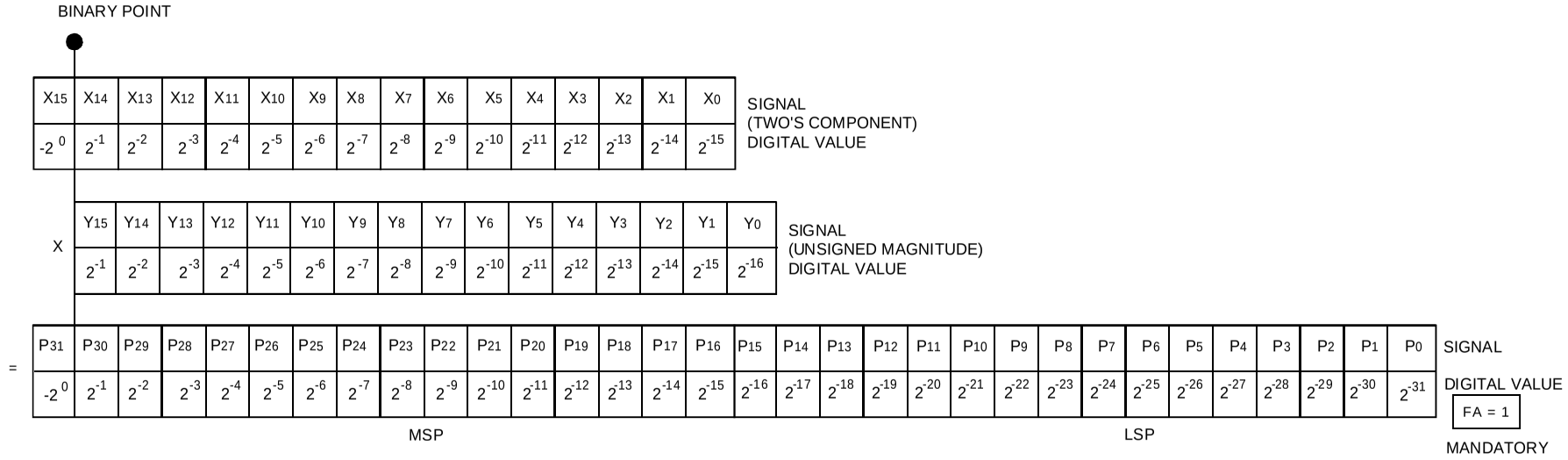


Fractional Two's Complement Notation

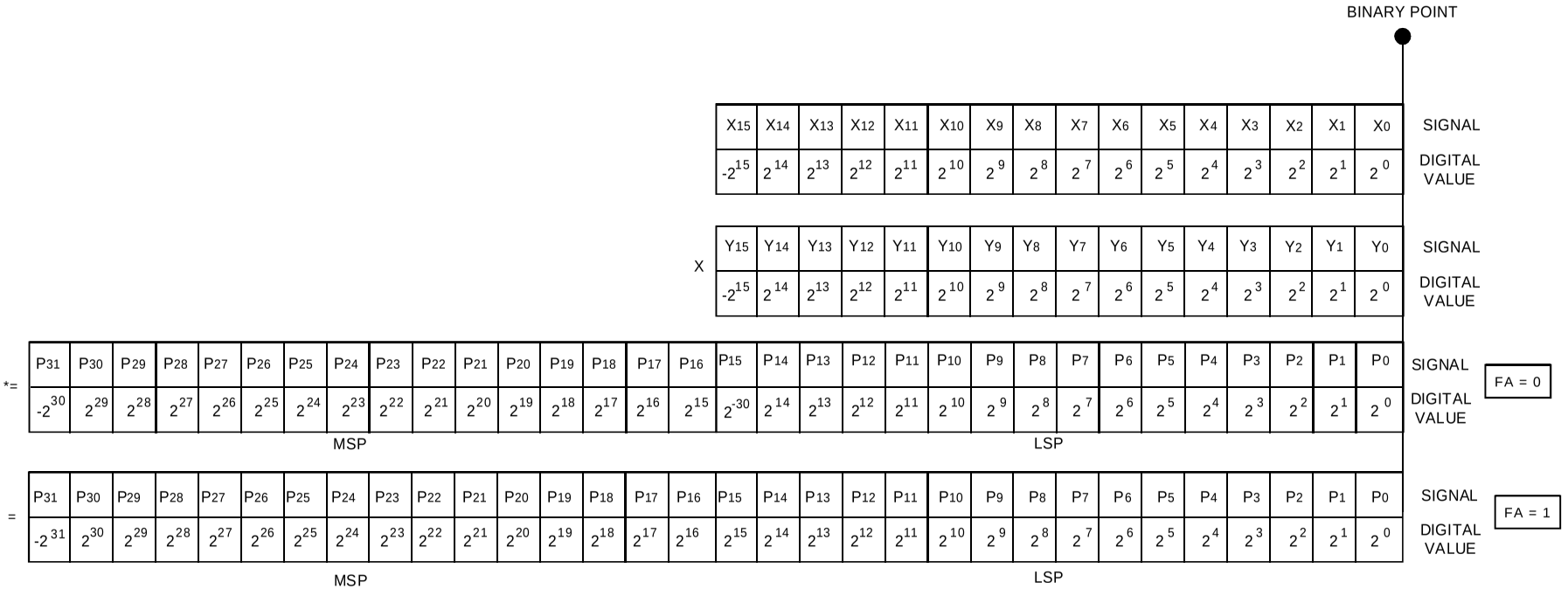


Fractional Unsigned Magnitude Notation

* In this format an overflow occurs in the attempted multiplication of the two's complement number 1,000...0 with 1,000.0 yeilding an erroneous product of -1 in the fraction case and -2^{30} in the integer case.

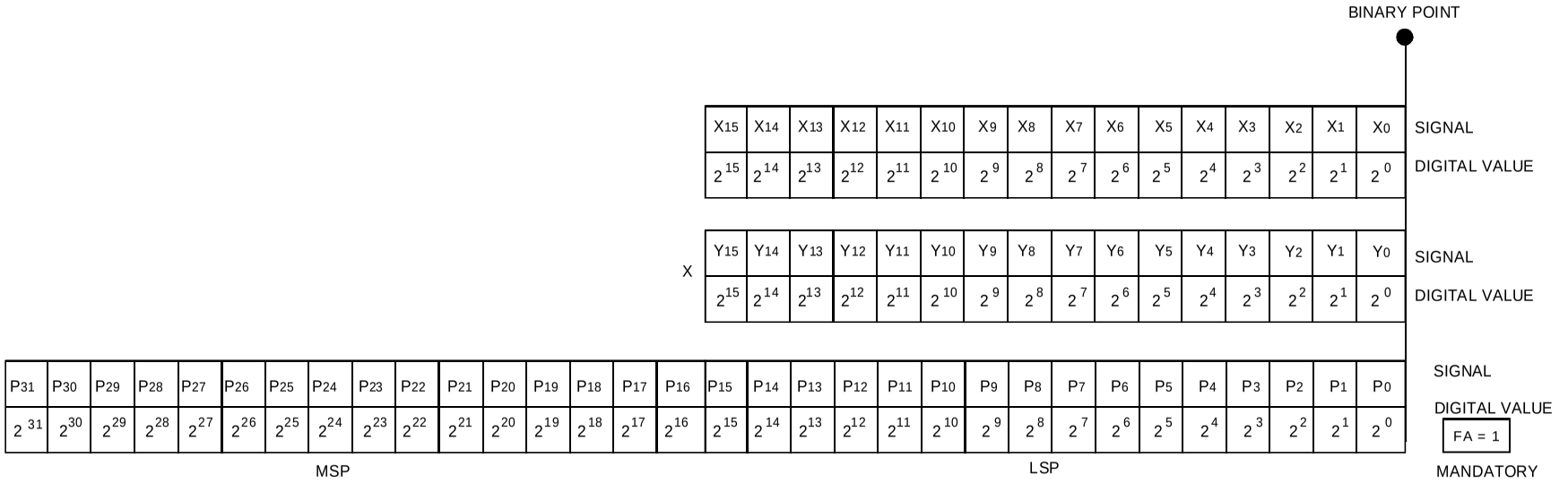


Fractional Mixed Mode Notation

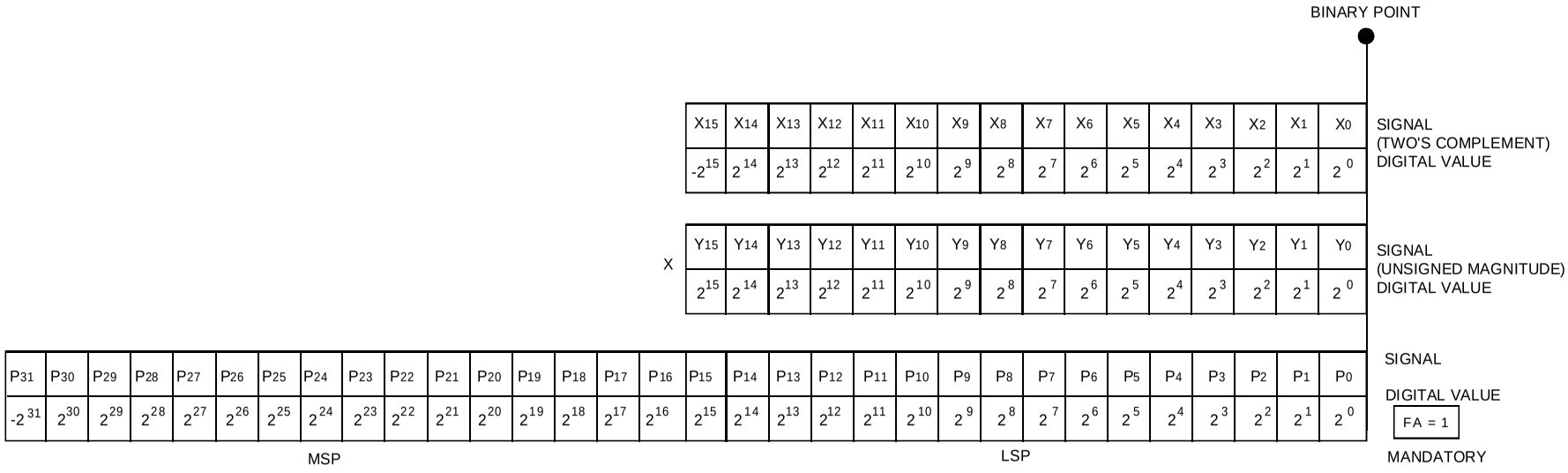


Integer Two's Complement Notation

* In this format an overflow occurs in the attempted multiplication of the two's complement number 1,000...0 with 1,000.0 yeilding an erroneous product of -1 in the fraction case and -2^{30} in the integer case.

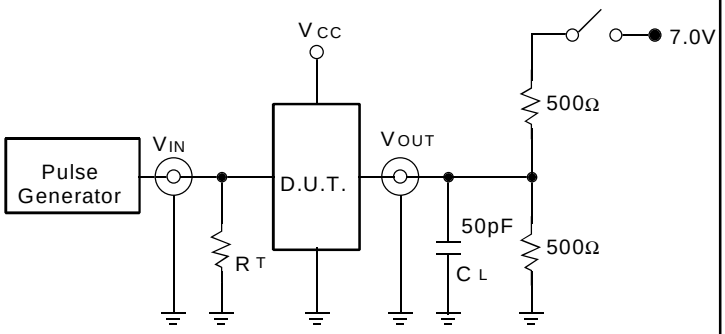


Integer Unsigned Magnitude Notation

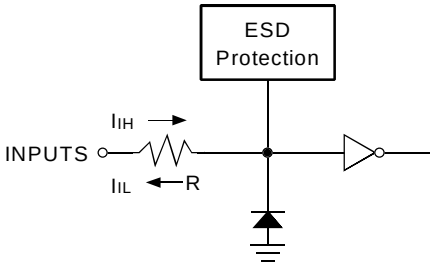


Integer Mixed Mode Notation

TEST CIRCUITS AND WAVEFORMS



AC Test Circuit



Input Interface Circuit

AC TEST CONDITIONS

Input Pulse Levels	GND to 3V
Input Rise/Fall Times	3ns
Input Timing Reference Levels	1.5V
Output Reference Levels	1.5V
Output Load	See Figure 1

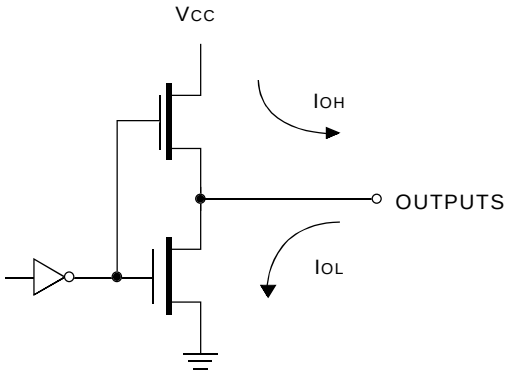
SWITCH POSITION

Test	Switch
Disable Low Enable Low	Closed
All Other Tests	Open

DEFINITIONS:

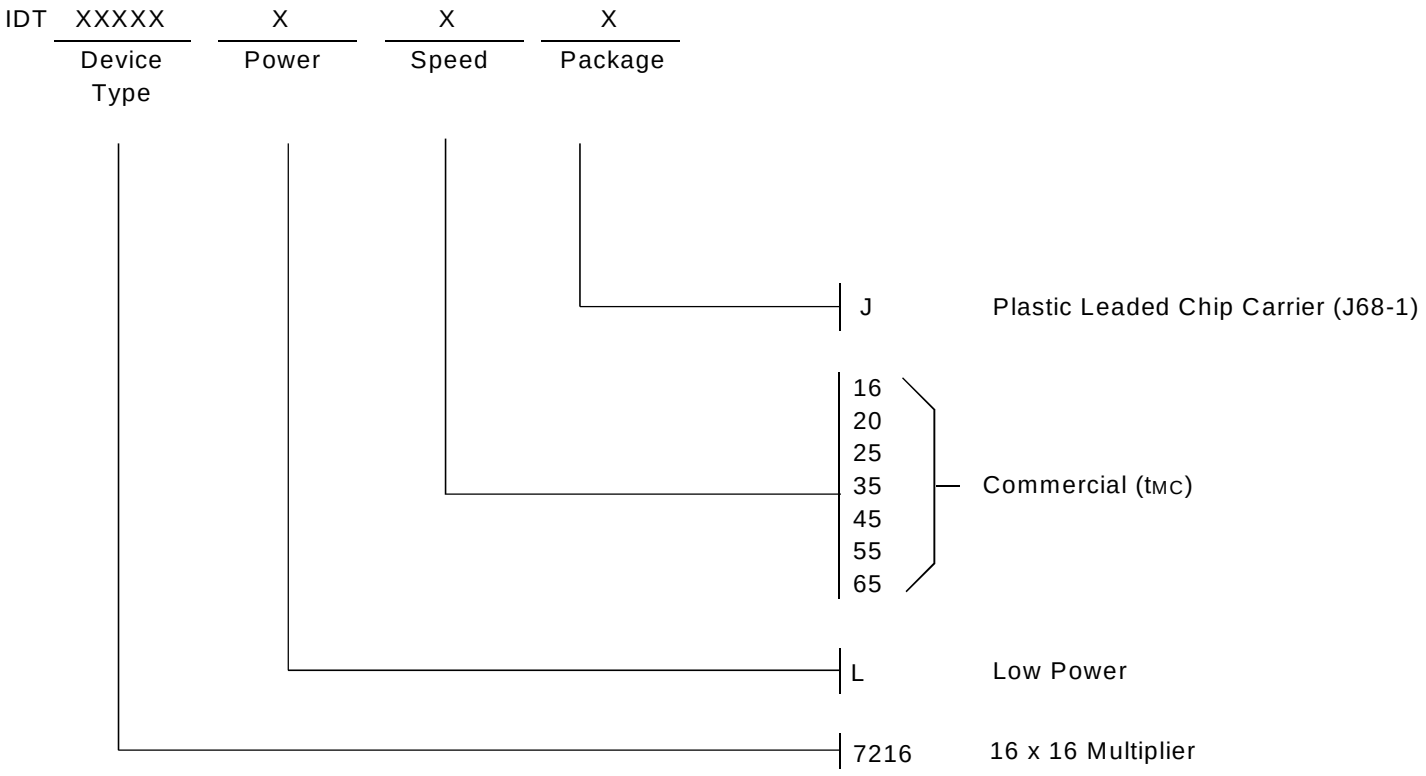
C_L = Load capacitance: includes jig and probe capacitance.

R_T = Termination resistance: should be equal to Z_{OUT} of the Pulse Generator.



Output Interface Circuit

ORDERING INFORMATION



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