64-BIT FLOW-THRU ERROR DETECTION AND CORRECTION UNIT

IDT49C465
IDT49C465A

FEATURES:

- 32-bit wide Flow-thruEDC™ unit, cascadable to 64 bits
- Single-chip 64-bit Generate Mode
- Separate system and memory buses
- On-chip pipeline latch with external control
- Supports bidirectional and common I/O memories
- Corrects all single-bit errors
- Detects all double-bit errors and some multiple bit errors
- Error Detection Time — 12ns
- Error Correction Time — 14ns
- On chip diagnostic registers
- Parity generation and checking on system data bus
- Low power CMOS — 100mA typical at 20MHz
- 144-pin PGA and PQFP packages

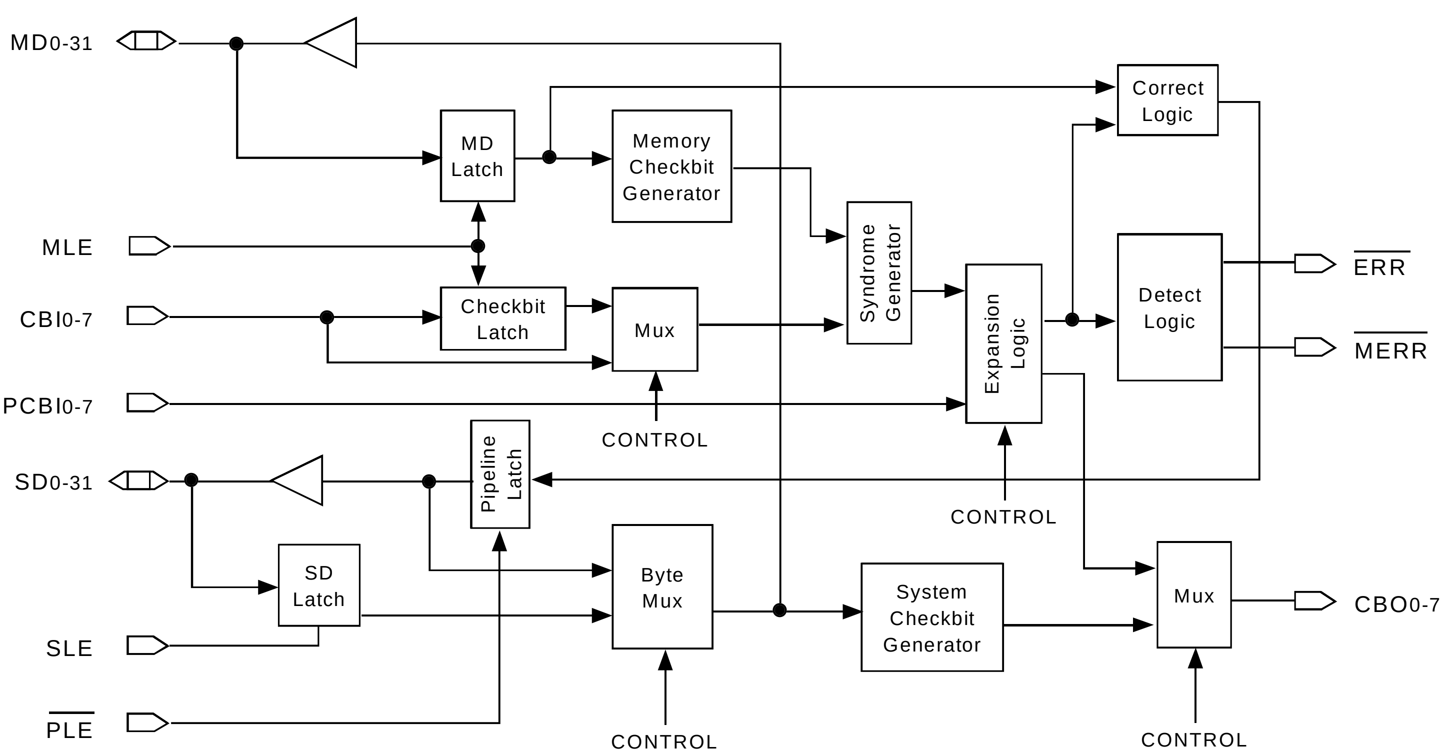
DESCRIPTION:

The IDT49C465/A is a 32-bit, two-data bus, Flow-thruEDC unit. The chip provides single-error correction and two and three bit error detection of both hard and soft memory errors. It can be expanded to 64-bit widths by cascading two units, without the need for additional external logic. The Flow-thruEDC has been optimized for speed and simplicity of control.

The EDC unit has been designed for use in either of two configurations in an error correcting memory system. The bidirectional configuration is most appropriate for systems using bidirectional memory buses. A second system configuration utilizes external octal buffers, and is well-suited for systems using memory with separate I/O buses.

The IDT49C465/A supports partial word writes, pipelining, and error diagnostics. It also provides parity protection for data on the system side.

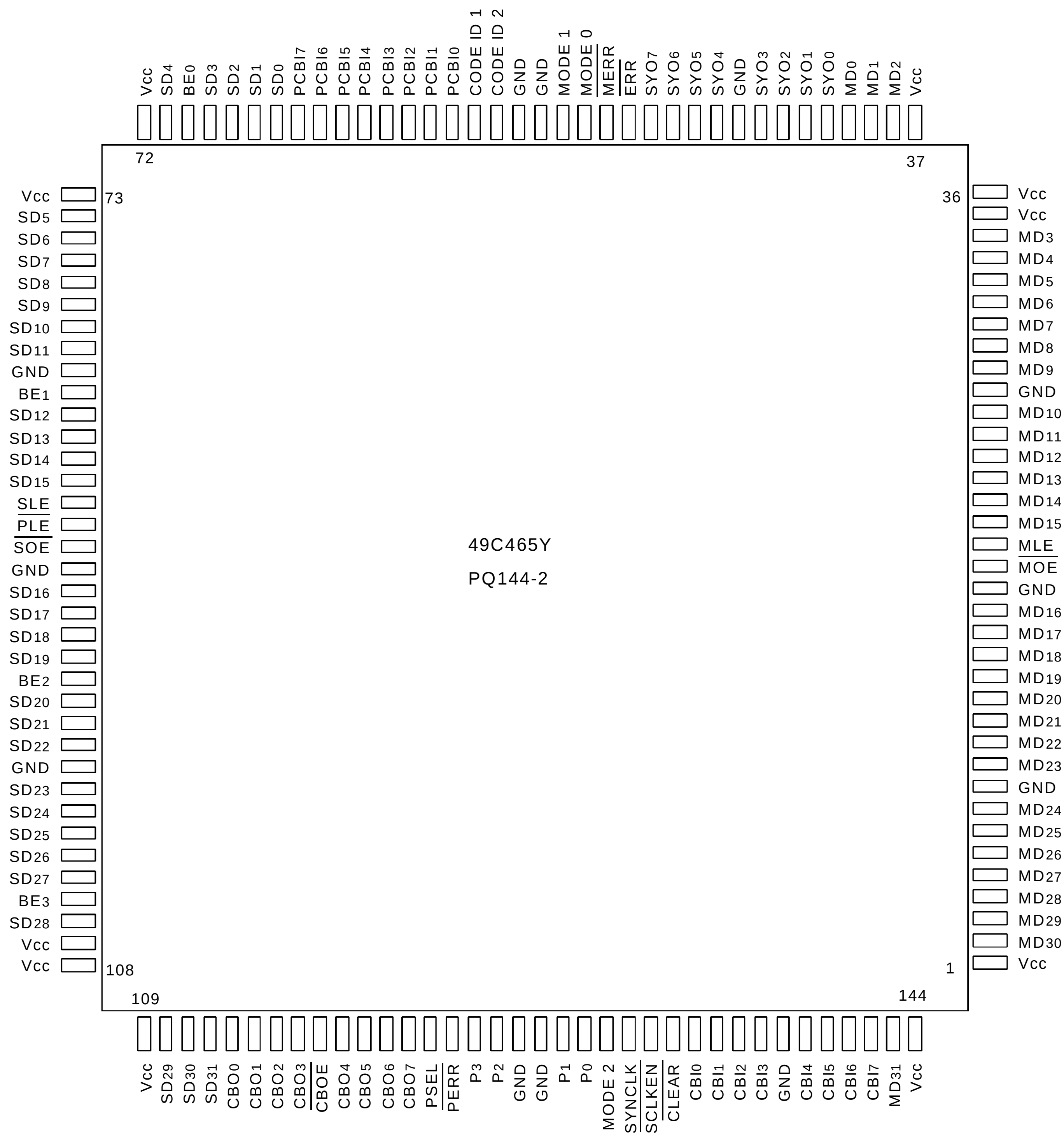
SIMPLIFIED FUNCTIONAL BLOCK DIAGRAM



COMMERCIAL TEMPERATURE RANGE

NOVEMBER 2000

PIN CONFIGURATION



PQFP
TOP VIEW

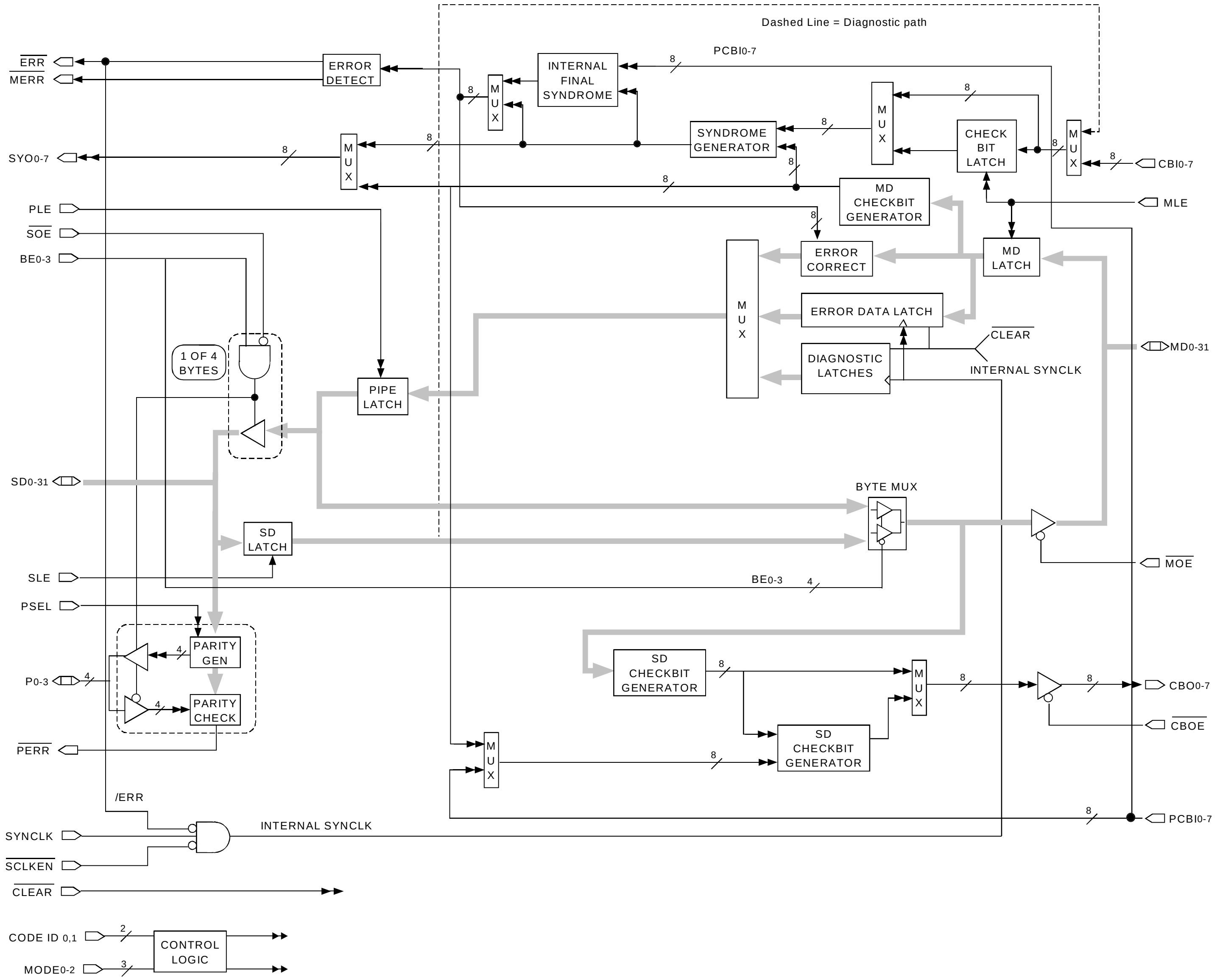
PIN CONFIGURATION

	A	B	C	D	E	F	G	H	J	K	L	M	N	P	R
15	Vcc	SD2	PCBI6	PCBI5	PCBI3	CODE ID 1	CODE ID 2	MODE 1	$\overline{\text{MERR}}$	$\overline{\text{ERR}}$	SYO5	SYO3	SYO1	MD1	Vcc
14	SD6	SD4	SD1	PCBI7	PCBI4	PCBI1	PCBI0	MODE 0	SYO6	SYO4	SYO2	MD0	MD2	Vcc	MD5
13	SD9	SD5	BE0	SD3	SD0	PCBI2	GND	GND	SYO7	GND	SYO0	Vcc	MD3	MD6	MD9
12	SD11	SD7	Vcc										MD4	MD8	GND
11	SD12	SD10	SD8										MD7	MD10	MD11
10	SD15	BE1	GND										MD12	MD13	MD15
9	SLE	SD13	SD14										$\overline{\text{MOE}}$	MD14	MLE
8	$\overline{\text{SOE}}$	$\overline{\text{PLE}}$	GND					G144-2					GND	MD17	MD16
7	SD17	SD19	SD16										MD20	MD21	MD18
6	SD18	BE2	SD20										GND	MD23	MD19
5	SD21	SD22	SD25										MD27	MD25	MD22
4	GND	SD24	BE3	NC*									Vcc	MD28	MD24
3	SD23	SD26	SD28	Vcc	CB00	$\overline{\text{CBOE}}$	CB07	GND	GND	$\overline{\text{SCLK}}$ $\overline{\text{EN}}$	GND	CB16	CB17	MD30	MD26
2	SD27	Vcc	SD29	SD31	CB02	CB04	CB06	P3	MODE 2	SYN-CLK	CB10	CB13	CB14	MD31	MD29
1	Vcc	SD30	CB01	CB03	CB05	PSEL	$\overline{\text{PERR}}$	P2	P1	P0	$\overline{\text{CLEAR}}$	CB11	CB12	CB15	Vcc

*** = Tied to Vcc internally**

**PGA (CAVITY UP)
TOP VIEW**

DETAILED FUNCTIONAL BLOCK DIAGRAM



SYSTEM CONFIGURATIONS

The IDT49C465 EDC unit can be used in various configurations in an EDC system. The basic configurations are shown below.

Figure 1 illustrates a bidirectional configuration, which is most appropriate for systems using bidirectional memory buses. It is the simplest configuration to understand and use. During a correction cycle, the corrected data word can be simultaneously output on both the system bus and memory bus. During partial-word-write operations, the new bytes are internally combined with the corrected old bytes for checkbit generation and writing to memory.

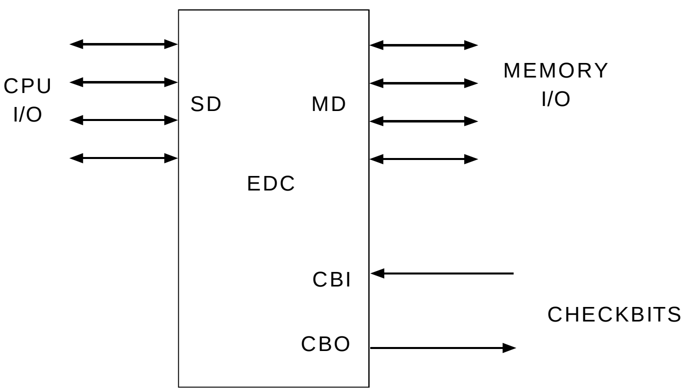


Figure 1. Common I/O Configuration

Figure 2 illustrates a separate I/O configuration. This is appropriate for systems using separate I/O memory buses. This configuration allows separate input and output memory buses to be used. Corrected data is output on the SD outputs for the system and for re-write to memory. Partial word-write bytes are combined externally for writing and checkbit generation.

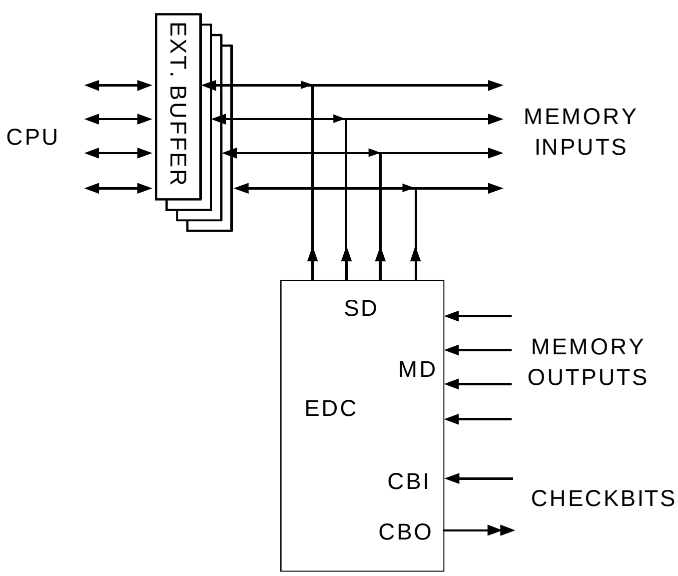


Figure 2. Separate I/O Configuration

Figure 3 illustrates a third configuration which uses external buffers and is also well-suited for systems using memory with separate I/O buses. Since data from memory does not need to pass through the part on every cycle, the EDC system may operate in “bus-watch” mode. As in the separate I/O configuration, corrected data is output on the SD outputs.

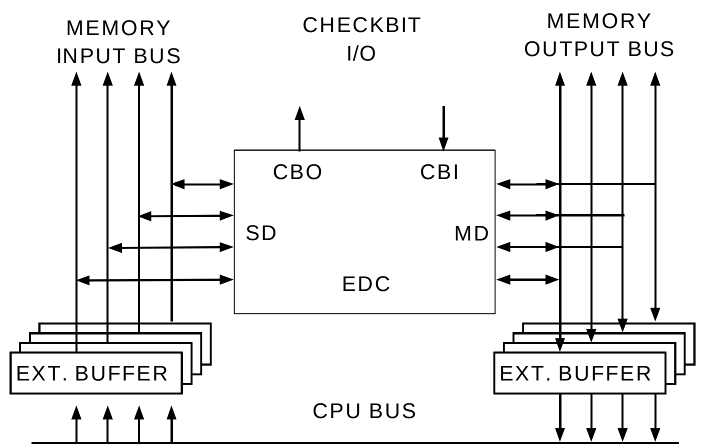


Figure 3. Bypassed Separate I/O Configuration

Figure 4 illustrates the single-chip generate-only mode for the very fast 64-bit checkbit generation in systems that use separate checkbit-generate and detect-correct units. If this is not desired, 64-checkbit generation and correction can be done with just two EDC units. 64-bit correction is also straightforward, fast, and requires no extra hardware for the expansion.

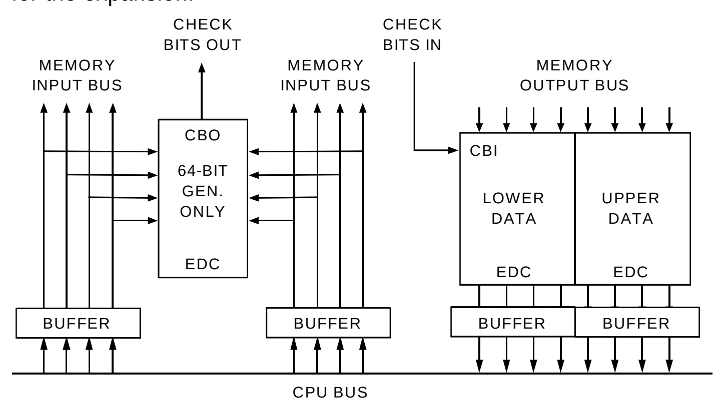


Figure 4. Separate generate/Correction Units with 64-Bit Checkbit Generation

FUNCTIONAL DESCRIPTION

The error detection/correction codes consist of a modified Hamming code; it is identical to that used in the IDT49C460.

32-BIT MODE (CODE ID 1,0 = 00)

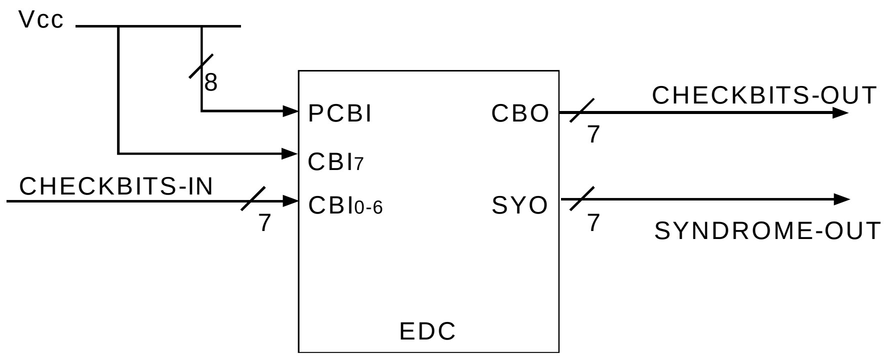


Figure 5. 32-Bit Mode

64-BIT MODE (CODE ID 1,0 = 10 & 11)

The expansion bus topology is shown in Figure 6. This topology allows the syndrome bits used by the correction logic to be generated simultaneously in both parts used in the expansion. During a 64-bit detection or correction operation, "Partial-Checkbit" data and "Partial-Syndrome" data is simultaneously exchanged between the two EDC units in opposite directions on dedicated expansion buses. This results in very short 64-bit detection and correction times.

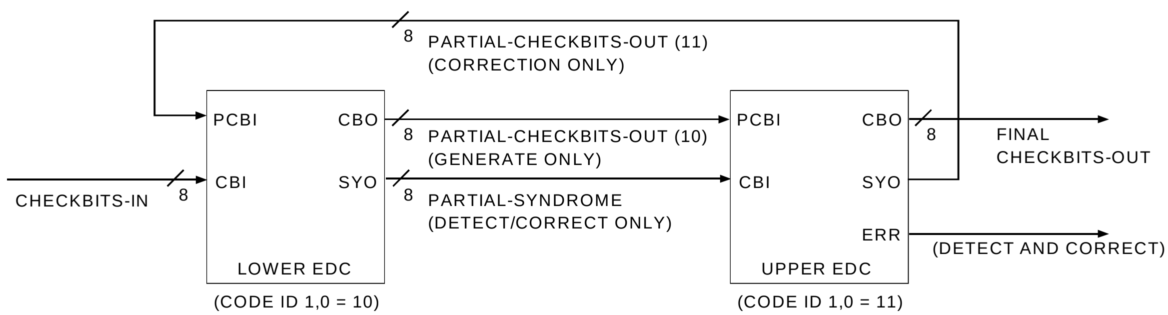


Figure 6. 64-Bit Mode — 2 Cascaded IDT49C465 Devices

64-BIT GENERATE-ONLY MODE (CODE ID 1,0 = 01)

If the identity pins CODE ID 1,0 = 01, a single EDC is placed in the 64-bit "Generate-only" mode. In this mode, the lower 32 bits of the 64-bit data word enter the device on the MD0-31 inputs and the upper 32-bits of the 64-bit data word enter the device on the SD0-31 inputs. This provides the device with the full 64-bit word from memory. The resultant generated checkbits are output on the CBO0-7 outputs. The generate time is less than that resulting from using a two-chip cascade.

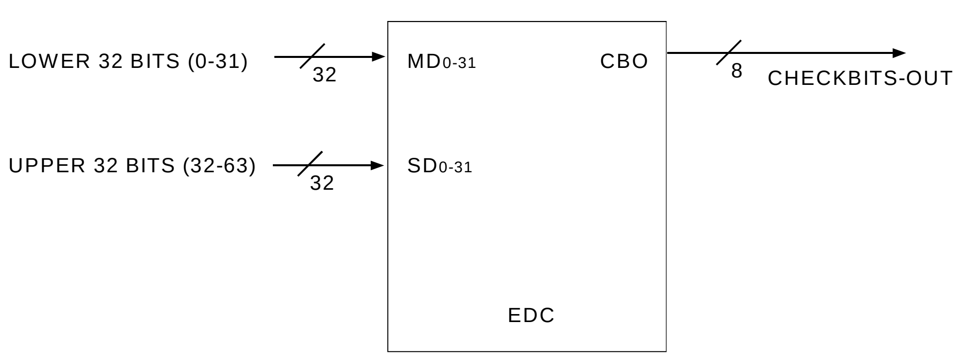


Figure 7. 64-Bit "Generate Only" Mode (Single Chip)

PIN DESCRIPTIONS

Symbol	I/O	Name and Function
I/O Buses and Controls		
SD$_{0-7}$ SD$_{8-15}$ SD$_{16-23}$ SD$_{24-31}$	I/O	**System Data Bus:** Data from the MD$_{0-31}$ appears at these pins corrected if MODE 2-0 = x11, or uncorrected in the other modes. The BEn inputs must be HIGH and the $\overline{SOE}$ pin must be LOW to enable the SD output buffers during a read cycle. (Also, see diagnostic section.) **Separate I/O Memory Systems:** In a write or partial-write cycle, the byte not-to-be-modified is output on SDn to n+7 for rewriting to memory, if BEn is HIGH and $\overline{SOE}$ is LOW. The new bytes to be written to memory are input on the SDn pins, for writing checkbits to memory, if BEn is LOW. **Separate I/O Memory Systems:** In a write or partial-write cycle, the byte not-to-be-modified is re-directed to the MS I/O pins, if BEn is HIGH, for checkbit generation and rewriting to memory by the MS I/O pins. $\overline{SOE}$ must be HIGH to avoid enabling the outputs drivers to the system bus in this more. The new bytes to be written are input on the SDn pins for checkbit generation and writing to memory. BEn must be LOW to direct input data from the System Data bus to the MD I/O pins for checkbit generation and writing to the checkbit memory.
SLE	I	**System Latch Enable:** SLE is an input used to latch data at the SD inputs. the latch is transparent when SLE is HIGH: the data is latched when SLE is LOW.
$\overline{PLE}$	I	**Pipeline Latch Enable:** $\overline{PLE}$ is an input which controls a pipeline latch, which controls data to be output on the SD bus and the MD bus during byte merges. Use of this latch is optional. The latch is transparent when $\overline{PLE}$ is LOW: the data is latched when $\overline{PLE}$ is HIGH.
$\overline{SOE}$	I	**System Output Enable:** When LOW, enables System output drivers and Parity outputs drivers if corresponding Byte Enable inputs are HIGH.
BE$_{0-3}$	I	**Byte Enables:** In systems using separate I/O memory buses, BEn is used to enable the SD and Parity outputs for byte n. The BEn pins also control the "Byte mux". When BEn is HIGH, the corrected or uncorrected data from the Memory Data latch is directed to the MD I/O pins and used for the checkbit generation for byte n. This is used in partial-word-write operations or during correction cycles. When BEn is LOW, the data from the System Data latch is directed to the MD I/O pins and used for the checkbit generation for byte n. BE$_0$ controls SD$_{0-7}$ BE$_0$ controls SD$_{16-23}$ BE$_1$ controls SD$_{8-15}$ BE$_1$ controls SD$_{24-31}$
MD$_{0-31}$	I/O	**Memory Data Bus:** These I/O pins accept a 32-bit data word from main memory for error detection and/or correction. They also output corrected old data or new data to be written to main memory when the EDC unit is used in a bidirectional configuration.
MLE	I	**Memory Latch Enable:** MLE is used to latch data from the MD inputs and checkbits from the CBI inputs. The latch is transparent when the MLE is HIGH: data is latched when MLE is LOW. When identified as the upper slice in a 64-bit cascade, the checkbit latch is bypassed.
$\overline{MOE}$	I	**Memory Output Enable:** $\overline{MOE}$ enables Memory Data Bus output drivers when LOW.
P$_{0-3}$	I/O	**Parity I/O:** The parity I/O pins for Bytes 0 to 3. These pins output the parity of their respective bytes when that byte is being output on the SD bus. These pins also serve as parity inputs and are used in generating the parity ERRor ($\overline{PERR}$) signal under certain conditions (see Byte Enable definition). The parity is odd or even depending on the state of the Parity SELect pin (PSEL).
PSEL	I	**Parity SELect:** If the Parity SELect pin is LOW, the parity is even. If the Parity SELect pin is HIGH, the parity is odd.
Inputs		
CBI$_{0-7}$	I	**CheckBits-In** (00) CheckBits-In-1 (10) Partial-Syndrome-In (11) In a single EDC system or in the lower slice of a cascaded EDC system, these inputs accept the checkbits from the checkbit memory. In the upper slice in a cascaded EDC system, these inputs accept the "Partial-Syndrome" from the lower slice (Detect/Correct path).
PCBI$_{0-7}$	I	**Partial-CheckBits-In** (10) Partial-CheckBits-In (11) In a single EDC system, these inputs are unused but should not be allowed to float. In a cascaded EDC system, the "Partial-checkbits" used by the lower slice are accepted by these inputs (Correction path only). In the upper slice of a cascaded EDC system, "Partial Checkbits" generated by the lower slice are accepted by these inputs (Generate path).
CODE ID $_{1,0}$	I	**CODE IDentity:** Inputs with identify the slice position/ functional mode of the IDT49C465. (00) Single 32-bit EDC unit (10) Lower slice of a 64-bit cascade (01) 64-bit "Checkbit-generate-only" unit (11) Upper slice of a 64-bit cascade

PIN DESCRIPTIONS (continued)

Symbol	I/O		Name and Function
Inputs (continued)			
$MODE_{2-0}$	I		**MODE Select:** Selects one of the five operating modes.
		(x11)	**"Normal" Mode:** Normal EDC operation (Flow-thru correction and generation).
		(x10)	**"Generate-Detect" Mode:** In this mode, error correction is disabled. Error generation and detection are normal.
		(000)	**"Error-Data-Output" Mode:** Allows the uncorrected data from an error event by the Error-Data register to be read by the system for diagnostic purposes. The Error-Data Register is cleared by toggling $\overline{CLEAR}$ LOW. The Syndrome Register and Error Data Register record the syndrome and uncorrected data from the first error that occurs after they are reset by the $\overline{CLEAR}$ pin. The Syndrome Register and Error-Data Register are updated when there is a positive edge on SYNCLK, an error condition is indicated ($\overline{ERR}$ = LOW), and the Error Counter indicates zero. **All-Zero-Data Source:** In Error-Data-Output Mode, clearing the Error-Data Register provides a source of all-zero-data for hardware initialization of memory, if this is desired.
		(x01)	**Diagnostic-output Mode:** In this mode, the contents of the Syndrome Register, Error Counter and Error-Type Register are output on the SD bus. This allows the syndrome bytes for an indicated error to be read by the system for error-logging purposes. The Syndrome Register and the Error-Data Register are updated when there is a positive edge an SYNCLK, and error condition is indicated, and the Error Counter indicates zero errors. Thus, the Syndrome Register saves the syndrome that was present when the first error occurred after the Error Counter was cleared. The Syndrome Register and the Error Counter are cleared by toggling $\overline{CLEAR}$ LOW. The Error Counter lets the system tell if more than one error has occurred since the last time the Syndrome Register or Error Data Register was read.
		(100)	**Checkbit-Injection Mode:** In "Checkbit-Injection" Mode, diagnostic checkbits may be input on the System Data Bus bits 0-7 (see Diagnostic Features - Detailed Description).
$\overline{CLEAR}$	I		**CLEAR:** When the $\overline{CLEAR}$ pin is taken LOW, the Error-Data Register, the Syndrome Register, the Error Counter, and the Error-Type Register are cleared.
SYNCLK	I		**SYNdrome CLocK:** If $\overline{ERR}$ is LOW, and the Error Counter indicates zero errors, syndrome bits are clocked into the Syndrome Register and data from the outputs of the Memory Data input latch are clocked into the Error-Data Register on the LOW-to-HIGH edge of SYNCLK. If $\overline{ERR}$ is LOW, the Error Counter will increment on the LOW-to-HIGH edge of SYNCLK, unless the Error Counter indicated fifteen errors.
$\overline{SCLKEN}$	I		**SynCLK ENable:** The $\overline{SCLKEN}$ enables the SYNCLK signal. SYNCLK is ignored if $\overline{SCLKEN}$ is HIGH.
Outputs and Enables			
CBO_{0-7}	O		**CheckBits-Out** (00, 01) Partial CheckBits-Out (10): CheckBits-Out (11): In a single EDC system, the checkbits are output to the checkbit memory on the outputs. In the lower slice in a cascaded EDC system, the "Partial-checkbits" used by the upper slice are generated by the lower slice CBO_{0-7} bits (Generate path only). In the upper slice of a cascade, the "Final-Checkbits" appear at these outputs (Generate path only).
$\overline{CBOE}$	I		**CheckBits Out Enable:** Enables CheckBit Output driver when LOW.
SYO_{0-7}	O		**SYndrome-Out** (00) Partial SYndrome-Out(10): Partial CheckBits-Out (11): In a 32-bit EDC system, the syndrome bits are output on these pins. In the lower slice in a 64-bit cascaded system, the "Partial-Syndrome" bits appear at these outputs (Detect/Correct path). In the upper slice in a cascaded EDC system, the "Partial-Checkbits" appear at these outputs (Correct path only). In a 64-bit cascaded system, the "Final-Syndrome" may be accessed in the "Diagnostic-Output" Mode from either the lower or the upper slice since the final syndrome is contained in both.
$\overline{ERR}$	O		**ERROR:** When in "Normal" and "Detect only" modes, a LOW on this pin indicates that one or more errors have been detected. $\overline{ERR}$ is not gated or latched internally.
$\overline{MERR}$	O		**Multiple ERRor:** When in "Normal" and "Detect only" modes, a LOW on this pin indicates that one or more errors have been detected. M$\overline{ERR}$ is not gated or latched internally.
$\overline{PERR}$	O		**Parity ERRor:** A LOW on this pin indicates a parity error which has resulted from the active bytes defined by the 4 Byte Enable pins. Parity ERRor ($\overline{PERR}$) is not gated or latched internally (see Byte Enable definition).
Power Supply Pins			
V_{CC} 1-10	P		+5 Volts
GND 1-12	P		Ground

DIAGNOSTIC DATA FORMAT (SYSTEM BUS)

Latched Data																Data Out (Unlatched)															
Error Type		Reserved		Error Counter				Syndrome Bits								Partial Checkbits								Checkbits							
Byte 3								Byte 2								Byte 1								Byte 0							
S	M	-	-	2^3	2^2	2^1	2^0	7	6	5	4	3	2	1	0	7	6	5	4	3	2	1	0	7	6	5	4	3	2	1	0
31	30			27			24	23							16	15							8	7							0

DIAGNOSTIC FEATURES — DETAILED DESCRIPTION

Mode 2-0	
x11	**"NORMAL" Mode** In this mode, operation is "Normal" or non-diagnostic.
x10	**"GENERATE-DETECT" Mode** When the EDC unit is in the **"Generate-Detect" Mode**, data is not corrected or altered by the error correction network. (Also referred to as the "Detect-only" mode.)
000	**"ERROR-DATA-OUTPUT" Mode** In this mode, the 32-bit data from the Error-Data Register is output on the SD bus. **Error Data Register**: The uncorrected data from the Memory Data bus input latch is stored in the Error-Data Register if the error counter contents indicates "0" and there is a positive transition on the SYNCLK input when the $\overline{\text{ERR}}$ signal is LOW. Thus, the Error-Data Register contains memory data corresponding to the first error to occur since the register was cleared. This register is cleared by pulling the CLEAR input LOW. The register is read by the System Data bus by entering the **"Error-Data-Output" Mode** and enabling the System Data bus output drivers. **All-Zero-Data**: The Error-Data Register can be used as an "all-zero-data" source for memory initialization in systems where the initialization process is to be done entirely by hardware.
x01	**"DIAGNOSTIC-OUTPUT" Mode** In this mode, data from the diagnostic registers, the PCBI bus, and the CBI bus is output on the SD bus. **Direct Checkbit Readback**: Internal data paths allow both the "Partial-Checkbit-Input" bus and the data in the "Checkbit-Input" latch to be read directly by the system bus for diagnostic purposes. Both the Checkbit Input Bus and the Partial Checkbit Input Bus are read via the System bus by entering the **"Diagnostic-Output" Mode** and enabling the System Data bus output drivers. The checkbits are output on the System Data bus bits 0-7; the Partial Checkbits are output on bits 8-15. **Syndrome Register**: After an error has been detected, the syndrome bits generated are clocked into the internal Syndrome Register if the error counter contents indicates "0" and there is a positive transition on the SYNCLK input when the $\overline{\text{ERR}}$ signal is LOW. This register is cleared by pulling the $\overline{\text{CLEAR}}$ input LOW. The register is read by the System Data bus by entering the **"Diagnostic-Output" Mode** and enabling the System Data bus output drivers. This data is output on SD bits 16-23. **Error Counter**: The 4-bit on-board error counter is incremented if the error counter contents do not indicate FF HEX, which corresponds to a count of 15, and there is a positive transition on the SYNCLK input where the $\overline{\text{ERR}}$ signal is LOW. This counter is cleared by pulling the $\overline{\text{CLEAR}}$ input LOW. The counter is read by the System Data bus by entering the **"Diagnostic-Output" Mode** and enabling the System Data bus output drivers. The data is output on SD bits 24-27. **Test Register**: These two bits are reserved for factory diagnostics only and must not be used by system software. This data is output on System Data bus bits 28-29. **Error-Type Register**: The Error-Type Register, clocked by the SYNCLK input, saves two bits which indicate whether a recorded error was a single or a multiple-bit error. This register holds only the first error type to occurs after the last Clear operation. This data is output on System Data bus bits 30-31.
100	**Direct Read-Path Checkbit Injection**: In the **"Checkbit-Injection" Mode**, bits 0-7 of the System Data input latch are presented to the inputs of the Checkbit Input Latch. If MLE is strobed, the checkbit latch will be loaded with this value in place of the checkbits from memory. By inserting various checkbit values, operation of the correction function of the EDC can be verified "on-board". Except for the "Checkbit-Injection" function, operation in this mode is identical to "Normal" Mode operation.

OPERATING MODE CHARTS

SLICE IDENTIFICATION

CODE ID 1	CODE 1D 0	Slice Definition
0	0	32-bit Flow-Thru EDC
0	1	64-bit GENERATE Only EDC
1	0	64-bit EDC- Lower 32 bits (0-31)
1	1	64-bit EDC- Upper 32 bits (32-63)

SLICE POSITION CONTROL

CODE ID	Slice Position/ Functional Operation	$\overline{\text{SOE}}$	SD Bus	$\overline{\text{MOE}}$	MD Bus	Checkbit Buses: PCBI Bus	Checkbit Buses: CBI Bus	Checkbit Buses: CBO Bus	Checkbit Buses: SYO Bus	P Bus	$\overline{\text{PERR}}$
1 0	Width =		32		32	8	8	8	8	4	1
0 0	Single 32-bit EDC unit										
	Generate(1)	1	Sys. 0-31	0	Sys. Byte Mux	—	—	CBs out	—	P in	active
	Detect/Correct(2)	0	Pipe. latch	1	MD 0-31	—	CBs in	—	Syn. out	P out	—
0 1	"64-bit Generate Only"	1	Sys. 32-63	1	Sys. 0-31	—	—	CBs out	—	—	—
1 0	Lower word, 64-bit bus										
	Generate(1)	1	Sys. 0-31	0	MD 0-31	—	—	PCBs out	—	P in	active
	Detect/Correct(2)	0	Pipe. latch	1	MD 0-31	U-SYOout	CBs in	—	Par.Synd	P out	—
1 1	Upper word, 64-bit bus										
	Generate(1)	1	Sys. 32-63	0	MD 32-63	—	—	F.CBs out	—	P in	active
	Detect/Correct(2)	0	Pipe. latch	1	MD 32-63	L-CBOout	L-SYOout	—	Par.Cbits	P out	—

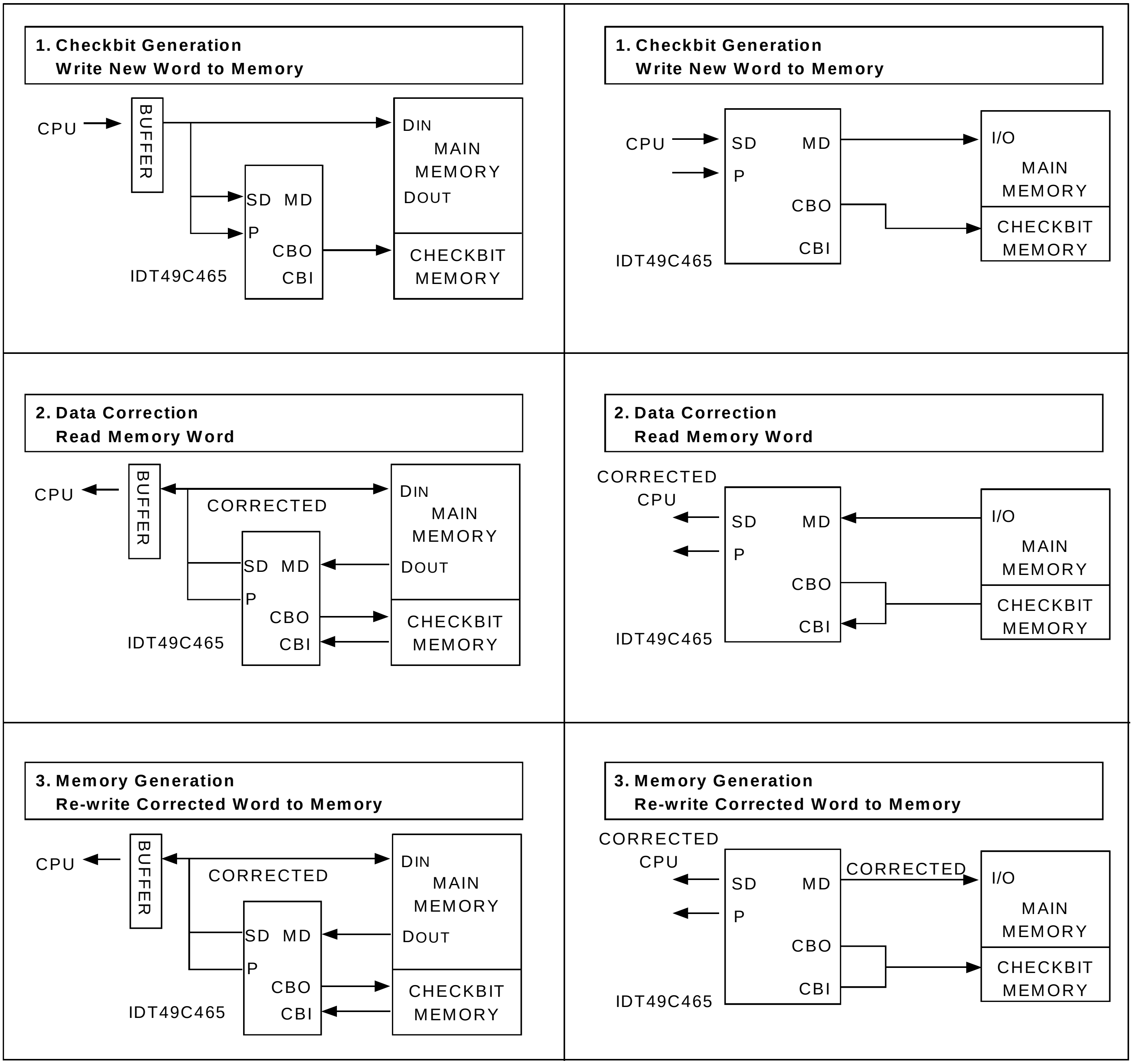
NOTES:
1. Checkbits generated from the data in the SD Latch.
2. Corrected data residing in the Pipe Latch.

FUNCTIONAL MODE CONTROL

MODE 2	MODE 1	MODE 0	Functional Mode of SD Bus	$\overline{\text{SOE}}$	SD Bus	$\overline{\text{MOE}}$	MD Bus	Checkbit Buses: PCBI Bus	Checkbit Buses: CBI Bus	Checkbit Buses: CBO Bus	Checkbit Buses: SYO Bus	P Bus	$\overline{\text{PERR}}$
2	1	0	Width =		32		32	8	8	8	8	4	1
x	1	1	**"Normal"**										
			Generate	1	CPU Data	0	Pipe. Latch	—	—	CB out	—	P in	active
			Correct	0	Pipe. latch	1	RAM Data	—	CB in	—	—	P out	—
x	0	1	**"Generate-Detect"**										
			Generate	1	CPU Data	0	Pipe. Latch	—	—	CB out	—	P in	active
			Correct	0	Pipe. latch	1	RAM Data	—	CB in	—	—	P out	—
0	0	0	**"Error-Data-Output"**	0	Err. D. latch	—	—	—	—	—	—	—	—
x	0	1	**"Diagnostic-Output"**	0	CBin latch PCBIin bus Syn. register Err counter Er. type reg.	—	—	PCBI in	CB in	—	—	—	—
1	0	0	**"Checkbit-Injection"**										
			Generate	1	Sys. 32-63	0	Pipe. Latch	—	—	CB out	—	P in	active
			Inject Checkbits	1	Pipe. latch	0	Pipe. Latch	—	—	—	—	—	—
			Correct	0		1	RAM Data	—	CB in	—	—	P out	—

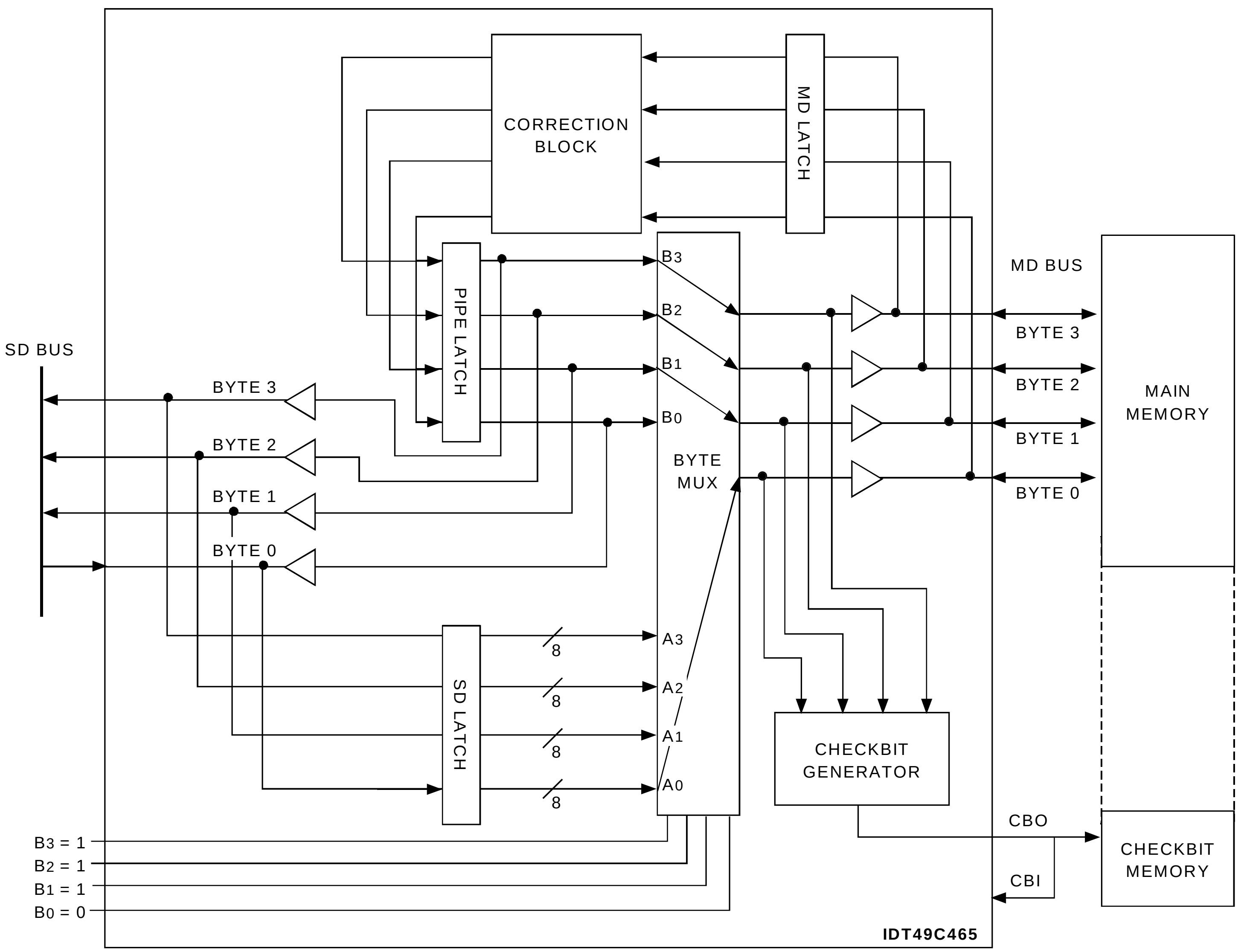
PRIMARY DATA PATH vs. MEMORY CONFIGURATION

SEPARATE I/O MEMORIES | **COMMON I/O MEMORIES**



PARTIAL-WORD-WRITE OPERATIONS

FOR COMMON I/O MEMORIES



In order to perform a partial-word-write operation, the complete word in question must be read from memory. This must be done in order to correct any error which may have occurred in the old word. Once the complete, corrected word is available, with all bytes verified, the new word may be assembled in the byte mux and the new checkbits generated.

The example shown above illustrates the case of combining three bytes from an old word with a new lower order byte to form a new word. The new word, along with the new checkbits, may now be written to memory.

In the separate I/O memory configuration, the situation is similar except that the new word is output on the SD Bus instead of the MD Bus (refer to previous page.)

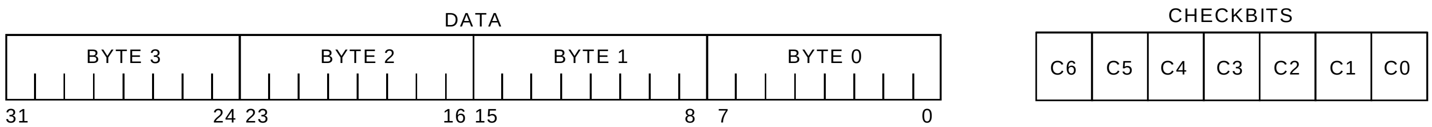
32-BIT DATA WORD CONFIGURATION

A single IDT49C465 EDC unit, connected as shown below, provides all the logic needed for single-bit error correction, and double-bit error detection, of a 32-bit data field. The identification code (00) indicates seven checkbits are required. the CBI_7 pin should be tied high.

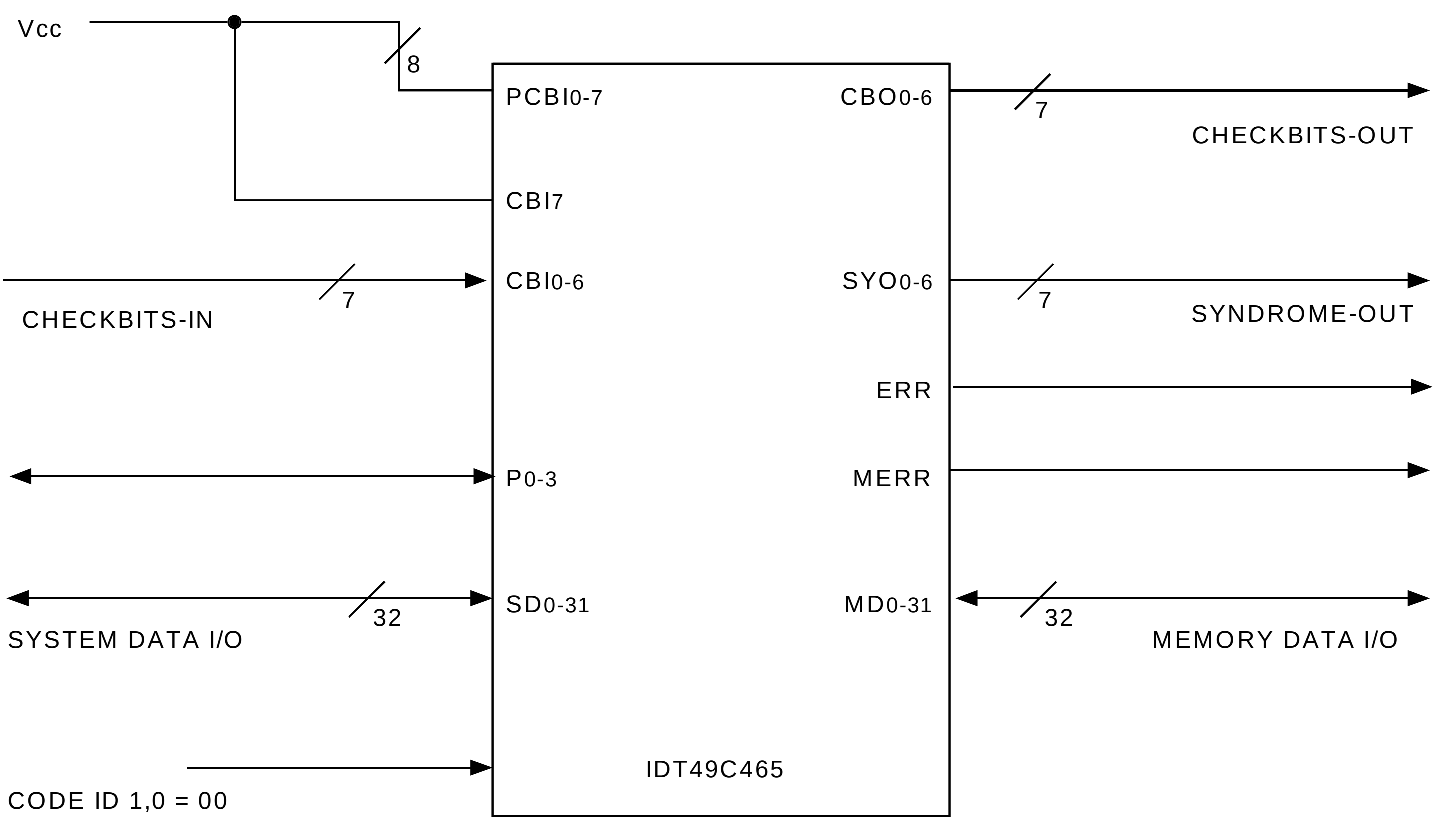
The 39-bit data format for bytes of data and seven checkbits is indicated below.

Syndrome bits are generated by an exclusive-OR of the generated checkbits with the checkbits read from memory. For example, Sn is the XOR of checkbits from those read with those generated. During Data Correction, the syndrome bits are used to complement (correct) single-bit errors in the data bits.

32-BIT DATA FORMAT



32-BIT HARDWARE CONFIGURATION



64-BIT DATA WORD CONFIGURATION

Two IDT49C465 EDC units, connected as shown below, provide all the logic needed for single-bit error correction, and double-bit error detection, of a 64-bit data field. The "Slice Identification" table gives the CODE ID 1, 0 values needed for distinguishing the upper 32 bits from the lower 32 bits. Final generated Checkbits, $\overline{\text{ERR}}$ and $\overline{\text{MERR}}$ (indicates multiple errors) signals come from the upper slice, the IC with CODE ID 1, 0 = 11. Control signals not shown are connected to both units in parallel.

Data-In bits 0 through 31 are connected to the same numbered inputs of the EDC with CODE ID 1, 0 = 10 while Data-In bits 32 through 63 are connected to data inputs 0 to 31, respectively, for the EDC unit with CODE ID 1, 0 = 11.

The 72-bit data format of data and checkbits is indicated below.

Correction of single-bit errors in the 64-bit configuration requires a simultaneous exchange of partial checkbits and partial syndrome bits between the upper and lower units.

Syndrome bits are generated by an exclusive-OR of the generated checkbits with the checkbits read from memory. For example, Sn is the XOR of checkbits from those read with those generated. During Data Correction, the syndrome bits are used to complement (correct) single-bit errors in the data bits. For double or multiple-bit error detection, the data available as output by the Pipeline Latch is not defined.

Critical AC performance data is provided in the table "Key AC Calculations", which illustrates the delays that are critical to 64-bit cascaded performance. As indicated, a summation of propagation delays is required when cascading these units.

64-BIT DATA FORMAT

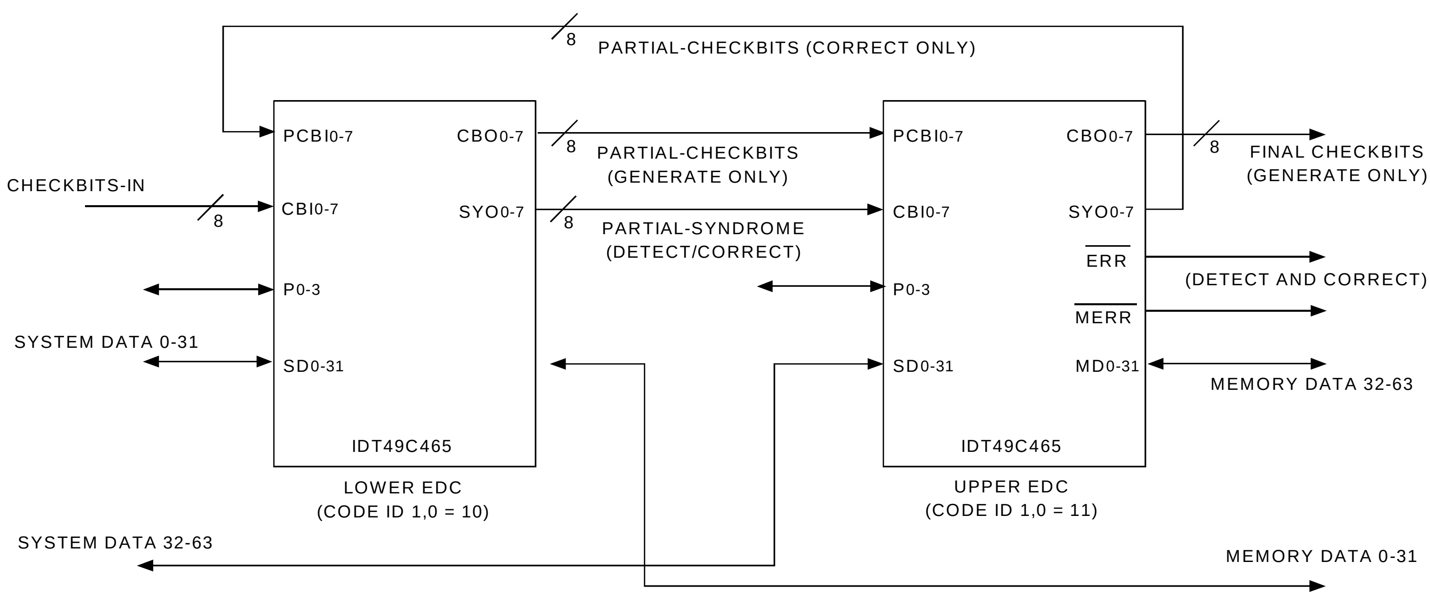
DATA

BYTE 7	BYTE 7	BYTE 5	BYTE 4	BYTE 3	BYTE 2	BYTE 1	BYTE 0
63 56	55 48	47 40	39 32	31 24	23 16	15 8	7 0

CHECKBITS

C7	C6	C5	C4	C3	C2	C1	C0

64-BIT HARDWARE CONFIGURATION



DEFINITIONS OF TERMS

D_0 - D_{31}	= System Data and/or Memory Data Inputs
CBI_0 - CBI_7	= Checkbit Inputs
$PCBI_0$ - $PCBI_7$	= Partial Checkbit Inputs
FS_0 - FS_7	= Final Internal Syndrome Bits

FUNCTIONAL EQUATIONS

The equations below describe the terms used in the IDT49C465 to determine the values of the partial checkbits, checkbits, partial syndromes, and final internal syndromes.

NOTE: All "⊕" symbols below represent the "EXCLUSIVE-OR" function

$PA = D_0 \oplus D_1 \oplus D_2 \oplus D_4 \oplus D_6 \oplus D_8 \oplus D_{10} \oplus D_{12} \oplus D_{16} \oplus D_{17} \oplus D_{18} \oplus D_{20} \oplus D_{22} \oplus D_{24} \oplus D_{26} \oplus D_{28}$

$PB = D_0 \oplus D_3 \oplus D_4 \oplus D_7 \oplus D_9 \oplus D_{10} \oplus D_{13} \oplus D_{15} \oplus D_{16} \oplus D_{19} \oplus D_{20} \oplus D_{23} \oplus D_{25} \oplus D_{26} \oplus D_{29} \oplus D_{31}$

$PB = D_0 \oplus D_1 \oplus D_5 \oplus D_6 \oplus D_7 \oplus D_{11} \oplus D_{12} \oplus D_{13} \oplus D_{16} \oplus D_{17} \oplus D_{21} \oplus D_{22} \oplus D_{23} \oplus D_{27} \oplus D_{28} \oplus D_{29}$

$PD = D_2 \oplus D_3 \oplus D_4 \oplus D_5 \oplus D_6 \oplus D_7 \oplus D_{14} \oplus D_{15} \oplus D_{18} \oplus D_{19} \oplus D_{20} \oplus D_{21} \oplus D_{22} \oplus D_{23} \oplus D_{30} \oplus D_{31}$

$PE = D_8 \oplus D_9 \oplus D_{10} \oplus D_{11} \oplus D_{12} \oplus D_{13} \oplus D_{14} \oplus D_{15} \oplus D_{24} \oplus D_{25} \oplus D_{26} \oplus D_{27} \oplus D_{28} \oplus D_{29} \oplus D_{30} \oplus D_{31}$

$PF = D_0 \oplus D_1 \oplus D_2 \oplus D_3 \oplus D_4 \oplus D_5 \oplus D_6 \oplus D_7 \oplus D_{24} \oplus D_{25} \oplus D_{26} \oplus D_{27} \oplus D_{28} \oplus D_{29} \oplus D_{30} \oplus D_{31}$

$PG = D_8 \oplus D_9 \oplus D_{10} \oplus D_{11} \oplus D_{12} \oplus D_{13} \oplus D_{14} \oplus D_{15} \oplus D_{16} \oplus D_{17} \oplus D_{18} \oplus D_{19} \oplus D_{20} \oplus D_{21} \oplus D_{22} \oplus D_{23}$

$PH_0 = D_0 \oplus D_4 \oplus D_6 \oplus D_7 \oplus D_8 \oplus D_9 \oplus D_{11} \oplus D_{14} \oplus D_{17} \oplus D_{18} \oplus D_{19} \oplus D_{21} \oplus D_{26} \oplus D_{28} \oplus D_{29} \oplus D_{31}$

$PH_1 = D_1 \oplus D_2 \oplus D_3 \oplus D_5 \oplus D_8 \oplus D_9 \oplus D_{11} \oplus D_{14} \oplus D_{17} \oplus D_{18} \oplus D_{19} \oplus D_{21} \oplus D_{24} \oplus D_{25} \oplus D_{27} \oplus D_{30}$

$PH_2 = D_0 \oplus D_4 \oplus D_6 \oplus D_7 \oplus D_{10} \oplus D_{12} \oplus D_{13} \oplus D_{15} \oplus D_{16} \oplus D_{20} \oplus D_{22} \oplus D_{23} \oplus D_{26} \oplus D_{28} \oplus D_{29} \oplus D_{31}$

CMOS TESTING CONSIDERATIONS

Special test board considerations must be taken into account when applying high-speed CMOS products to the automatic test environment. Large output currents are being switched in very short periods and proper testing demands that test set-ups have minimized inductance and guaranteed zero voltage grounds. The techniques listed below will assist the user in obtaining accurate testing results.

1. All input pins should be connected to a voltage potential during testing. If left floating, the device may oscillate, causing improper device operation and possible latchup.

2. Placement and value of decoupling capacitors is critical. Each physical set-up has different electrical characteristics and it is recommended that various decoupling capacitor sizes be experimented with. Capacitors should be positioned using the minimum lead lengths. They should also be distributed to decouple power supply lines and be placed as close as possible to the DUT power pins.

3. Device grounding is extremely critical for proper device testing. The use of multi-layer performance boards with radial decoupling between power and ground planes is necessary. The ground plane must be sustained from the performance board to the DUT interface board. Wiring unused interconnect pins to the ground plane is recommended. Heavy gauge stranded wire should be used for power wiring, with twisted pairs being recommended for minimized inductance.

4. To guarantee data sheet compliance, the input thresholds should be tested per input pin in a static environment. To allow for testing and hardware-induced noise, IDT recommends using the $V_{IL} \leq 0V$ and $V_{IH} \geq 3V$ for AC tests.

DETAILED DESCRIPTION — CHECKBIT AND SYNDROME GENERATION vs. CODE ID

LOGIC EQUATIONS FOR THE CBO OUTPUTS

Checkbit Generation	CODE ID 1,0		
	00	10	11
	Final Checkbits	Partial Checkbits	Final Checkbits
CBO_0	PH_0	PH_1	$PH_2 \oplus PCBI_0$
CBO_1	PA	PA	$PA \oplus PCBI_1$
CBO_2	$\overline{PB}$	$\overline{PB}$	$PB \oplus PCBI_2$
CBO_3	$\overline{PC}$	$\overline{PC}$	$PC \oplus PCBI_3$
CBO_4	PD	PD	$PD \oplus PCBI_4$
CBO_5	PE	PE	$PE \oplus PCBI_5$
CBO_6	PF	PF	$PF \oplus PCBI_6$
CBO_7	—	PF	$PG \oplus PCBI_7$

LOGIC EQUATIONS FOR THE SYO OUTPUTS

Checkbit Generation	CODE ID 1,0		
	00	10	11
	Final Syndrome	Partial Syndrome	Partial Checkbits
SYO_0	$PH_0 \oplus CBI_0$	$PH_1 \oplus CBI_0$	PH_2
SYO_1	$PA \oplus CBI_1$	$PA \oplus CBI_1$	PA
SYO_2	$\overline{PB} \oplus CBI_2$	$\overline{PB} \oplus CBI_2$	PB
SYO_3	$\overline{PC} \oplus CBI_3$	$\overline{PC} \oplus CBI_3$	PC
SYO_4	$PD \oplus CBI_4$	$PD \oplus CBI_4$	PD
SYO_5	$PE \oplus CBI_5$	$PE \oplus CBI_5$	PE
SYO_6	$PF \oplus CBI_6$	$PF \oplus CBI_6$	PF
SYO_7	—	$PF \oplus CBI_7$	PG

LOGIC EQUATIONS FOR THE FINAL SYNDROME (FSn)

Checkbit Generation	CODE ID 1,0	
	00	10, 11
	Final Syndrome	Final Internal Syndrome
FS_0	$PH_0 \oplus CBI_0$	$PH_1 (L) \oplus PH_2 (U) \oplus CBI_0$
FS_1	$PA \oplus CBI_1$	$PA (L) \oplus PA (U) \oplus CBI_1$
FS_2	$\overline{PB} \oplus CBI_2$	$\overline{PB} (L) \oplus PB (U) \oplus CBI_2$
FS_3	$\overline{PC} \oplus CBI_3$	$\overline{PC} (L) \oplus PC (U) \oplus CBI_3$
FS_4	$PD \oplus CBI_4$	$PD (L) \oplus PD (U) \oplus CBI_4$
FS_5	$PE \oplus CBI_5$	$PE (L) \oplus PE (U) \oplus CBI_5$
FS_6	$PF \oplus CBI_6$	$PF (L) \oplus PF (U) \oplus CBI_6$
FS_7	—	$PF (L) \oplus PG (U) \oplus CBI_7$

32-BIT SYNDROME DECODE TO BIT-IN-ERROR [(1)]

						HEX	0	1	2	3	4	5	6	7
		SYNDROME BITS				S6	0	0	0	0	1	1	1	1
						S5	0	0	1	1	0	0	1	1
						S4	0	1	0	1	0	1	0	1
HEX	S3	S2	S1	S0										
0	0	0	0	0			*	C4	C5	T	C6	T	T	30
1	0	0	0	1			C0	T	T	14	T	M	M	T
2	0	0	1	0			C1	T	T	M	T	2	24	T
3	0	0	1	1			T	18	8	T	M	T	T	M
4	0	1	0	0			C2	T	T	15	T	3	25	T
5	0	1	0	1			T	19	9	T	M	T	T	31
6	0	1	1	0			T	20	10	T	M	T	T	M
7	0	1	1	1			M	T	T	M	T	4	26	T
8	1	0	0	0			C3	T	T	M	T	5	27	T
9	1	0	0	1			T	21	11	T	M	T	T	M
A	1	0	1	0			T	22	12	T	1	T	T	M
B	1	0	1	1			17	T	T	M	T	6	28	T
C	1	1	0	0			T	23	13	T	M	T	T	M
D	1	1	0	1			M	T	T	M	T	7	29	T
E	1	1	1	0			16	T	T	M	T	M	M	T
F	1	1	1	1			T	M	M	T	0	T	T	M

NOTE:

1. The table indicates the decoding of the seven syndrome bits to identify the bit-in-error for a single-bit error, or whether a double or triple-bit error was detected. The all-zero case indicattes no error detected.
   * = No errors detected
   # = The number of the single bit-in-error
   T = Two errors detected
   M = three or more errors detected

DETAILED DESCRIPTION — 32-BIT CONFIGURATION

32-BIT MODIFIED HAMMING CODE - CHECKBIT ENCODING CHART [1]

Generated Checkbits	Parity	Participating Data Bits															
		0	1	2	3	4	5	6	7	8	9	10	11	12	13	14	15
CB0	Even (XOR)	X				X		X	X	X	X		X			X	
CB1	Even (XOR)	X	X	X		X		X		X		X		X			
CB2	Odd (XNOR)	X			X	X			X		X	X			X		X
CB3	Odd (XNOR)	X	X				X	X	X				X	X	X		
CB4	Even (XOR)			X	X	X	X	X	X							X	X
CB5	Even (XOR)									X	X	X	X	X	X	X	X
CB6	Even (XOR)	X	X	X	X	X	X	X	X								

Generated Checkbits	Parity	Participating Data Bits															
		16	17	18	19	20	21	22	23	24	25	26	27	28	29	30	31
CB0	Even (XOR)		X	X	X		X					X		X	X		X
CB1	Even (XOR)	X	X	X		X		X		X		X		X			
CB2	Odd (XNOR)	X			X	X			X		X	X			X		X
CB3	Odd (XNOR)	X	X				X	X	X				X	X	X		
CB4	Even (XOR)			X	X	X	X	X	X							X	X
CB5	Even (XOR)									X	X	X	X	X	X	X	X
CB6	Even (XOR)									X	X	X	X	X	X	X	X

NOTE:
1. The table indicates the data bits participating in the checkbit generation. For example, checkbit C0 is the Exclusive-OR function of the 16 data input bits marked with an X.

DETAILED DESCRIPTION — 64-BIT CONFIGURATION

64-BIT MODIFIED HAMMING CODE - CHECKBIT ENCODING CHART [1, 2]

Generated		Participating Data Bits															
Checkbits	**Parity**	**0**	**1**	**2**	**3**	**4**	**5**	**6**	**7**	**8**	**9**	**10**	**11**	**12**	**13**	**14**	**15**
CB0	Even (XOR)		X	X	X		X			X	X		X			X	
CB1	Even (XOR)	X	X	X		X		X		X		X		X			
CB2	Odd (XNOR)	X			X	X			X		X	X			X		X
CB3	Odd (XNOR)	X	X				X	X	X				X	X	X		
CB4	Even (XOR)			X	X	X	X	X	X							X	X
CB5	Even (XOR)									X	X	X	X	X	X	X	X
CB6	Even (XOR)	X	X	X	X	X	X	X	X								
CB7	Even (XOR)	X	X	X	X	X	X	X	X								

Generated		Participating Data Bits															
Checkbits	**Parity**	**16**	**17**	**18**	**19**	**20**	**21**	**22**	**23**	**24**	**25**	**26**	**27**	**28**	**29**	**30**	**31**
CB0	Even (XOR)		X	X	X		X			X	X		X			X	
CB1	Even (XOR)	X	X	X		X		X		X		X		X			
CB2	Odd (XNOR)	X			X	X			X		X	X			X		X
CB3	Odd (XNOR)	X	X				X	X	X				X	X	X		
CB4	Even (XOR)			X	X	X	X	X	X							X	X
CB5	Even (XOR)									X	X	X	X	X	X	X	X
CB6	Even (XOR)									X	X	X	X	X	X	X	X
CB7	Even (XOR)									X	X	X	X	X	X	X	X

Generated		Participating Data Bits															
Checkbits	**Parity**	**32**	**33**	**34**	**35**	**36**	**37**	**38**	**39**	**40**	**41**	**42**	**43**	**44**	**45**	**46**	**47**
CB0	Even (XOR)	X				X		X	X			X		X	X		X
CB1	Even (XOR)	X	X	X		X		X		X		X		X			
CB2	Odd (XNOR)	X			X	X			X		X	X			X		X
CB3	Odd (XNOR)	X	X				X	X	X				X	X	X		
CB4	Even (XOR)			X	X	X	X	X	X							X	X
CB5	Even (XOR)									X	X	X	X	X	X	X	X
CB6	Even (XOR)	X	X	X	X	X	X	X	X								
CB7	Even (XOR)									X	X	X	X	X	X	X	X

Generated		Participating Data Bits															
Checkbits	**Parity**	**48**	**49**	**50**	**51**	**52**	**53**	**54**	**55**	**56**	**57**	**58**	**59**	**60**	**61**	**62**	**63**
CB0	Even (XOR)	X				X		X	X			X		X	X		X
CB1	Even (XOR)	X	X	X		X		X		X		X		X			
CB2	Odd (XNOR)	X			X	X			X		X	X			X		X
CB3	Odd (XNOR)	X	X				X	X	X				X	X	X		
CB4	Even (XOR)			X	X	X	X	X	X							X	X
CB5	Even (XOR)									X	X	X	X	X	X	X	X
CB6	Even (XOR)									X	X	X	X	X	X	X	X
CB7	Even (XOR)	X	X	X	X	X	X	X	X								

NOTES:
1. The table indicates the data bits participating in the checkbit generation. For example, checkbit C0 is the Exclusive-OR function of the 64 data input bits marked with an X.
2. The checkbit is generated as either an XOR or an XNOR of the 64 data bits noted by an “X” in the table.

DETAILED DESCRIPTION — 64-BIT CONFIGURATION (cont.)

64-BIT SYNDROME DECODE TO BIT-IN-ERROR (1)

					HEX	0	1	2	3	4	5	6	7	8	9	A	B	C	D	E	F
	Syndrome Bits				S7	0	0	0	0	0	0	0	0	1	1	1	1	1	1	1	1
					S6	0	0	0	0	1	1	1	1	0	0	0	0	1	1	1	1
					S5	0	0	1	1	0	0	1	1	0	0	1	1	0	0	1	1
					S4	0	1	0	1	0	1	0	1	0	1	0	1	0	1	0	1
HEX	S3	S2	S1	S0																	
0	0	0	0	0		*	C4	C5	T	C6	T	T	62	C7	T	T	46	T	M	M	T
1	0	0	0	1		C0	T	T	14	T	M	M	T	T	M	M	T	M	T	T	30
2	0	0	1	0		C1	T	T	M	T	34	56	T	T	50	40	T	M	T	T	M
3	0	0	1	1		T	18	8	T	M	T	T	M	M	T	T	M	T	2	24	T
4	0	1	0	0		C2	T	T	15	T	35	57	T	T	51	41	T	M	T	T	31
5	0	1	0	1		T	19	9	T	M	T	T	63	M	T	T	47	T	3	25	T
6	0	1	1	0		T	20	10	T	M	T	T	M	M	T	T	M	T	4	26	T
7	0	1	1	1		M	T	T	M	T	36	58	T	T	52	42	T	M	T	T	M
8	1	0	0	0		C3	T	T	M	T	37	59	T	T	53	43	T	M	T	T	M
9	1	0	0	1		T	21	11	T	M	T	T	M	M	T	T	M	T	5	27	T
A	1	0	1	0		T	22	12	T	33	T	T	M	49	T	T	M	T	6	28	T
B	1	0	1	1		17	T	T	M	T	38	60	T	T	54	44	T	1	T	T	M
C	1	1	0	0		T	23	13	T	M	T	T	M	M	T	T	M	T	7	29	T
D	1	1	0	1		M	T	T	M	T	39	61	T	T	55	45	T	M	T	T	M
E	1	1	1	0		16	T	T	M	T	M	M	T	T	M	M	T	0	T	T	M
F	1	1	1	1		T	M	M	T	32	T	T	M	48	T	T	M	T	M	M	T

NOTE:

1. The table indicates the decoding of the seven syndrome bits to identify the bit-in-error for a single-bit error, or whether a double or triple-bit error was detected. The all-zero case indicattes no error detected.
   * = No errors detected
   # = The number of the single bit-in-error
   T = Two errors detected
   M = three or more errors detected

KEY AC CALCULATIONS — 64-BIT CASCADED CONFIGURATION

Mode	64-Bit Propagation Delay From	To	Total AC Delay for IDT49C465 in 64-bit Mode (L) = Lower slice (U) = Upper slice
Generate	SD Bus	Checkbits out	SD to CBO (L) + PCBI to CBO (U) t SC (L) + t PCC (U)
Detect	MD Bus MD Bus	$\overline{\text{ERR}}$ for 64-bits $\overline{\text{MERR}}$ for 64 bits	MD to SYO (L) + CBI to $\overline{\text{ERR}}$ (U) t MSY (L) + t CE (U) MD to SYO (L) + CBI to $\overline{\text{MERR}}$ t MSY (L) + t CME (U)
Correct (1)	MD BUs	Corrected Data Out	MD to SYO (L) + CBI to SD (U) t MSY (L) + t CS (U) (or) → MD to SYO (U) + PCBI to SD (L) t MSY (U) + t PCS (L)

NOTE:

1. (or) = Whichever is worse.

ABSOLUTE MAXIMUM RATINGS [1]

Symbol	Description	Com'l.	Unit
V_{CC}	Power Supply Voltage	– 0.5 to +7	V
V_{TERM}	Terminal Voltage with Respect to GND	– 0.5 to Vcc +0.5	V
T_A	Operating Temperature	0 to +70	°C
T_{BIAS}	Temperature Under Bias	– 55 to +125	°C
T_{STG}	Storage Temperature	– 55 to +125	°C
I_{OUT}	DC Output Current	30	mA

NOTE:
1. Stresses greater than those listed under ABSOLUTE MAXIMUM RATINGS may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect reliability.

CAPACITANCE (T_A = +25°C, f = 1.0MHz)

Symbol	Parameter[1]	Conditions	Pkg.	Typ.	Unit
C_{IN}	Input Capacitance	V_{IN} = 0V	PGA	10	pF
			PQFP	5	
C_{OUT}	Output Capacitance	V_{OUT} = 0V	PGA	12	pF
			PQFP	7	

NOTE:
1. This parameter is sampled and not 100% tested.

DC ELECTRICAL CHARACTERISTICS OVER OPERATING RANGE

Following Conditions Apply Unless Otherwise Specified:
Commercial: T_A = 0°C to +70°C, Vcc = 5V ± 5%

Symbol	Parameter	Test Conditions[1]		Min.	Typ.[2]	Max.	Unit
V_{IH}	Input HIGH Level[4]	Guaranteed Logic HIGH	Normal Inputs	2	—	—	V
			Hysteresis Inputs	3	—	—	
V_{IL}	Input LOW Level[4]	Guaranteed Logic LOW		—	—	0.8	V
I_{IH}	Input HIGH Current	Vcc = Max, V_{IN} = Vcc		—	—	5	µA
I_{IL}	Input LOW Current	Vcc = Max, V_{IN} = GND		—	—	– 5	µA
I_{OZ}	Off State (Hi-Z)	V_{CC} = 3.6V	V_O = 0V	—	—	– 10	µA
			V_O = 3V	—	—	10	
I_{OS}	Short Circuit Current	V_{CC} = Max.[3]		– 20	—	– 150	mA
V_{OH}	Output HIGH Voltage	Vcc = Min. V_{IN} = V_{IN} or V_{IL}	I_{OH} = – 6mA	2.4	—	—	V
V_{OL}	Output LOW Voltage	Vcc = Min. V_{IN} = V_{IN} or V_{IL}	I_{OL} = 12mA	—	—	.5	V
V_H	Hysteresis	$\overline{CLEAR}$, MLE, $\overline{PLE}$, SLE, $\overline{SYNCLK}$, $\overline{SCLKEN}$		—	200	—	mV
I_{CCQ}	Quiescent Power Supply Current CMOS Levels	V_{IN} = V_{CC} or GND, V_{CC} = Max. All Inputs, Outputs Disabled		—	—	5	mA
I_{CCQT}	Quiescent Power Supply Current TTL Input Levels	V_{IN} = 3.4V, V_{IL} = 0V, V_{CC} = Max. All Inputs, Outputs Disabled		—	—	1	mA/ Input
I_{CCD1}	Dynamic Power Supply Current f = 10MHz	f_{CP} = 10MHz, 50% Duty Cycle V_{IH} = V_{CC}, V_{IL} = GND, Read Mode, Outputs Disabled		—	—	100	mA
I_{CCD2}	Dynamic Power Supply Current f = 20MHz	f_{CP} = 20MHz, 50% Duty Cycle V_{IH} = V_{CC}, V_{IL} = GND, Read Mode, Outputs Disabled		—	—	200	mA

NOTES:
1. For conditions shown as Min. or Max., use appropriate value specified above for the applicable device type.
2. Typical values are at Vcc = 5V, +25°C ambient temperature, and maximum loading.
3. Not more than one output should be shorted at one time. Duration of the short-circuit test should not exceed one second.
4. These input levels provide zero noise immunity and should only be static tested in a noise-free environment.
5. Total supply current is the sum of the Quiescent current and the dynamic current and is calculated as follows:
   $I_{CC} = I_{CCQ} + I_{CCQT} (N_T \times D_T) + I_{CCD} (f_{OP})$
   where: N_T = Total # of quiescent TTL inputs
   D_T = AC Duty Cycle - % or time high (TTL)
   f_{OP} = Operating frequency

AC PARAMETERS — 49C465A

PROPAGATION DELAY TIMES (1,2)

Number	Parameter Name	From Input (edge)	To Output (edge)	32-bit System Standalone Slice CODE ID = 00 Max.	64-bit "Generate only" Slice CODE ID = 01 Max.	64-bit System Lower Slice CODE ID = 10 Max.	64-bit System Upper Slice CODE ID = 11 Max.	Unit	Refer to Timing Diagram Figure
GENERATE (WRITE) PARAMETERS									
01	t_{BC}	BE_N	CBO	15	—	15	15	ns	—
02	t_{BM}	BE_N	MD_{OUT}	15	—	15	15	ns	—
03	t_{MC}	**MD_{IN}**	**CBO**	—	**15**	—	—	ns	10
04	t_{PCC}	**PC_{BI}**	**CBO**	—	—	—	**12**	ns	7
05	t_{PPE}	PX_{IN}	$\overline{PERR}$	12	—	12	12	ns	—
06	t_{SC}	**SD_{IN}**	**CBO**	**14**	**14**	**14**	**14**	ns	7
07	t_{SM}	**SD_{IN}**	MD_{OUT}	12	—	12	12	ns	7
08	t_{SPE}	**SD_{IN}**	$\overline{PERR}$	12	—	12	12	ns	—
DETECT (READ) PARAMETERS									
09	t_{CE}	**CBI**	$\overline{ERR}$ Low	14	—	—	**12**	ns	8, 10
10	t_{CME}	**CBI**	$\overline{MERR}$ Low	15	—	—	15	ns	8, 10
11	t_{CSY}	**CBI**	SYO	12	—	12	—	ns	8, 10
12	t_{ME}	**MD_{IN}**	$\overline{ERR}$	**12**	—	—	12	ns	8, 10
13	t_{MME}	**MD_{IN}**	$\overline{MERR}$	16	—	—	16	ns	8, 10
14	t_{MSY}	**MD_{IN}**	**SYO**	16	—	**12**	**12**	ns	8, 10
CORRECT (READ) PARAMETERS									
15	t_{CS}	**CBI**	**SD_{OUT}**	16	—	—	**16**	ns	8, 11
16	t_{MP}	**MD_{IN}**	P_X	18	—	18	18	ns	8, 11
17	t_{MS}	**MD_{IN}**	**SD_{OUT}**	**14**	—	—	—	ns	8, 11
18	t_{MSY}	**MD_{IN}**	**SYO**	16	—	**12**	**12**	ns	8, 11
19	t_{PCS}	**PCBI**	**SD_{OUT}**	—	—	**13**	—	ns	11
DIAGNOSTIC PARAMETERS									
20	t_{CLR}	CLEAR = Low	SD_{OUT}	15	—	15	15	ns	15
21	t_{MIS}	MODE ID	SD_{OUT}	15	—	15	15	ns	15

NOTES:
1. Where "edge" is not specified, both HIGH and LOW edges are implied.
2. **BOLD** indicates critical system parameters.

AC PARAMETERS — 49C465A

PROPAGATION DELAY TIMES FROM LATCH ENABLES

Number	Parameter Name	Parameter Description From Input	(edge)	To Output	(edge)	Max.	Unit	Refer to Timing Diagram Figure
22	t_{MLC}			CBO	*	16	ns	13
23	t_{MLE}			$\overline{ERR}$	*	13	ns	8, 10, 11
24	t_{MLME}	MLE =	HIGH	$\overline{MERR}$	*	16	ns	8
25	t_{MLP}			P_x	*	18	ns	8, 11
26	t_{MLS}			SD_{OUT}	*	18	ns	8, 10, 11
27	t_{MLSY}			SYO	*	15	ns	8, 10
28	t_{PLS}	$\overline{PLE}$ =	LOW	SD_{OUT}	*	10	ns	8, 11
29	t_{PLP}	$\overline{PLE}$ =	LOW	P_x	*	13	ns	8, 11
30	t_{SLC}	SLE =	HIGH	CBO	*	16	ns	7, 9
31	t_{SLM}	SLE =	HIGH	MD_{OUT}	*	12	ns	7, 9

NOTE:
* = Both HIGH and LOW edges are implied.

ENABLE AND DISABLE TIMES

Number	Parameter Name	Parameter Description From Input	(edge)	To Output	(edge)	Min.	Max.	Unit	Refer to Timing Diagram Figure
32	t_{BESZx}	BEN =	HIGH	SD_{OUT}	*	2	13	ns	8, 10, 11
33	t_{BESxZ}		LOW		Hi-Z	2	11	ns	
34	t_{BEPZx}	BEN =	HIGH	P_{OUT}	*	2	13	ns	8, 11
35	t_{BEPxZ}		LOW		Hi-Z	2	11	ns	
36	t_{CECZx}	$\overline{CBOE}$ =	LOW	CBO	*	2	13	ns	7, 9
37	t_{CECxZ}		HIGH		Hi-Z	2	11	ns	
38	t_{MEMZx}	$\overline{MOE}$ =	LOW	MD_{OUT}	*	2	13	ns	7, 9
39	t_{MEMxZ}		HIGH		Hi-Z	2	11	ns	8, 10
40	t_{SESZx}	$\overline{SOE}$ =	LOW	SD_{OUT}	*	2	13	ns	8, 10
41	t_{SESxZ}		HIGH		Hi-Z	2	11	ns	7, 9

NOTE:
* = Delay to both edges.

SET-UP AND HOLD TIMES — 49C465A

Number	Parameter Name	Parameter Description From Input	(edge)	To Output	(edge)	Min.	Unit	Refer to Timing Diagram Figure
42	t_{SSLS}	SDIN Set-up	*	before SLE =	LOW	3	ns	7, 9
43	t_{SSLH}	SDIN Hold	*	after SLE =	LOW	3	ns	7, 9
44	t_{MMLS}	MDIN Set-up	*	before MLE =	LOW	3	ns	8, 10, 11
45	t_{MMLH}	MDIN Hold	*	after MLE =	LOW	3	ns	8, 10, 11
46	t_{CMLS}	CBI Set-up	*	before MLE =	LOW	3	ns	8, 10, 11
47	t_{CMLH}	CBI Hold	*	after MLE =	LOW	3	ns	8, 10, 11
48	t_{MPLS}	MDIN Set-up	*	before $\overline{PLE}$ =	HIGH	10	ns	—
49	t_{MPLH}	MDIN Hold	*	after $\overline{PLE}$ =	HIGH	0	ns	—
50	t_{CPLS}	CBI Set-up	*	before $\overline{PLE}$ =	HIGH	10	ns	—
51	t_{CPLH}	CBI Hold	*	after $\overline{PLE}$ =	HIGH	0	ns	—
52	t_{CPCLS}	PCBI Set-up	*	before $\overline{PLE}$ =	HIGH	10	ns	—
53	t_{CPCLH}	PCBI Hold	*	after $\overline{PLE}$ =	HIGH	0	ns	—
DIAGNOSTIC SET-UP AND HOLD TIMES								
54	t_{CSCS}	CBI Set-up	*			10	ns	15
55	t_{MSCS}	MDIN Set-up	*	before SYNCLK =	HIGH	10	ns	15
56	t_{MLSCS}	MLE Set-up =	HIGH			10	ns	15
57	t_{SESCS}	SCLKEN Set-up =	LOW			3	ns	15
58	t_{SESCH}	SCLKEN Hold =	LOW	after SYNCLK =	HIGH	3	ns	15

NOTE:
* = Where “edge” is not specified, both HIGH and LOW edges are implied.

MINIMUM PULSE WIDTH

Number	Parameter name	Minimum Pulse Width Input	Conditions	Min.	Unit	Refer to Timing Diagram Figure
59	t_{CLEAR}	Min. $\overline{CLEAR}$ LOW time to clear diag. registers	Data = Valid	8	ns	14
60	t_{MLE}	Min. MLE HIGH time to strobe new data	MD, CBI = Valid	5	ns	—
61	t_{PLE}	Min. $\overline{PLE}$ HIGH time to strobe new data	SD = Valid	5	ns	—
62	t_{SLE}	Min. SLE HIGH time to strobe new data	SD = Valid	5	ns	—
63	t_{SYNCLK}	Min. SYNCLK HIGH time to clock in new data	SCKEN = LOW	5	ns	14

Input Rise Levels	GND to 3V
Input Rise/Fall Times	1V/ns
Input Timing Reference Levels	1.5V
Output Reference Levels	1.5V
Output Load	See Figure 18

64-BIT LOWER SLICE APPLICATION EXCEPTION (49C465A)

Number	Parameter Name	Parameter Description From Input	(edge)	To Output	(edge)	Typ.	Min.	Max.	Unit	Refer to Timing Diagram Figure
39(a)	t_{MEMxZ}	MOE	HIGH	MD_{OUT}	Hi-Z	—	—	11	ns	12
	t_{PCBI}(1)	MOE	HIGH	PCB_{IN}		23	—	—	ns	12
26(a)	t_{MLS}	MLE	HIGH	SD_{OUT}		—	28	—	ns	12

64-BIT UPPER SLICE APPLICATION EXCEPTION (49C465A)

Number	Parameter Name	Parameter Description From Input	(edge)	To Output	(edge)	Min.	Max.	Unit	Refer to Timing Diagram Figure
39(a)	t_{MEMxZ}	MOE	HIGH	MD_{OUT}	Hi-Z	—	11	ns	13
44(a)	t_{MMLS}	MD_{IN} Set-up				5.5	—	ns	13
45(a)	t_{MMLH}	MD_{IN} Hold				5.5	—	ns	13
46(a) (2)	t_{CMLS}	CBI Set-up				—	—	ns	13
47(a) (2)	t_{CMLH}	CBI Hold				—	—	ns	13

Number	Parameter Name	Minimum Pulse Width Input	Conditions	Min.	Max.	Unit	Refer to Timing Diagram Figure
60(a)	t_{MLE}	Min. MLE HIGH time to strobe new data	MD, CBI = Valid	7.5	—	ns	13

Number	Parameter Name	Parameter Description From Input	(edge)	To Output	(edge)	Typ.	Min.	Max.	Unit	Refer to Timing Diagram Figure
	t_{CBI}(3)	MOE	HIGH	CB_{IN}		23	—	—	ns	13
26(a)	t_{MLS}	MLE	HIGH	SD_{OUT}		—	28	—	ns	13

NOTES:
1. Partial Checkbit input (PCBI) of 64-bit lower slice comes from the Syndrome output of the upper slice unit. Valid input time is shown above as t_{PCBI}.
2. There is no setup and hold time for CBI bus input on 64-bit upper slice operation mode.
3. Valid CBI signal comes from the Syndrome output of lower slice. Typical time of valid CB_{IN} is shown as t_{CBI}.

AC PARAMETERS — 49C465

PROPAGATION DELAY TIMES [1,2]

				32-bit System Standalone Slice	64-bit "Generate only" Slice	64-bit System			
						Lower Slice	Upper Slice		
				CODE ID = 00	CODE ID = 01	CODE ID = 10	CODE ID = 11		
Number	Parameter Name	Parameter Description: From Input (edge)	Parameter Description: To Output (edge)	Max.	Max.	Max.	Max.	Unit	Refer to Timing Diagram Figure
GENERATE (WRITE) PARAMETERS									
01	t_{BC}	BE_N	CBO	20	—	20	20	ns	—
02	t_{BM}	BE_N	MD_{OUT}	20	—	20	20	ns	—
03	t_{MC}	**MD_{IN}**	**CBO**	—	**17**	—	—	ns	10
04	t_{PCC}	**PC_{BI}**	**CBO**	—	—	—	**15**	ns	7
05	t_{PPE}	PX_{IN}	$\overline{PERR}$	15	—	15	15	ns	—
06	t_{SC}	**SD_{IN}**	**CBO**	**16**	**16**	**16**	**16**	ns	7
07	t_{SM}	**SD_{IN}**	MD_{OUT}	15	—	15	15	ns	7
08	t_{SPE}	**SD_{IN}**	$\overline{PERR}$	15	—	15	15	ns	—
DETECT (READ) PARAMETERS									
09	t_{CE}	**CBI**	$\overline{ERR}$ Low	16	—	—	**15**	ns	8, 10
10	t_{CME}	**CBI**	$\overline{MERR}$ Low	20	—	—	20	ns	8, 10
11	t_{CSY}	**CBI**	SYO	15	—	12	—	ns	8, 10
12	t_{ME}	**MD_{IN}**	$\overline{ERR}$ Low	**15**	—	—	15	ns	8, 10
13	t_{MME}	**MD_{IN}**	$\overline{MERR}$ Low	20	—	—	20	ns	8, 10
14	t_{MSY}	**MD_{IN}**	**SYO**	18	—	**15**	**15**	ns	8, 10
CORRECT (READ) PARAMETERS									
15	t_{CS}	**CBI**	**SD_{OUT}**	20	—	—	**20**	ns	8, 11
16	t_{MP}	**MD_{IN}**	P_X	20	—	20	20	ns	8, 11
17	t_{MS}	**MD_{IN}**	**SD_{OUT}**	**16**	—	—	—	ns	8, 11
18	t_{MSY}	**MD_{IN}**	**SYO**	18	—	**15**	**15**	ns	8, 11
19	t_{PCS}	**PCBI**	**SD_{OUT}**	—	—	**15**	—	ns	11
DIAGNOSTIC PARAMETERS									
20	t_{CLR}	CLEAR = Low	SD_{OUT}	20	—	20	20	ns	15
21	t_{MIS}	MODE ID	SD_{OUT}	20	—	20	20	ns	15

NOTES:

1. Where "edge" is not specified, both HIGH and LOW edges are implied.
2. **BOLD** indicates critical system parameters.

AC PARAMETERS — 49C465

PROPAGATION DELAY TIMES FROM LATCH ENABLES

Number	Parameter Name	Parameter Description: From Input	(edge)	To Output	(edge)	Max.	Unit	Refer to Timing Diagram Figure
22	t_{MLC}			CBO	*	20	ns	13
23	t_{MLE}			$\overline{ERR}$	*	15	ns	8, 10, 11
24	t_{MLME}	MLE =	HIGH	$\overline{MERR}$	*	20	ns	8
25	t_{MLP}			P_X	*	20	ns	8, 11
26	t_{MLS}			SD_{OUT}	*	20	ns	8, 10, 11
27	t_{MLSY}			SYO	*	18	ns	8, 10
28	t_{PLS}	$\overline{PLE}$ =	LOW	SD_{OUT}	*	12	ns	8, 11
29	t_{PLP}	$\overline{PLE}$ =	LOW	P_X	*	16	ns	8, 11
30	t_{SLC}	SLE =	HIGH	CBO	*	20	ns	7, 9
31	t_{SLM}	SLE =	HIGH	MD_{OUT}	*	15	ns	7, 9

NOTE:
* = Both HIGH and LOW edges are implied.

ENABLE AND DISABLE TIMES

Number	Parameter Name	Parameter Description: From Input	(edge)	To Output	(edge)	Min.	Max.	Unit	Refer to Timing Diagram Figure
32	t_{BESZX}	BEN =	HIGH	SD_{OUT}	*	2	15	ns	8, 10, 11
33	t_{BESXZ}		LOW		Hi-Z	2	13	ns	
34	t_{BEPZX}	BEN =	HIGH	P_{OUT}	*	2	15	ns	8, 11
35	t_{BEPXZ}		LOW		Hi-Z	2	13	ns	
36	t_{CECZX}	$\overline{CBOE}$ =	LOW	CBO	*	2	15	ns	7, 9
37	t_{CECXZ}		HIGH		Hi-Z	2	13	ns	
38	t_{MEMZX}	$\overline{MOE}$ =	LOW	MD_{OUT}	*	2	15	ns	7, 9
39	t_{MEMXZ}		HIGH		Hi-Z	2	13	ns	8, 10
40	t_{SESZX}	$\overline{SOE}$ =	LOW	SD_{OUT}	*	2	15	ns	8, 10
41	t_{SESXZ}		HIGH		Hi-Z	2	13	ns	7, 9

NOTE:
* = Delay to both edges.

SET-UP AND HOLD TIMES — 49C465

Number	Parameter Name	Parameter Description: From Input	(edge)	To Output	(edge)	Min.	Unit	Refer to Timing Diagram Figure
42	t_{SSLS}	SDIN Set-up	*	before SLE =	LOW	4	ns	7, 9
43	t_{SSLH}	SDIN Hold	*	after SLE =	LOW	4	ns	7, 9
44	t_{MMLS}	MDIN Set-up	*	before MLE =	LOW	4	ns	8, 10, 11
45	t_{MMLH}	MDIN Hold	*	after MLE =	LOW	4	ns	8, 10, 11
46	t_{CMLS}	CBI Set-up	*	before MLE =	LOW	4	ns	8, 10, 11
47	t_{CMLH}	CBI Hold	*	after MLE =	LOW	4	ns	8, 10, 11
48	t_{MPLS}	MDIN Set-up	*	before $\overline{PLE}$ =	HIGH	12	ns	—
49	t_{MPLH}	MDIN Hold	*	after $\overline{PLE}$ =	HIGH	0	ns	—
50	t_{CPLS}	CBI Set-up	*	before $\overline{PLE}$ =	HIGH	12	ns	—
51	t_{CPLH}	CBI Hold	*	after $\overline{PLE}$ =	HIGH	0	ns	—
52	t_{CPCLS}	PCBI Set-up	*	before $\overline{PLE}$ =	HIGH	12	ns	—
53	t_{CPCLH}	PCBI Hold	*	after $\overline{PLE}$ =	HIGH	0	ns	—

DIAGNOSTIC SET-UP AND HOLD TIMES

Number	Parameter Name	From Input	(edge)	To Output	(edge)	Min.	Unit	Refer to Timing Diagram Figure
54	t_{CSCS}	CBI Set-up	*			12	ns	15
55	t_{MSCS}	MDIN Set-up	*	before SYNCLK =	HIGH	12	ns	15
56	t_{MLSCS}	MLE Set-up =	HIGH			12	ns	15
57	t_{SESCS}	SCLKEN Set-up =	LOW			4	ns	15
58	t_{SESCH}	SCLKEN Hold =	LOW	after SYNCLK =	HIGH	4	ns	15

NOTE:
* = Where “edge” is not specified, both HIGH and LOW edges are implied.

MINIMUM PULSE WIDTH

Number	Parameter name	Minimum Pulse Width: Input	Conditions	Min.	Unit	Refer to Timing Diagram Figure
59	t_{CLEAR}	Min. $\overline{CLEAR}$ LOW time to clear diag. registers	Data = Valid	8	ns	14
60	t_{MLE}	Min. MLE HIGH time to strobe new data	MD, CBI = Valid	5	ns	—
61	t_{PLE}	Min. $\overline{PLE}$ HIGH time to strobe new data	SD = Valid	5	ns	—
62	t_{SLE}	Min. SLE HIGH time to strobe new data	SD = Valid	5	ns	—
63	t_{SYNCLK}	Min. SYNCLK HIGH time to clock in new data	SCKEN = LOW	5	ns	14

Input Rise Levels	GND to 3V
Input Rise/Fall Times	1V/ns
Input Timing Reference Levels	1.5V
Output Reference Levels	1.5V
Output Load	See Figure 18

64-BIT LOWER SLICE APPLICATION EXCEPTION (49C465)

Number	Parameter Name	Parameter Description: From Input	(edge)	To Output	(edge)	Typ.	Min.	Max.	Unit	Refer to Timing Diagram Figure
39(a)	t_{MEMxZ}	MOE	HIGH	MD_{OUT}	Hi-Z	—	—	13	ns	12
	t_{PCBI}(1)	MOE	HIGH	PCB_{IN}		27	—	—	ns	12
26(a)	t_{MLS}	MLE	HIGH	SD_{OUT}		—	34	—	ns	12

64-BIT UPPER SLICE APPLICATION EXCEPTION (49C465)

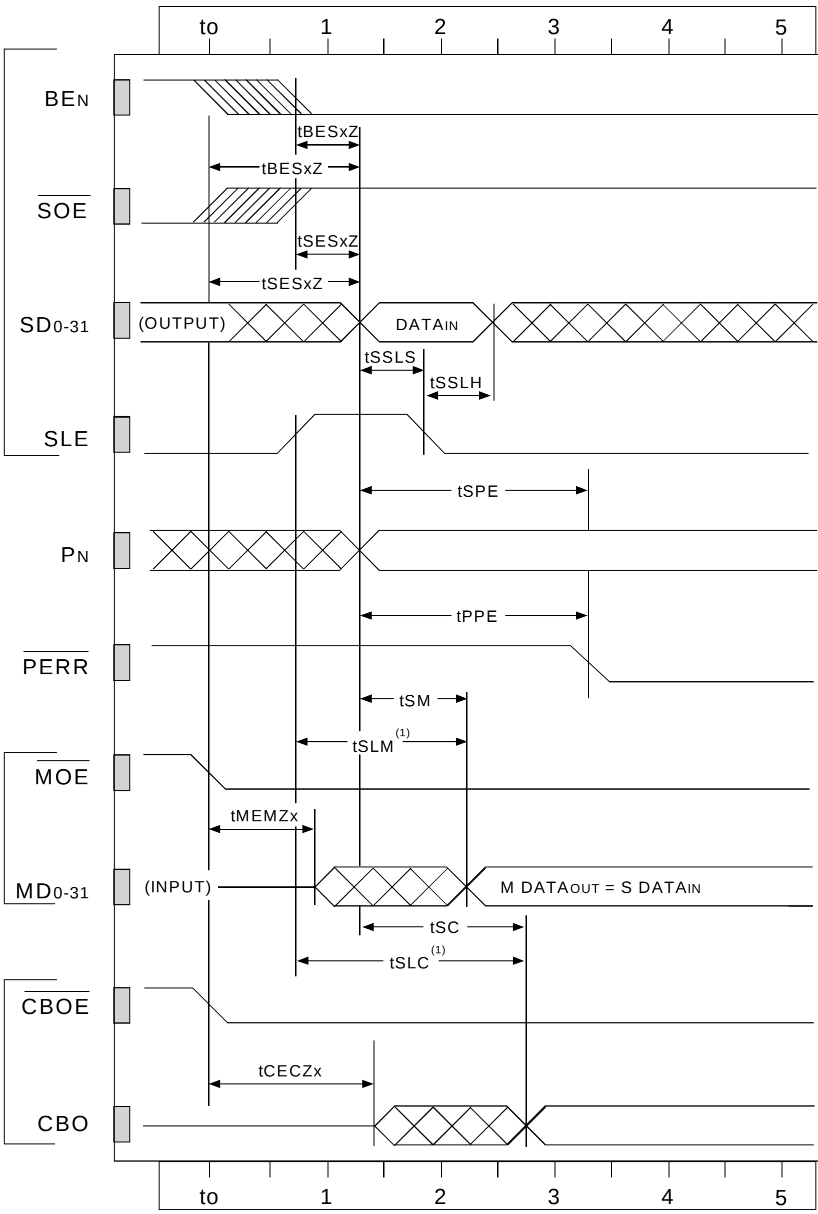
Number	Parameter Name	Parameter Description: From Input	(edge)	To Output	(edge)	Min.	Max.	Unit	Refer to Timing Diagram Figure
39(a)	t_{MEMxZ}	MOE	HIGH	MD_{OUT}	Hi-Z	—	13	ns	13
44(a)	t_{MMLS}	MD_{IN} Set-up				6.5	—	ns	13
45(a)	t_{MMLH}	MD_{IN} Hold				6.5	—	ns	13
46(a) (2)	t_{CMLS}	CBI Set-up				—	—	ns	13
47(a) (2)	t_{CMLH}	CBI Hold				—	—	ns	13

Number	Parameter Name	Minimum Pulse Width: Input	Conditions	Min.	Max.	Unit	Refer to Timing Diagram Figure
60(a)	t_{MLE}	Min. MLE HIGH time to strobe new data	MD, CBI = Valid	8.5	—	ns	13

Number	Parameter Name	Parameter Description: From Input	(edge)	To Output	(edge)	Typ.	Min.	Max.	Unit	Refer to Timing Diagram Figure
	t_{CBI}(3)	MOE	HIGH	CB_{IN}		27	—	—	ns	13
26(a)	t_{MLS}	MLE	HIGH	SD_{OUT}		—	34	—	ns	13

NOTES:
1. Partial Checkbit input (PCBI) of 64-bit lower slice comes from the Syndrome output of the upper slice unit. Valid input time is shown above as t_{PCBI}.
2. There is no setup and hold time for CBI bus input on 64-bit upper slice operation mode.
3. Valid CBI signal comes from the Syndrome output of lower slice. Typical time of valid CB_{IN} is shown as t_{CBI}.

AC TIMING DIAGRAMS—32-BIT CONFIGURATION

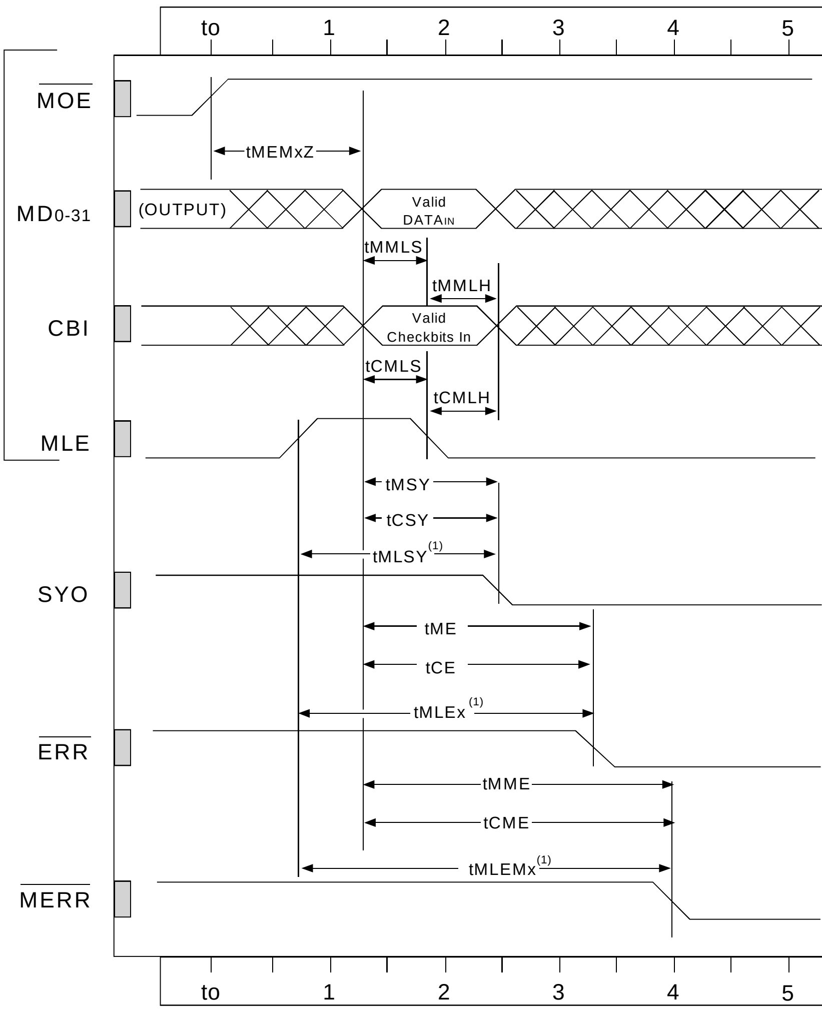


Parameter Name	Propagation Delay From To	Min./Max.
tBESxZ min.	BEN - Low to SDOUT Disabled	min.
tBESxZ max.	BEN - Low to SDOUT Disabled	max.
tSESxZ min.	$\overline{SOE}$ - Low to SDOUT Disabled	min.
tSESxZ max.	$\overline{SOE}$ - Low to SDOUT Disabled	max.
tSSLS	SDIN Set-up to SLEIN = Low	min.
tSSLH	SDIN Hold to SLEIN = Low	min.
tSPE	SDIN to $\overline{PERR}$OUT	max.
tPPE	PX to $\overline{PERR}$OUT	max.
tSM	SDIN to MDOUT	max.
tSLM(1)	SLE = High to MDOUT	max.
tMEMZx	$\overline{MOE}$ = Low to MDOUT Enabled	max.
tSC	SDIN to CBO	max.
tSLC(1)	SLE = High to $\overline{CBO}$	max.
tCECZx	$\overline{CBOE}$ = Low to CBO Enable	max.

NOTE:
1. Assumes that System Data is valid at least 3ns (Com.) before SLE goes HIGH.

Figure 7. 32-Bit Generate Timing

AC TIMING DIAGRAMS—32-BIT CONFIGURATION

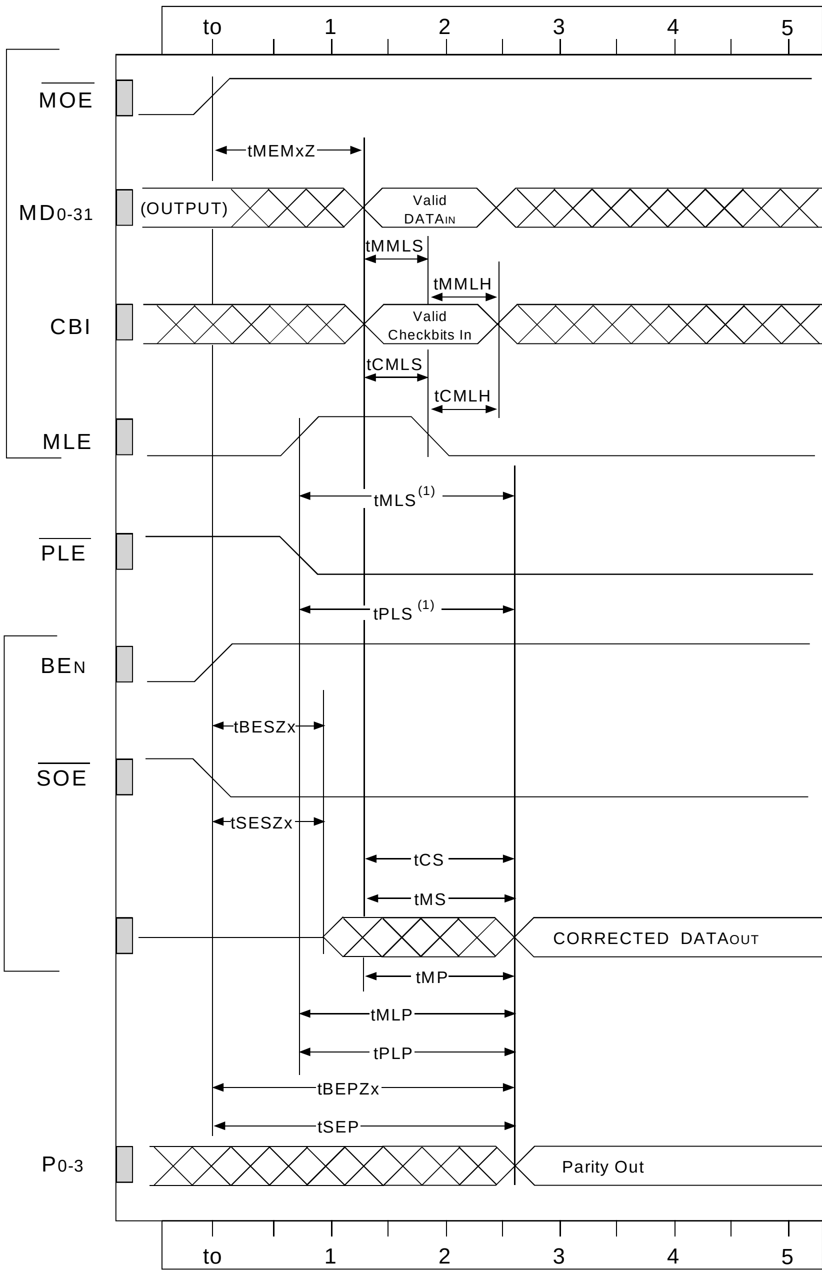


Parameter Name	Propagation Delay From / To	Min./Max.
tMEMxZ	MOE - High to MDOUT Disabled	max.
tMMLS	MDIN Set-up to MLE = Low	min.
tMMLH	MDIN Hold to MLE = Low	min.
tCMLS	Checkbit Set-up to MLE = Low	min.
tCMLH	Checkbit Hold to MLE = Low	min.
tMSY	MDIN to SYOOUT	max.
tCSY	Checkbits in to SYOOUT	max.
tMLSY(1)	MLE = High to SYOOUT	max.
tME	MDIN to ERR = Low	max.
tCE	Checkbits in to ERR = Low	max.
tMLEx(1)	MLE = High to ERR = Low(1)	max.
tMME	MDIN to MERR = Low	max.
tCME	Checkbits in to MERR = Low	max.
tMLEMx(1)	MLE = High to MERR = Low(1)	max.

NOTE:
1. Assumes that Memory Data and Checkbits are valid at least 3ns before MLE goes HIGH.

Figure 8. 32-Bit Detect Timing

AC TIMING DIAGRAMS—32-BIT CONFIGURATION

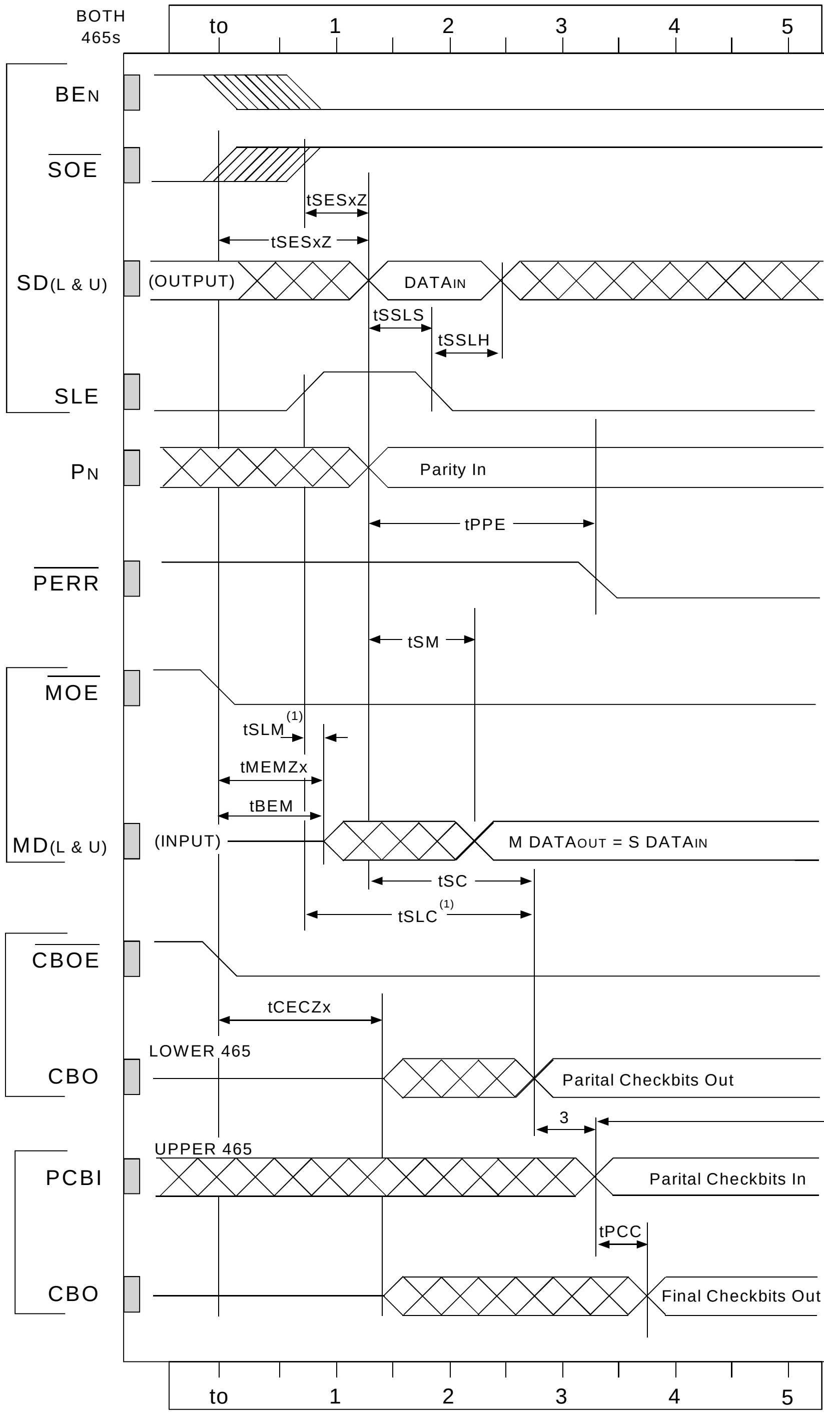


Parameter Name	Propagation Delay From To	Min./Max.
t_{MEMxZ}	$\overline{MOE}$ - High to MD_{OUT} Disabled	max.
t_{MMLS}	MD_{IN} Set-up to MLE = Low	min.
t_{MMLH}	MD_{IN} Hold to MLE = Low	min.
t_{CMLS}	Checkbit Set-up to MLE = Low	min.
t_{CMLH}	Checkbit Hold to MLE = Low	min.
t_{MLS} (1)	MLE_{IN} = High to SD_{OUT} (1)	max.
t_{PLS} (1)	$\overline{PLE}$ = Low to SD_{OUT} (1)	max.
t_{BESZx}	BE_N = High to SD_{OUT} Enabled	max.
t_{SESZx}	$\overline{SOE}$ = Low to SD_{OUT} Enabled	max.
t_{CS}	CBI to Corrected SD_{OUT}	max.
t_{MS}	MD_{IN} to Corrected SD_{OUT}	max.
t_{MP}	MD_{IN} to Parity Out	max.
t_{MLP}	MLE = High to Parity Out	max.
t_{PLP}	$\overline{PLE}$ = Low to Parity Out	max.
t_{BEPZx}	BE_N = High to Parity Out	max.
t_{SEP}	$\overline{SOE}$ = Low to Parity Out	max.

NOTE:
1. Assumes that Memory Data and Checkbits are valid at least 3ns before MLE goes HIGH.

Figure 9. 32-Bit Correct Timing

AC TIMING DIAGRAMS—64-BIT CONFIGURATION

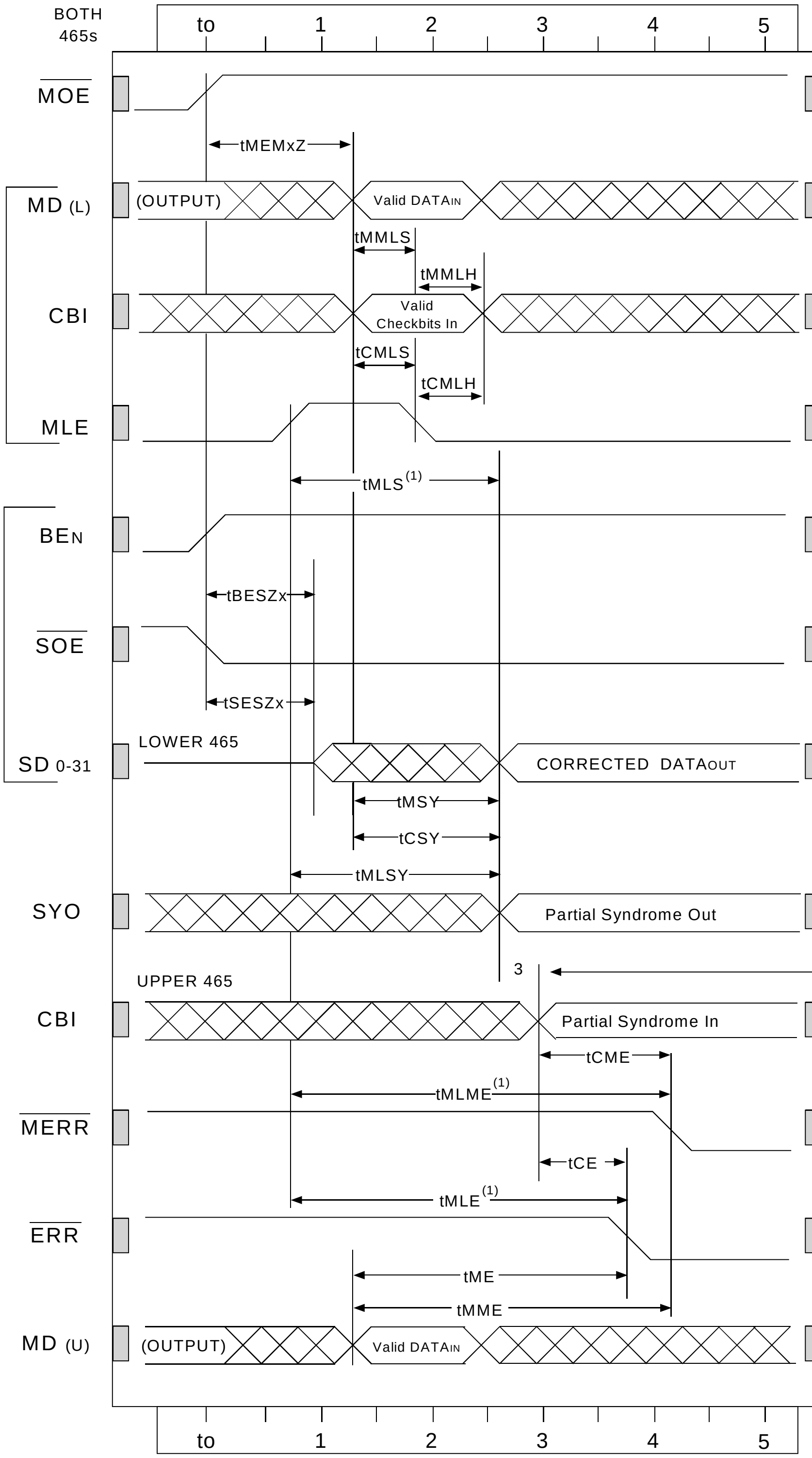


Parameter Name	Propagation Delay From To	Min./ Max.
tSESxZ min.	$\overline{SOE}$ - High to SD_{OUT} Disabled	min.
tSESxZ max.	$\overline{SOE}$ - High to SD_{OUT} Disabled	max.
tSSLS	SD_{IN} Set-up to SLE_{IN} = Low	min.
tSSLH	SD_{IN} Hold to SLE_{IN} = Low	min.
tPPE	P_X to $\overline{PERR}$	max.
tSM	SD_{IN} to MD_{OUT}	max.
tSLM[(1)]	SLE = High to MD_{OUT}	max.
tMEMZx	$\overline{MOE}$ = Low to MD_{OUT} Enabled	max.
tBEM	BE_{IN} to MD_{OUT}	max.
tSC	SD Lower In to CBO	max.
tSLC[(1)]	SLE_{IN} = High to CBO[(1)]	max.
tCECZx	$\overline{CBOE}$ = Low to CBO Enabled	max.
tPCC	PCBI to CBO	max.

NOTE:
1. Assumes that SystemData is valid at least 3ns before SLE goes HIGH.

Figure 10. 64-Bit Generate Timing—(64-Bit Cascading System)

AC TIMING DIAGRAMS—64-BIT CONFIGURATION

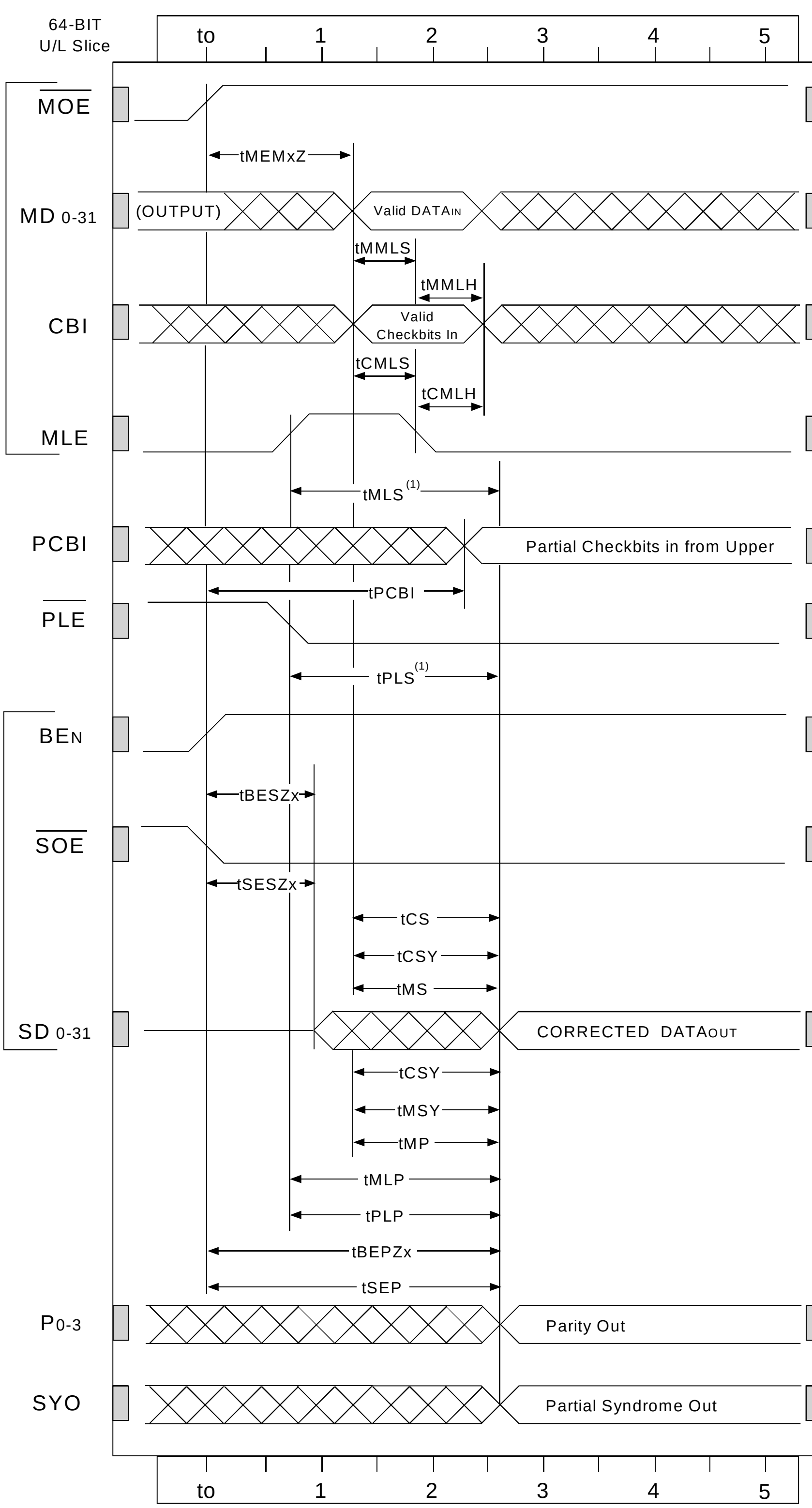


Parameter Name	Propagation Delay From To	Min./ Max.
tMEMxZ	$\overline{MOE}$ = High to MDOUT Disabled	max.
tMMLS	MDIN Set-up to MLE = Low	min.
tMMLH	MDIN Hold to MLE = Low	min.
tCMLS	CBI Set-up to MLE = Low	min.
tCMLH	CBI Hold to MLE = Low	min.
tMLS(1)	MLE = High to SDOUT(1)	max.
tBESZx	BEN = High to SDOUT Enabled	max.
tSESZx	$\overline{SOE}$ = Low to SDOUT Enabled	max.
tMSY	MD Lower In to SYOOUT	max.
tCSY	CBI to SYO	max.
tMLSY	MLE = High to SYO	max.
tCME	CBI to $\overline{MERR}$	max.
tMLME(1)	MLE = High to $\overline{MERR}$	max.
tCE	CBI to $\overline{ERR}$	max.
tMLE(1)	MLE = High to $\overline{ERR}$	max.
tME	MDIN to $\overline{ERR}$	max.
tMME	MDIN to $\overline{MERR}$	max.

NOTE:
1. Assumes that SystemData is valid at least 3ns before SLE goes HIGH.

Figure 11. 64-Bit Detect Timing

AC TIMING DIAGRAMS—64-BIT CONFIGURATION

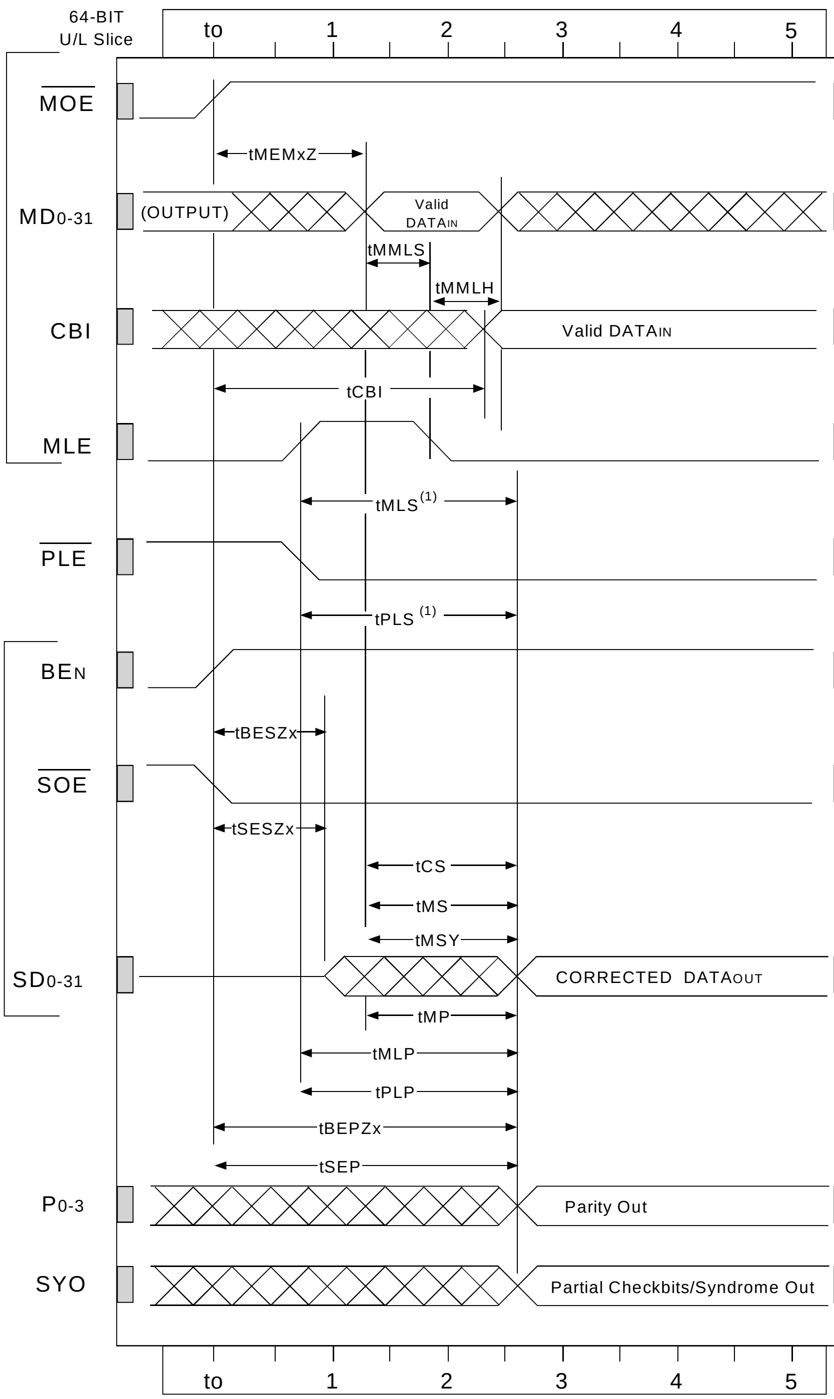


Parameter Name	Propagation Delay From / To	Min./Max.
tMEMxZ	$\overline{MOE}$ = High to MDOUT Disabled	max.
tMMLS	MDIN Set-up to MLE = Low	min.
tMMLH	MDIN Hold to MLE = Low	min.
tCMLS	CBI Set-up to MLE = Low	min.
tCMLH	CBI Hold to MLE = Low	min.
tMLS(1)	MLEIN = High to SDOUT(1)	max.
tPLS(1)	$\overline{PLE}$ = Low to SDOUT(1)	max.
tBESZx	BEN = High to SDOUT Enabled	max.
tSESZx	$\overline{SOE}$ = Low to SDOUT Enabled	max.
tCS	CBI to Corrected SDOUT	max.
tCSY	CBI to Syndrome	max.
tMS	MDIN to Corrected SDOUT	max.
tCSY	CBI to Syndrome	max.
tMSY	MDIN to Syndrome	max.
tMP	MDIN to Parity Out	max.
tMLP	MLE = High to Parity Out	max.
tPLP	$\overline{PLE}$ = Low to Parity Out	max.
tBEPZx	BEN = High to Parity Out	max.
tSEP	$\overline{SOE}$ = Low to Parity Out	max.

NOTE:
1. Assumes that Memory Data and Checkbits are valid at least 4ns before MLE goes HIGH.

Figure 12. 64-Bit Correct Timing (Lower Slice)

AC TIMING DIAGRAMS—64-BIT CONFIGURATION

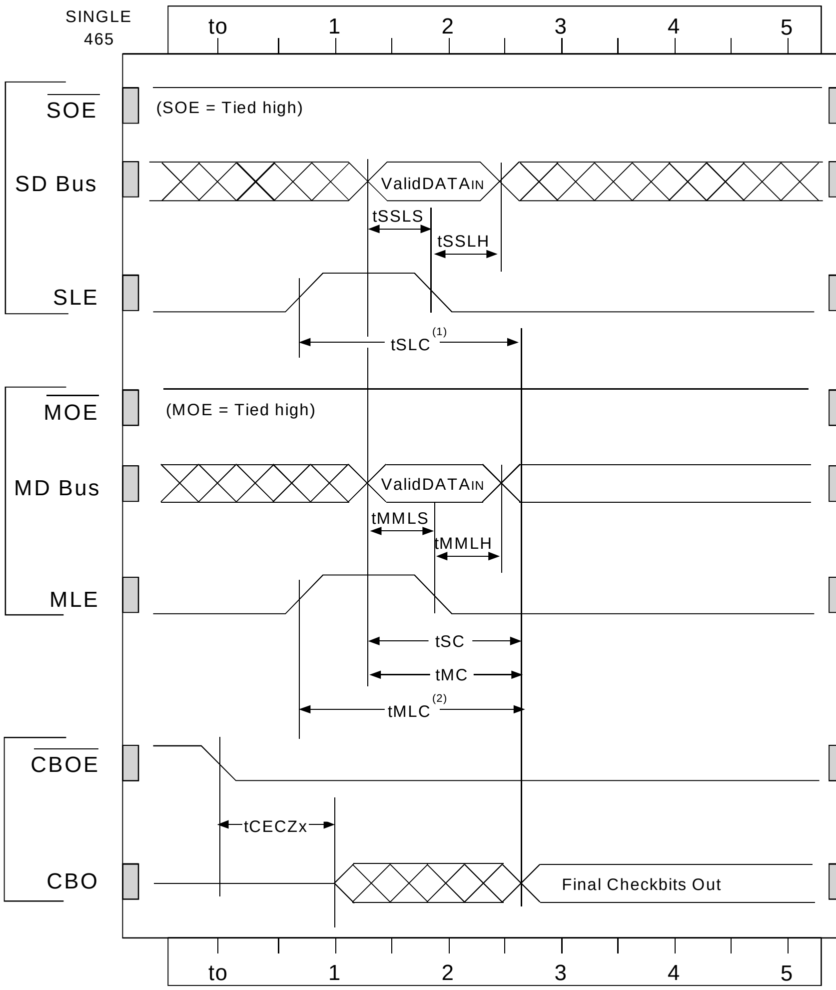


Parameter Name	Propagation Delay From To	Min./Max.
tMEMxZ	$\overline{MOE}$ = High to MDOUT Disabled	max.
tMMLS	MDIN Set-up to MLE = Low	min.
tMMLH	MDIN Hold to MLE = Low	min.
tCMLS	CBI Set-up to MLE = Low	min.
tCMLH	CBI Hold to MLE = Low	min.
tMLS(1)	MLEIN = High to SDOUT(1)	max.
tPLS (1)	$\overline{PLE}$ = Low to SDOUT(1)	max.
tBESZx	BEN = High to SDOUT Enabled	max.
tSESZx	$\overline{SOE}$ = Low to SDOUT Enabled	max.
tCS	CBI to Corrected SDOUT	max.
tMS	MDIN to Corrected SDOUT	max.
tMSY	MDIN to Corrected SDOUT	max.
tMP	MDIN to Parity Out	max.
tMLP	MLE = High to Parity Out	max.
tPLP	$\overline{PLE}$ = Low to Parity Out	max.
tBEPZx	BEN = High to Parity Out	max.
tSEP	$\overline{SOE}$ = Low to Parity Out	max.

NOTE:
1. Assumes that Memory Data and Checkbits are valid at least 4ns before MLE goes HIGH.

Figure 13. 64-Bit Correct Timing (Upper Slice)

AC TIMING DIAGRAMS—64-BIT CONFIGURATION

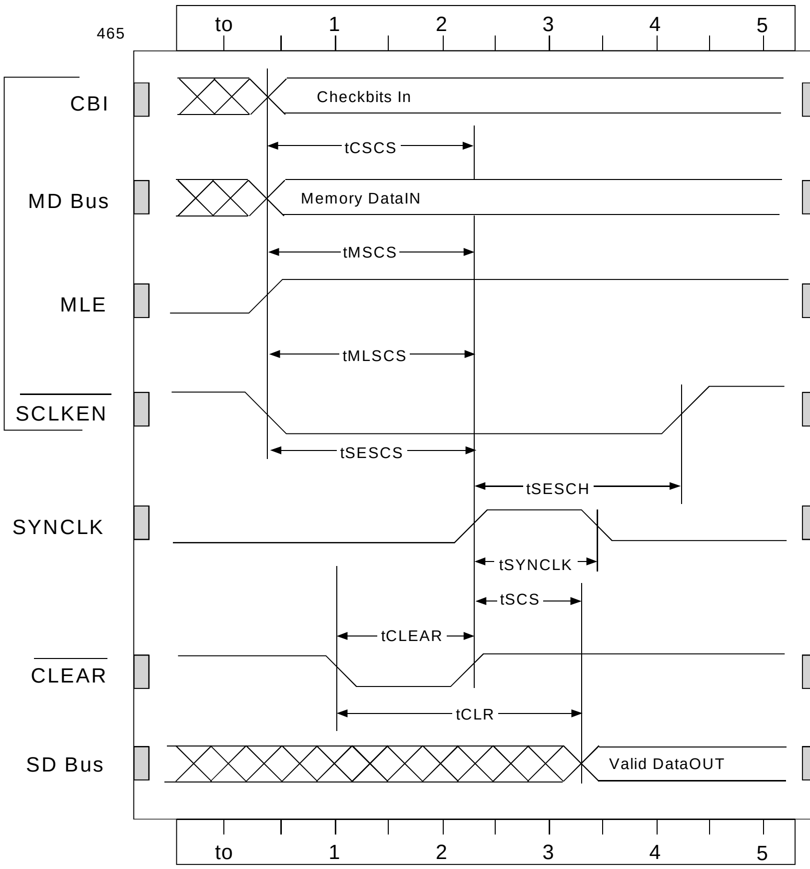


Parameter Name	Propagation Delay From / To	Min./ Max.
tSSLS	SDIN Set-up to SLEIN = Low	min.
tSSLH	SDIN Hold to SLEIN = Low	min.
tSLC(1)	SLE = High to CBO (1)	max.
tMMLS	MDIN Set-up to MLEIN = Low	min.
tMMLH	MDIN Hold to MLEIN = Low	min.
tSC	Bits 32-63 to CBO	max.
tMC	Bits 0-31 to CBO	max.
tMLC(2)	MLEIN = High to CBO (2)	max.
tCECZx	CBOE = Low to CBO Enabled	max.

NOTES:
1. Assumes that System Data is valid at least 3ns before SLE goes HIGH.
2. Assumes that Memory Data is valid at least 4ns before MLE goes HIGH.

Figure 14. 64-Bit Single Chip "Generate Only" Timing

AC TIMING DIAGRAMS—DIAGNOSTIC TIMING

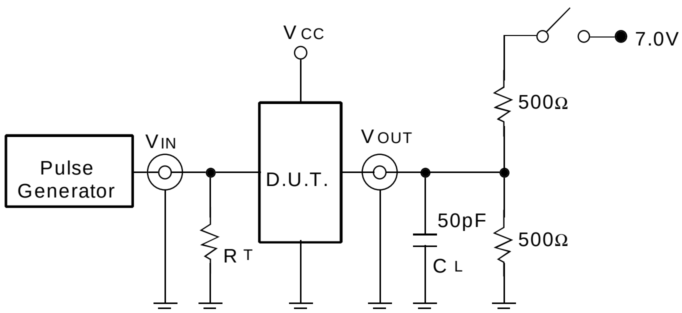


Parameter Name	Propagation Delay From To	Min./ Max.
tCSCS	CBI Set-up to SYNCLK = High	
tMSCS	MDIN Set-up to SYNCLK = High	min.
tMLSCS	MLE = High Set-up to SYNCLK = High	max.
tSESCS	SCLKEN Set-up to SYNCLK = High	min.
tSESCH	SCLKEN = Hold After SYNCLK = High	min.
tSYNCLK	SCLKEN Pulse Witdh	max.
tSCS	SCLKEN = High to SDOUT	max.
tCLEAR	CLEAR Pulse Witch	max.
tCLR	CLEAR = Low to SDOUT	max.

Figure 15. 32-Bit Diagnostic Timing

TEST WAVEFORMS

TEST CIRCUITS FOR ALL OUTPUTS



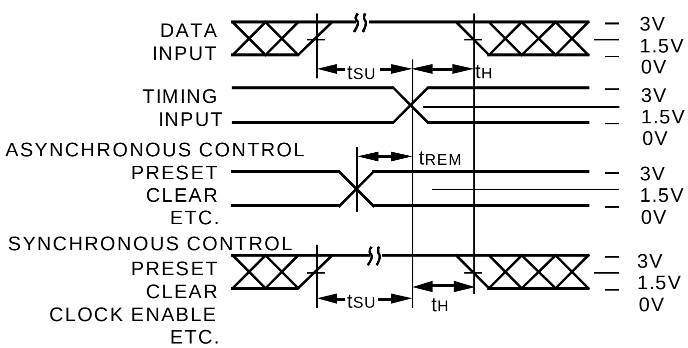
SWITCH POSITION

Test	Switch
Open Drain Disable Low Enable Low	Closed
All Other Tests	Open

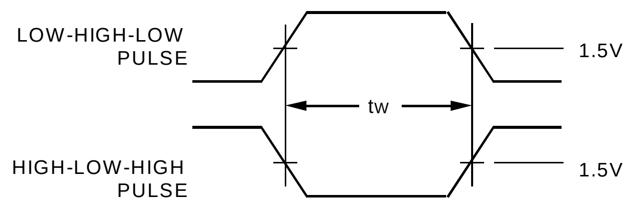
DEFINITIONS:

C_L= Load capacitance: includes jig and probe capacitance.
R_T = Termination resistance: should be equal to Z_{OUT} of the Pulse Generator.

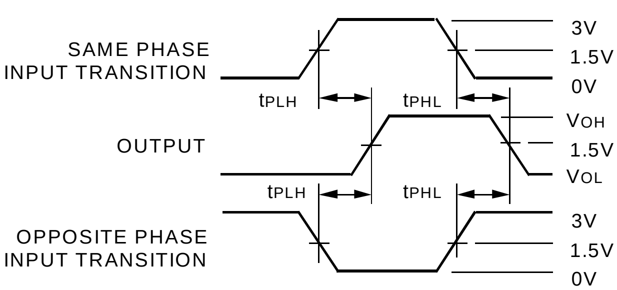
SET-UP, HOLD, AND RELEASE TIMES



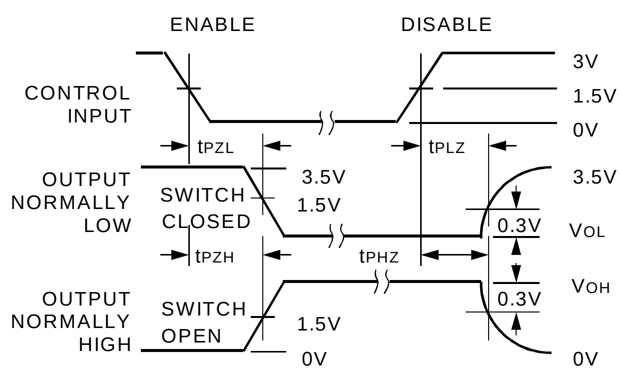
PULSE WIDTH



PROPAGATION DELAY



ENABLE AND DISABLE TIMES



NOTES:

1. Diagram shown for input Control Enable-LOW and input Control Disable-HIGH.
2. Pulse Generator for All Pulses: Rate ≤ 1.0MHz; t_F ≤ 2.5ns; t_R ≤ 2.5ns.

ORDERING INFORMATION

IDT XXXXX XX

Device Type Package

PQF	Plastic Quad Flatpack
G	Pin Grid Array

49C465	32-Bit Flow-thru™ Error Detection and
49C465A	Correction Unit

CORPORATE HEADQUARTERS
2975 Stender Way
Santa Clara, CA 95054

for SALES:
800-345-7015 or 408-727-6116
fax: 408-492-8674
www.idt.com*

**To search for sales office near you, please click the sales button found on our home page or dial the 800# above and press 2.*