PROGRAMMABLE SKEW PLL CLOCK DRIVER TURBOCLOCK™

QS5992

FEATURES:

- 4 pairs of programmable skew outputs
- Low skew: 200ps same pair, 250ps all outputs
- Selectable positive or negative edge synchronization: Excellent for DSP applications
- Synchronous output enable
- Output frequency: 6.25MHz to 100MHz
- 2x, 4x, 1/2, and 1/4 outputs
- 5V with CMOS outputs
- 3 skew grades:
  QS5992-2: t_{SKEW0}<250ps
  QS5992-5: t_{SKEW0}<500ps
  QS5992-7: t_{SKEW0}<750ps
- 3-level inputs for skew and PLL range control
- PLL bypass for DC testing
- External feedback, internal loop filter
- 46mA I_{OL} high drive outputs
- Low Jitter: <200ps peak-to-peak
- Outputs drive 50Ω terminated lines
- Pin-compatible with Cypress CY7B992
- Available in PLCC Package

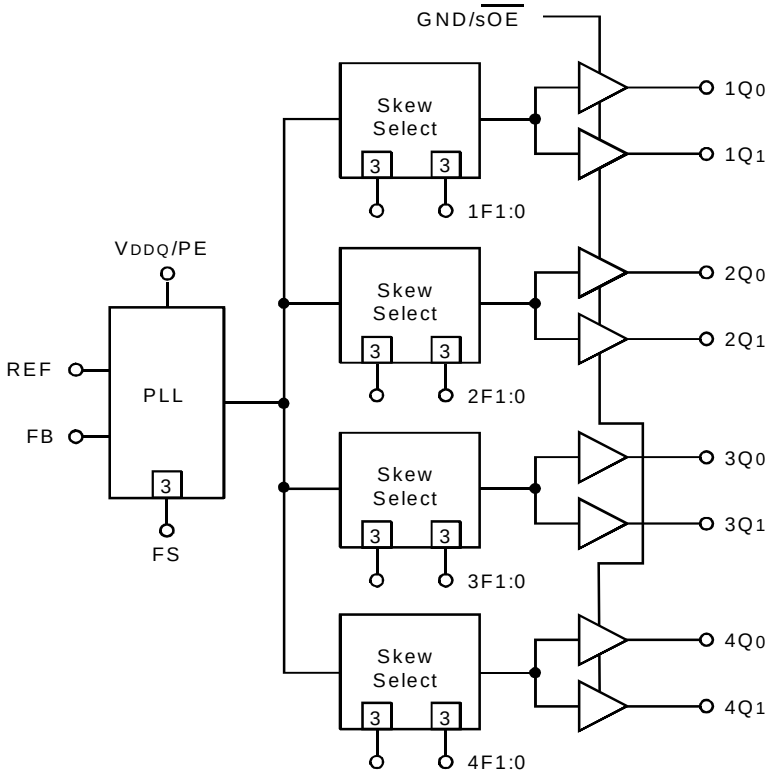
DESCRIPTION:

The QS5992 is a high fanout PLL based clock driver intended for high performance computing and data-communications applications. A key feature of the programmable skew is the ability of outputs to lead or lag the REF input signal. The QS5992 has eight programmable skew outputs in four banks of 2. Skew is controlled by 3-level input signals that may be hard-wired to appropriate HIGH-MID-LOW levels.

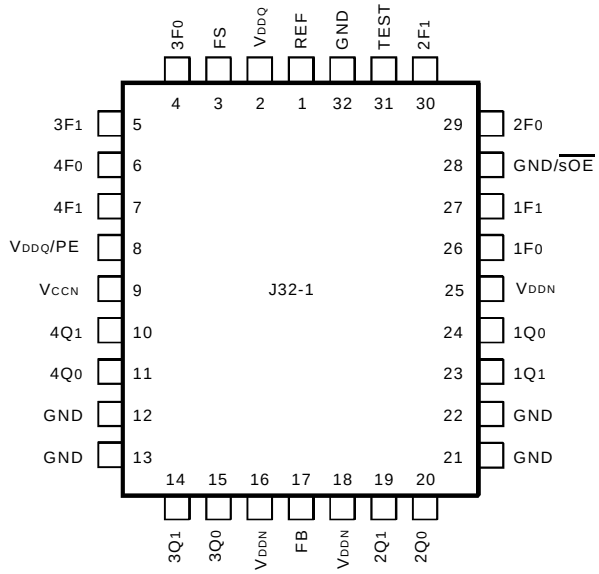
The QS5992 maintains Cypress CY7B992 compatibility while providing two additional features: Synchronous Output Enable (GND/$\overline{sOE}$), and Positive/Negative Edge Synchronization (V_{DDQ}/PE). When the GND/$\overline{sOE}$ pin is held low, all the outputs are synchronously enabled (CY7B992 compatibility). However, if GND/$\overline{sOE}$ is held high, all the outputs except 3Q0 and 3Q1 are synchronously disabled.

Furthermore, when the V_{DDQ}/PE is held high, all the outputs are synchronized with the positive edge of the REF clock input (CY7B992 compatibility). When V_{DDQ}/PE is held low, all the outputs are synchronized with the negative edge of REF.

FUNCTIONAL BLOCK DIAGRAM



PIN CONFIGURATION



PLCC
TOP VIEW

ABSOLUTE MAXIMUM RATINGS (1)

Symbol	Rating	Max.	Unit
	Supply Voltage to Ground	–0.5 to +7	V
V_I	DC Input Voltage	–0.5 to +7	V
	Maximum Power Dissipation (T_A = 85°C)	0.8	W
T_{STG}	Storage Temperature Range	–65°C to +150°C	°C

NOTE:
1. Stresses greater than those listed under ABSOLUTE MAXIMUM RATINGS may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect reliability.

CAPACITANCE (T_A = 25° C, f = 1MHz, V_{IN} = 0V)

Parameter	Description	Typ.	Max.	Unit
C_{IN}	Input Capacitance	5	7	pF

NOTE:
1. Capacitance applies to all inputs except TEST, FS, and nF1:0.

PIN DESCRIPTION

Pin Name	Type	Description
REF	IN	Reference Clock Input
FB	IN	Feedback Input
TEST (1)	IN	When MID or HIGH, disables PLL (except for conditions of Note 1). REF goes to all outputs. Skew selections (see Control Summary Table) remain in effect. Set LOW for normal operation.
GND/ $\overline{sOE}$ (1)	IN	Synchronous Output Enable. When HIGH, it stops clock outputs (except $3Q_0$ and $3Q_1$) in a LOW state - $3Q_0$ and $3Q_1$ may be used as the feedback signal to maintain phase lock. When TEST is held at MID level and GND/$\overline{sOE}$ is HIGH, the nF[1:0] pins act as output disable controls for individual banks when nF[1:0] = LL. Set GND/$\overline{sOE}$ LOW for normal operation.
V_{DDQ}/PE	IN	Selectable positive or negative edge control. When LOW/HIGH the outputs are synchronized with the negative/positive edge of the reference clock.
nF[1:0]	IN	3-level inputs for selecting 1 of 9 skew taps or frequency functions
FS	IN	Selects appropriate oscillator circuit based on anticipated frequency range. (See PLL Programmable Skew Range.)
nQ[1:0]	OUT	Four banks of two outputs with programmable skew
V_{DDN}	PWR	Power supply for output buffers
V_{DDQ}	PWR	Power supply for phase locked loop and other internal circuitry
GND	PWR	Ground

NOTE:
1. When TEST = MID and GND/$\overline{sOE}$ = HIGH, PLL remains active with nF[1:0] = LL functioning as an output disable control for individual output banks. Skew selections remain in effect unless nF[1:0] = LL.

PROGRAMMABLE SKEW

Output skew with respect to the REF input is adjustable to compensate for PCB trace delays, backplane propagation delays or to accommodate requirements for special timing relationships between clocked components. Skew is selectable as a multiple of a time unit t_U which is of the order of a nanosecond (see PLL Programmable Skew Range and Resolution Table). There are nine skew configurations available for each output pair. These configurations are chosen by the $nF_{1:0}$ control pins. In order to minimize the number of control pins, 3-level inputs (HIGH-MID-LOW) are used, they are intended for but not restricted to hard-wiring. Undriven 3-level inputs default to the MID level. Where programmable skew is not a requirement, the control pins can be left open for the zero skew default setting. The Control Summary Table shows how to select specific skew taps by using the $nF_{1:0}$ control pins.

EXTERNAL FEEDBACK

By providing external feedback, the QS5992 gives users flexibility with regard to skew adjustment. The FB signal is compared with the input REF signal at the phase detector in order to drive the VCO. Phase differences cause the VCO of the PLL to adjust upwards or downwards accordingly.

An internal loop filter moderates the response of the VCO to the phase detector. The loop filter transfer function has been chosen to provide minimal jitter (or frequency variation) while still providing accurate responses to input frequency changes.

PLL PROGRAMMABLE SKEW RANGE AND RESOLUTION TABLE

	FS = LOW	FS = MID	FS = HIGH	Comments
Timing Unit Calculation (t_U)	1/(44 x F_{NOM})	1/(26 x F_{NOM})	1/(16 x F_{NOM})	
VCO Frequency Range (F_{NOM}) (1,2)	25 to 35MHz	35 to 60MHz	60 to 100 MHz (4)	
Skew Adjustment Range (3) Max Adjustment:	±9.09ns	±9.23ns	±9.38ns	ns
	±49º	±83º	±135º	Phase Degrees
	±14%	±23%	±37%	% of Cycle Time
Example 1, F_{NOM} = 25MHz	t_U = 0.91ns	—	—	
Example 2, F_{NOM} = 30MHz	t_U = 0.76ns	—	—	
Example 3, F_{NOM} = 40MHz	—	t_U = 0.96ns	—	
Example 4, F_{NOM} = 50MHz	—	t_U = 0.77ns	—	
Example 5, F_{NOM} = 80MHz	—	—	t_U = 0.78ns	

NOTES:

1. The device may be operated outside recommended frequency ranges without damage, but functional operation is not guaranteed. Selecting the appropriate FS value based on input frequency range allows the PLL to operate in its 'sweet spot' where jitter is lowest.
2. The level to be set on FS is determined by the nominal operating frequency of the VCO and Time Unit Generator. The VCO frequency always appears at $1Q_{1:0}$, $2Q_{1:0}$, and the higher outputs when they are operated in their undivided modes. The frequency appearing at the REF and FB inputs will be the same as the VCO when the output connected to FB is undivided. The frequency of the REF and FB inputs will be 1/2 or 1/4 the VCO frequency when the part is configured for a frequency multiplication by using a divided output as the FB input.
3. Skew adjustment range assumes that a zero skew output is used for feedback. If a skewed Q output is used for feedback, then adjustment range will be greater. For example if a $4t_U$ skewed output is used for feedback, all other outputs will be skewed $–4t_U$ in addition to whatever skew value is programmed for those outputs. 'Max adjustment' range applies to output pairs 3 and 4 where ± $6t_U$ skew adjustment is possible and at the lowest F_{NOM} value.
4. The maximum REF Clock Input Frequency is 85MHz. Use Q/2 or Q/4 as feedback and use the Control Summary Table explicitly for output frequency to 100MHz.

CONTROL SUMMARY TABLE FOR FEEDBACK SIGNALS

nF1:0	Skew (Pair #1, #2)	Skew (Pair #3)	Skew (Pair #4)
LL (1)	$–4t_U$	Divide by 2	Divide by 2
LM	$–3t_U$	$–6t_U$	$–6t_U$
LH	$–2t_U$	$–4t_U$	$–4t_U$
ML	$–1t_U$	$–2t_U$	$–2t_U$
MM	Zero Skew	Zero Skew	Zero Skew
MH	$1t_U$	$2t_U$	$2t_U$
HL	$2t_U$	$4t_U$	$4t_U$
HM	$3t_U$	$6t_U$	$6t_U$
HH	$4t_U$	Divide by 4	Inverted (2)

NOTES:

1. LL disables outputs if TEST = MID and GND/$\overline{sOE}$ = HIGH.
2. When pair #4 is set to HH (inverted), GND/$\overline{sOE}$ disables pair #4 HIGH when V_{DDQ}/PE= HIGH, GND/$\overline{sOE}$ disables pair #4 LOW when V_{DDQ}/PE= LOW.

RECOMMENDED OPERATING RANGE

Symbol	Description	QS5992-5, -7 (Industrial)		QS5992-2 (Commercial)		Unit
		Min.	Max.	Min.	Max.	
V_{DD}	Power Supply Voltage	4.5	5.5	4.75	5.25	V
T_A	Ambient Operating Temperature	-40	+85	0	+70	°C

DC ELECTRICAL CHARACTERISTICS OVER OPERATING RANGE

Symbol	Parameter	Conditions		Min.	Max.	Unit
V_{IH}	Input HIGH Voltage	Guaranteed Logic HIGH (REF, FB Inputs Only)		V_{DD}–1.35	—	V
V_{IL}	Input LOW Voltage	Guaranteed Logic LOW (REF, FB Inputs Only)		—	1.35	V
V_{IHH}	Input HIGH Voltage (1)	3-Level Inputs Only		V_{DD}–1	—	V
V_{IMM}	Input MID Voltage (1)	3-Level Inputs Only		V_{DD}/2–0.5	V_{DD}/2+0.5	V
V_{ILL}	Input LOW Voltage (1)	3-Level Inputs Only		—	1	V
I_{IN}	Input Leakage Current (REF, FB Inputs Only)	V_{IN} = V_{DD} or GND V_{DD} = Max.		—	±5	µA
I_3	3-Level Input DC Current (TEST, FS, nF1:0)	V_{IN} = V_{DD}	HIGH Level	—	±200	µA
		V_{IN} = V_{DD}/2	MID Level	—	±50	
		V_{IN} = GND	LOW Level	—	±200	
I_{PU}	Input Pull-Up Current (V_{DDQ}/PE)	V_{DD} = Max., V_{IN} = GND		—	±100	µA
I_{PD}	Input Pull-Down Current (GND/$\overline{sOE}$)	V_{DD} = Max., V_{IN} = V_{DD}		—	±100	µA
V_{OH}	Output HIGH Voltage	V_{DD} = Min., I_{OH} = –16mA		—	—	V
		V_{DD} = Min., I_{OH} = –40mA		V_{DD}–0.75	—	V
V_{OL}	Output LOW Voltage	V_{DD} = Min., I_{OL} = 46mA		—	0.45	V
I_{OS}	Output Short Circuit Current (2)	V_{DD} = Max., V_O = GND		—	N/A	mA

NOTES:
1. These inputs are normally wired to V_{DD}, GND, or unconnected. Internal termination resistors bias unconnected inputs to V_{DD}/2. If these inputs are switched, the function and timing of the outputs may be glitched, and the PLL may require an additional t_{LOCK} time before all datasheet limits are achieved.
2. This output is not to be shorted.

POWER SUPPLY CHARACTERISTICS

Symbol	Parameter	Test Conditions	Typ.	Max.	Unit
I_{DDQ}	Quiescent Power Supply Current	V_{DD} = Max., TEST = MID, REF = LOW, GND/$\overline{sOE}$ = LOW, All outputs unloaded	10	40	mA
ΔI_{DD}	Power Supply Current per Input HIGH	V_{DD} = Max., V_{IN} = 3.4V	0.4	1.5	mA
I_{DDD}	Dynamic Power Supply Current per Output	V_{DD} = Max., C_L = 0pF	100	160	µA/MHz
I_{TOT}	Total Power Supply Current	V_{DD} = 5V, F_{REF} = 20MHz, C_L = 240pF (1)	43	—	mA
		V_{DD} = 5V, F_{REF} = 33MHz, C_L = 240pF (1)	63	—	mA
		V_{DD} = 5V, F_{REF} = 66MHz, C_L = 240pF (1)	117	—	mA

NOTE:
1. For eight outputs, each loaded with 30pF.

INPUT TIMING REQUIREMENTS

Symbol	Description (1)	Min.	Max.	Unit
t_R, t_F	Maximum input rise and fall times, 0.8V to 2V	—	10	ns/V
t_{PWC}	Input clock pulse, HIGH or LOW	3	—	ns
D_H	Input duty cycle	10	90	%
R_{EF}	Reference Clock Input	10	85	MHz

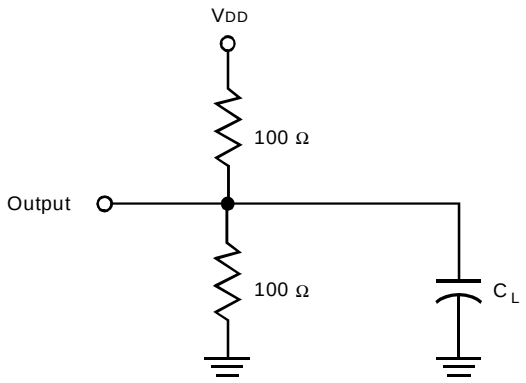
NOTE:
1. Where pulse width implied by D_H is less than t_{PWC} limit, t_{PWC} limit applies.

SWITCHING CHARACTERISTICS OVER OPERATING RANGE

Symbol	Parameter		QS5992-2			QS5992-5			QS5992-7			Unit
			Min.	Typ.	Max.	Min.	Typ.	Max.	Min.	Typ.	Max.	
F_{NOM}	VCO Frequency Range		See PLL Programmable Skew Range and Resolution Table									
t_{RPWH}	REF Pulse Width HIGH (1)		3	—	—	3	—	—	3	—	—	ns
t_{RPWL}	REF Pulse Width LOW (1)		3	—	—	3	—	—	3	—	—	ns
t_U	Programmable Skew Time Unit		See Skew Selection Table for Output Pairs									
t_{SKEWPR}	Zero Output Matched-Pair Skew (xQ_0, xQ_1) (1,2,3)		—	0.05	0.2	—	0.1	0.25	—	0.1	0.25	ns
t_{SKEW0}	Zero Output Skew (All Outputs) C_L = 0pF (1,4)		—	0.1	0.25	—	0.25	0.5	—	0.3	0.75	ns
t_{SKEW1}	Output Skew (Rise-Rise, Fall-Fall, Same Class Outputs) (1,3)		—	0.25	0.5	—	0.6	0.7	—	0.6	1	ns
t_{SKEW2}	Output Skew (Rise-Fall, Nominal-Inverted, Divided-Divided) (1,5)		—	0.5	01.2	—	0.6	1.5	—	0.5	1.5	ns
t_{SKEW3}	Output Skew (Rise-Rise, Fall-Fall, Different Class Outputs) (1,5)		—	0.25	0.5	—	0.5	0.7	—	0.7	1.2	ns
t_{SKEW4}	Output Skew (Rise-Fall, Nominal-Divided, Divided-Inverted) (1,2)		—	0.5	0.9	—	0.6	1.7	—	1.2	1.7	ns
t_{DEV}	Device-to-Device Skew (1,2,6)		—	—	0.75	—	—	1.25	—	—	1.65	ns
t_{PD}	REF Input to FB Propagation Delay (1,8)		–0.25	0	0.25	–0.5	0	0.5	–0.7	0	0.7	ns
t_{ODCV}	Output Duty Cycle Variation from 50% (1)		–1.2	0	1.2	–1.2	0	1.2	–1.5	0	1.5	ns
t_{PWH}	Output HIGH Time Deviation from 50% (1,9)		—	—	3	—	—	4	—	—	5.5	ns
t_{PWL}	Output LOW Time Deviation from 50% (1,10)		—	—	3	—	—	4	—	—	5.5	ns
t_{ORISE}	Output Rise Time (1)		0.5	2	2.5	0.5	2	3.5	0.5	3	5	ns
t_{OFALL}	Output Fall Time (1)		0.5	2	2.5	0.5	2	3.5	0.5	3	5	ns
t_{LOCK}	PLL Lock Time (7)		—	—	0.5	—	—	0.5	—	—	0.5	ms
t_{JR}	Cycle-to-Cycle Output Jitter	RMS	—	—	25	—	—	25	—	—	25	ps
		Peak-to-Peak	—	—	200	—	—	200	—	—	200	

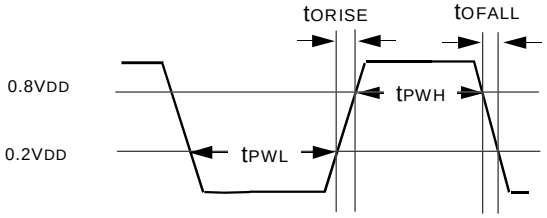
NOTES:
1. All timing tolerances apply for $F_{NOM} \geq 25$MHz.
2. Skew is the time between the earliest and the latest output transition among all outputs for which the same t_U delay has been selected when all are loaded with the specified load.
3. t_{SKEWPR} is the skew between a pair of outputs (xQ_0 and xQ_1) when all eight outputs are selected for $0t_U$.
4. t_{SKEW0} is the skew between outputs when they are selected for $0t_U$.
5. There are 3 classes of outputs: Nominal (multiple of t_U delay), Inverted ($4Q_0$ and $4Q_1$ only with $4F_0 = 4F_1$ = HIGH), and Divided (3Qx and 4Qx only in Divide-by-2 or Divide-by-4 mode).
6. t_{DEV} is the output-to-output skew between any two devices operating under the same conditions (V_{DD}, ambient temperature, air flow, etc.)
7. t_{LOCK} is the time that is required before synchronization is achieved. This specification is valid only after V_{DD} is stable and within normal operating limits. This parameter is measured from the application of a new signal or frequency at REF or FB until t_{PD} is within specified limits.
8. t_{PD} is measured with REF input rise and fall times (from 0.8V to 2V) of 1ns.
9. Measured at $0.8V_{DD}$.
10. Measured at $0.2V_{DD}$.
11. Refer to Input Timing Requirements table for more detail.

AC TEST LOADS AND WAVEFORMS

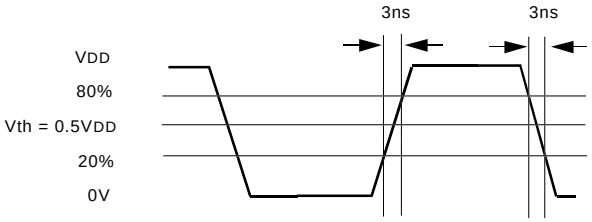


CL = 50pF (CL = 30pF for -2 and -5 devices)

TEST LOAD

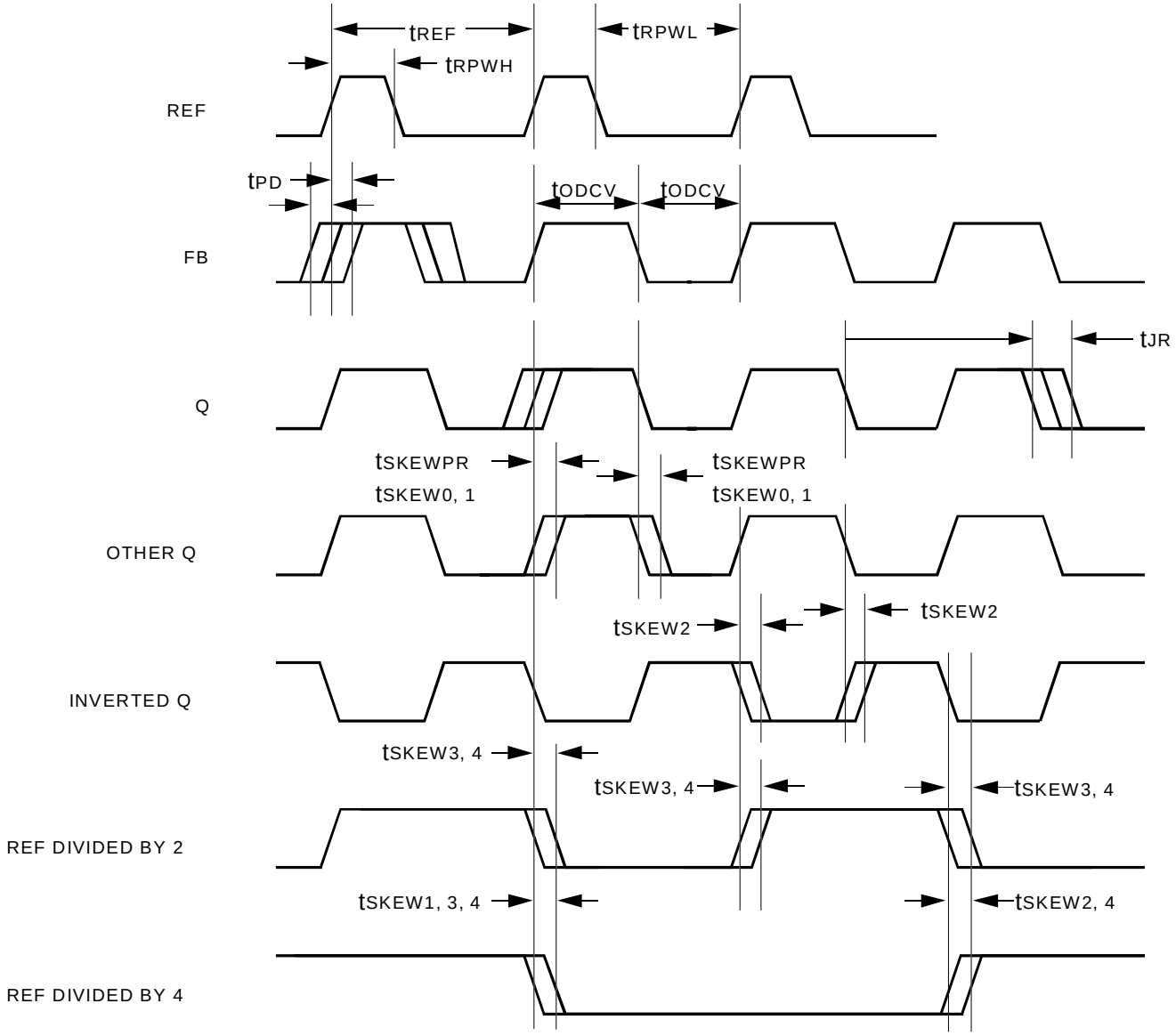


CMOS OUTPUT WAVEFORM



CMOS INPUT TEST WAVEFORM

AC TIMING DIAGRAM



NOTES:

V_{DDQ}/PE: The AC Timing Diagram applies to V_{DDQ}/PE=V_{DD}. For V_{DDQ}/PE=GND, the negative edge of FB aligns with the negative edge of REF, divided outputs change on the negative edge of REF, and the positive edges of the divide-by-2 and the divide-by-4 signals align.

Skew: The time between the earliest and the latest output transition among all outputs for which the same t_U delay has been selected when all are loaded with 50pF (30pF for -2 and -5) and terminated with 50Ω to V_{DD}/2.

t_{SKEWPR}: The skew between a pair of outputs (xQ_0 and xQ_1) when all eight outputs are selected for $0t_U$.

t_{SKEW0}: The skew between outputs when they are selected for $0t_U$.

t_{DEV}: The output-to-output skew between any two devices operating under the same conditions (V_{DD}, ambient temperature, air flow, etc.)

t_{ODCV}: The deviation of the output from a 50% duty cycle. Output pulse width variations are included in t_{SKEW2} and t_{SKEW4} specifications.

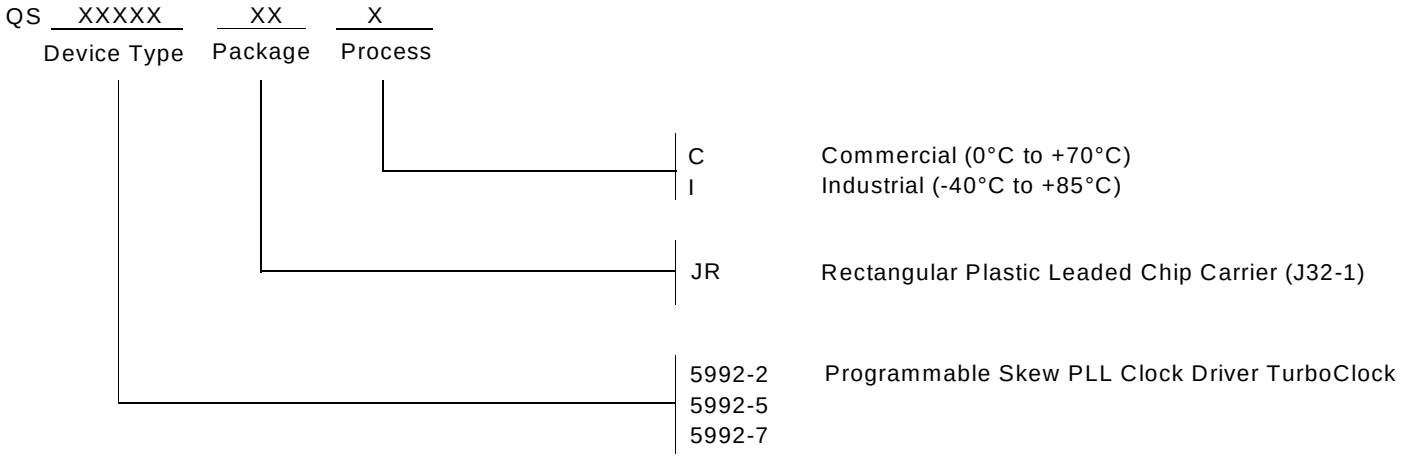
t_{PWH} is measured at $0.8V_{DD}$.

t_{PWL} is measured at $0.2V_{DD}$.

t_{ORISE} and t_{OFALL} are measured between $0.2\ V_{DD}$ and $0.8V_{DD}$.

t_{LOCK}: The time that is required before synchronization is achieved. This specification is valid only after V_{DD} is stable and within normal operating limits. This parameter is measured from the application of a new signal or frequency at REF or FB until t_{PD} is within specified limits.

ORDERING INFORMATION



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