



## LOW SKEW CMOS PLL CLOCK DRIVER WITH INTEGRATED LOOP FILTER

**QS5931**

### FEATURES:

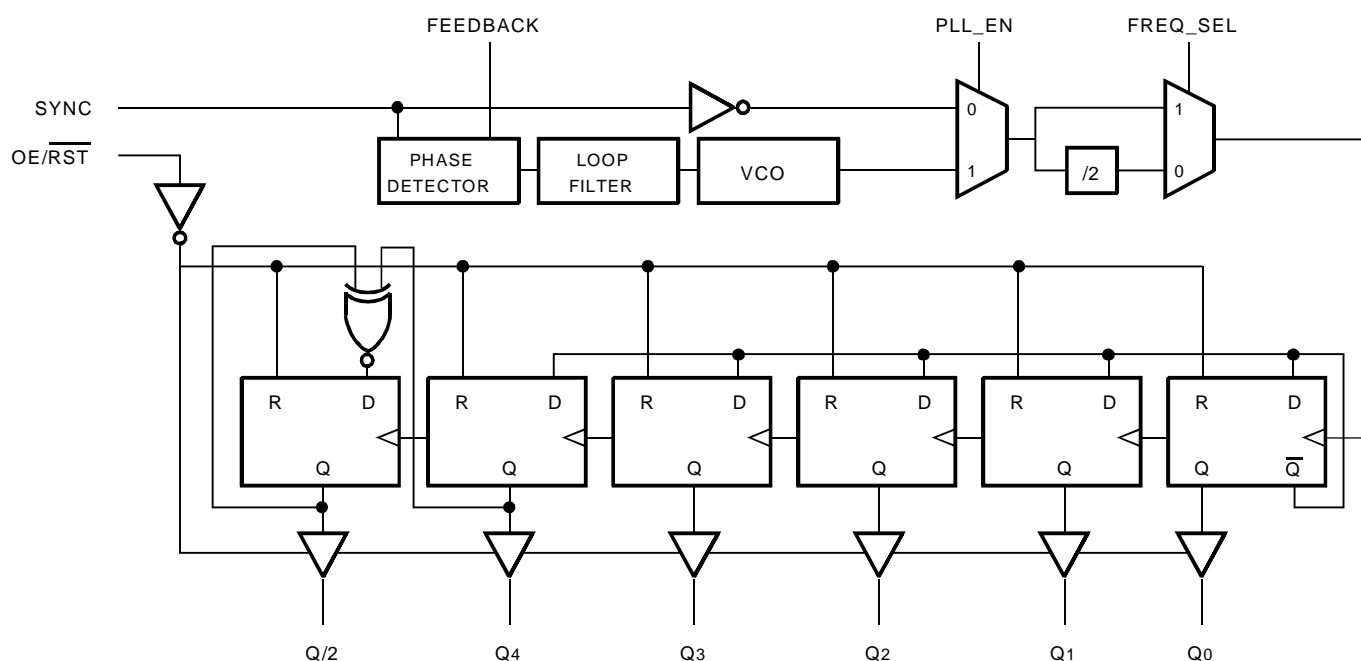
- 5V operation
- Six low noise CMOS level outputs
- Q outputs, Q/2 output
- <500ps output skew, Q0-Q4
- Outputs 3-state and reset while OE/ $\overline{\text{RST}}$  low
- PLL disable feature for low frequency testing
- Internal loop filter RC network
- Internal VCO/2 option
- Balanced drive outputs  $\pm 36\text{mA}$
- ESD >2000V
- 80MHz maximum frequency
- Available in QSOP package

### DESCRIPTION:

The QS5931 Clock Driver uses an internal phase locked loop (PLL) to lock low skew outputs to a reference clock input. Six outputs are available: Q0-Q4, Q/2. Careful layout and design ensure < 500ps skew between the Q0-Q4, and Q/2 outputs. The QS5931 includes an internal RC filter which provides excellent jitter characteristics and eliminates the need for external components. Various combinations of feedback and a divide-by-2 in the VCO path allow applications to be customized for linear VCO operation over a wide range of input SYNC frequencies. The PLL can also be disabled by the PLL\_EN signal to allow low frequency or DC testing. The QS5931 is designed for use in cost sensitive high-performance computing systems, workstations, multi-board computers, networking hardware, and mainframe systems. Several can be used in parallel or scattered throughout a system for guaranteed low skew, system-wide clock distribution networks. In the QSOP package, the QS5931 clock driver represents the best value in small form factor, high-performance clock management products.

For more information on PLL clock driver products, see Application Note AN-227.

### FUNCTIONAL BLOCK DIAGRAM

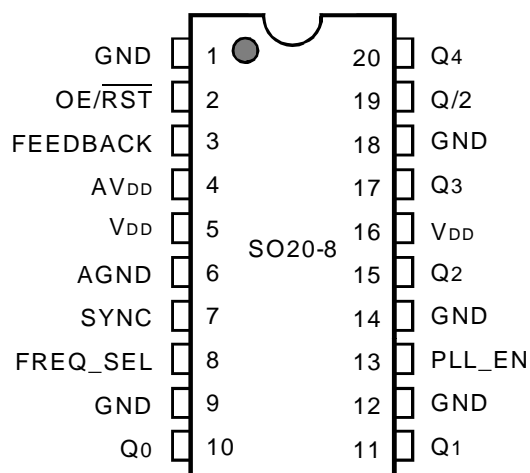


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**INDUSTRIAL TEMPERATURE RANGE**

**JANUARY 2002**

## PIN CONFIGURATION



QSOP  
TOP VIEW

## ABSOLUTE MAXIMUM RATINGS<sup>(1)</sup>

| Symbol   | Description                           | Max          | Unit |
|----------|---------------------------------------|--------------|------|
| AVDD/VDD | Supply Voltage to Ground              | -0.5 to +7   | V    |
|          | DC Input Voltage VIN                  | -0.5 to +5.5 | V    |
|          | Maximum Power Dissipation (TA = 85°C) | 0.5          | W    |
| TSTG     | Storage Temperature Range             | -65 to +150  | °C   |

### NOTE:

- Stresses beyond those listed under ABSOLUTE MAXIMUM RATINGS may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.

## CAPACITANCE (TA = +25°C, f = 1MHz, VIN = 0V)

| Pins | Typ. | Max. | Unit |
|------|------|------|------|
| CIN  | 3    | 4    | pF   |
| COUT | 4    | 5    | pF   |

## PIN DESCRIPTION

| Pin Name | I/O | Description   |
|----------|-----|---|
| SYNC     | I   | Reference clock input   |
| FREQ_SEL | I   | VCO frequency select. For choosing optimal VCO operating frequency depending on input frequency. HIGH is for higher frequencies, LOW is for lower frequencies.  |
| FEEDBACK | I   | PLL feedback input which is connected to either a Q or a Q/2 output. External feedback provides flexibility for different output frequency relationships. See the Frequency Selection Table for more information. |
| Q0-Q4    | O   | Clock outputs   |
| Q/2      | O   | Clock output. Matched in phase, but frequency is half the Q frequency.  |
| OE/RST   | I   | Output enable/asynchronous reset. Resets all output registers. When 0, all outputs are held in a tri-stated condition. When 1, outputs are enabled.   |
| PLL_EN   | I   | PLL enable. Enables and disables the PLL. Allows the SYNC input to be single-stepped for system debug.  |
| VDD      | —   | Power supply for output buffers   |
| AVDD     | —   | Power supply for phase lock loop and other internal circuitries   |
| GND      | —   | Ground supply for output buffers  |
| AGND     | —   | Ground supply for phase lock loop and other internal circuitries  |

## OUTPUT FREQUENCY SPECIFICATIONS

Industrial: TA = -40°C to +85°C, AVDD/VDD = 5.0V ± 10%

| Symbol   | Description             | -50 | -66 | -80 | Units |
|----------|-------------------------|-----|-----|-----|-------|
| FMAX_Q   | Max Frequency, Q0 - Q4, | 50  | 66  | 80  | MHz   |
| FMAX_Q/2 | Max Frequency, Q/2      | 25  | 33  | 40  | MHz   |
| FMIN_Q   | Min Frequency, Q0 - Q4  | 10  | 10  | 10  | MHz   |
| FMIN_Q/2 | Min Frequency, Q/2      | 5   | 5   | 5   | MHz   |

## FREQUENCY SELECTION TABLE

| FREQ_SEL | Output Used for Feedback | SYNC (MHz)<br>(allowable range) <sup>(1)</sup> |                        | Output Frequency Relationships |          |
|----------|--------------------------|--|------------------------|--------------------------------|----------|
|          |                          | Min.   | Max                    | Q/2                            | Q0 - Q4  |
| HIGH     | Q/2                      | F <sub>MIN_Q/2</sub>                           | F <sub>MAX_Q/2</sub>   | SYNC                           | SYNC X 2 |
| HIGH     | Q0 - Q4                  | F <sub>MIN_Q</sub>                             | F <sub>MAX_Q</sub>     | SYNC / 2                       | SYNC     |
| LOW      | Q/2                      | F <sub>MIN_Q/2/2</sub>                         | F <sub>MAX_Q/2/2</sub> | SYNC                           | SYNC X 2 |
| LOW      | Q0 - Q4                  | F <sub>MIN_Q /2</sub>                          | F <sub>MAX_Q /2</sub>  | SYNC / 2                       | SYNC     |

**NOTE:**  
1. Operation in the specified SYNC frequency range guarantees that the VCO will operate in its optimal range of 20MHz to F<sub>MAX\_Q</sub> x2. Operation with Sync inputs outside specified frequency ranges may result in out-of-lock outputs. FREQ\_SEL only affects VCO frequency and does not affect output frequencies.

## DC ELECTRICAL CHARACTERISTICS OVER OPERATING RANGE

Following Conditions Apply Unless Otherwise Specified:

Industrial: T<sub>A</sub> = -40°C to +85°C, AV<sub>DD</sub>/V<sub>DD</sub> = 5.0V ± 10%

| Symbol          | Parameter              | Conditions   | Min.                  | Typ. | Max. | Unit |
|-----------------|------------------------|--|-----------------------|------|------|------|
| V <sub>IH</sub> | Input HIGH Voltage     | Guaranteed Logic HIGH Level  | 2                     | —    | —    | V    |
| V <sub>IL</sub> | Input LOW Voltage      | Guaranteed Logic LOW Level   | —                     | —    | 0.8  | V    |
| V <sub>OH</sub> | Output HIGH Voltage    | I <sub>OH</sub> = -24mA  | V <sub>DD</sub> - 0.6 | —    | —    | V    |
|                 |                        | I <sub>OH</sub> = -100μA   | V <sub>DD</sub> - 0.2 | —    | —    |      |
| V <sub>OL</sub> | Output LOW Voltage     | V <sub>DD</sub> = Min., I <sub>OL</sub> = 24mA   | —                     | —    | 0.45 | V    |
|                 |                        | V <sub>DD</sub> = Min., I <sub>OL</sub> = 100μA  | —                     | —    | 0.2  |      |
| V <sub>H</sub>  | Input Hysteresis       | —  | —                     | 100  | —    | mV   |
| I <sub>OZ</sub> | Output Leakage Current | V <sub>OUT</sub> = V <sub>DD</sub> or GND,<br>V <sub>DD</sub> = Max., Outputs Disabled | —                     | —    | 5    | μA   |
| I <sub>IN</sub> | Input Leakage Current  | AV <sub>DD</sub> = Max., V <sub>IN</sub> = AV <sub>DD</sub> or GND                     | —                     | —    | 5    | μA   |

## POWER SUPPLY CHARACTERISTICS

| Symbol           | Parameter                               | Test Conditions  | Typ. | Max. | Unit   |
|------------------|---|--|------|------|--------|
| I <sub>DDQ</sub> | Quiescent Power Supply Current          | V <sub>DD</sub> = Max., OE/ $\overline{\text{RST}}$ = LOW,<br>SYNC = LOW, All outputs unloaded | —    | 1    | mA     |
| ΔI <sub>DD</sub> | Power Supply Current per Input HIGH     | V <sub>DD</sub> = Max., V <sub>IN</sub> = 3V   | 1    | 30   | μA     |
| I <sub>DDO</sub> | Dynamic Power Supply Current per Output | V <sub>DD</sub> = Max., C <sub>L</sub> = 0pF   | 0.2  | 0.3  | μA/MHz |

## INPUT TIMING REQUIREMENTS

| Symbol                          | Description <sup>(1)</sup>                    | Min. | Max.               | Unit |
|---------------------------------|---|------|--------------------|------|
| t <sub>r</sub> , t <sub>f</sub> | Maximum input rise and fall times, 0.8V to 2V | —    | 3                  | ns   |
| F <sub>i</sub>                  | Input Clock Frequency, SYNC <sup>(1)</sup>    | 2.5  | F <sub>MAX_Q</sub> | MHz  |
| t <sub>PWC</sub>                | Input clock pulse, HIGH or LOW <sup>(2)</sup> | 2    | —                  | ns   |
| D <sub>H</sub>                  | Duty Cycle, SYNC <sup>(2)</sup>               | 25   | 75                 | %    |

**NOTES:**  
1. See Output Frequency and Frequency Selection tables for more detail on allowable SYNC input frequencies for different speed grades with different FEEDBACK and FREQ\_SEL combinations.  
2. Where pulse width implied by D<sub>H</sub> is less than tw<sub>PC</sub> limit, tw<sub>PC</sub> limit applies

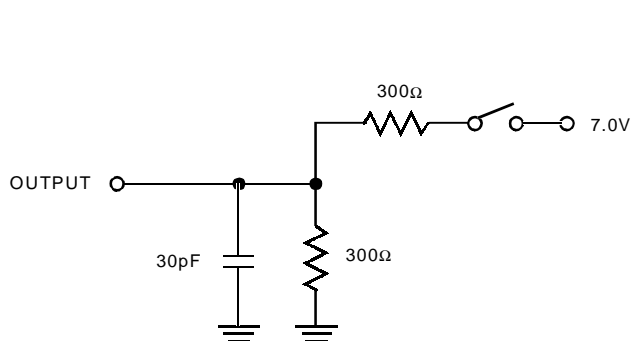
## SWITCHING CHARACTERISTICS OVER OPERATING RANGE

| Symbol                               | Parameter <sup>(1)</sup>   | Min.                     | Max.                     | Unit |
|--------------------------------------|--|--------------------------|--------------------------|------|
| t <sub>SKR</sub>                     | Output Skew Between Rising Edges, Q <sub>0</sub> -Q <sub>4</sub> and Q/2 <sup>(2)</sup>  | —                        | 500                      | ps   |
| t <sub>SKF</sub>                     | Output Skew Between Falling Edges, Q <sub>0</sub> -Q <sub>4</sub> and Q/2 <sup>(2)</sup> | —                        | 500                      | ps   |
| t <sub>PW</sub>                      | Pulse Width, Q <sub>0</sub> -Q <sub>4</sub> , Q/2 outputs, 80MHz                         | T <sub>cy</sub> /2 — 0.4 | T <sub>cy</sub> /2 + 0.4 | ns   |
| t <sub>J</sub>                       | Cycle-to-Cycle Jitter <sup>(4)</sup>   | — 0.15                   | 0.15                     | ns   |
| t <sub>PD</sub>                      | SYNC Input to Feedback Delay <sup>(5)</sup>  | — 500                    | 500                      | ps   |
| t <sub>LOCK</sub>                    | SYNC to Phase Lock   | —                        | 10                       | ms   |
| t <sub>PZH</sub><br>t <sub>PZL</sub> | Output Enable Time, OE/ $\overline{\text{RST}}$ LOW to HIGH <sup>(3)</sup>               | 0                        | 14                       | ns   |
| t <sub>PHZ</sub><br>t <sub>PLZ</sub> | Output Disable Time, OE/ $\overline{\text{RST}}$ HIGH to LOW <sup>(3)</sup>              | 0                        | 14                       | ns   |
| t <sub>R</sub> , t <sub>F</sub>      | Output Rise/Fall Times, 0.2V <sub>DD</sub> to 0.8V <sub>DD</sub>                         | 0.3                      | 2.5                      | ns   |

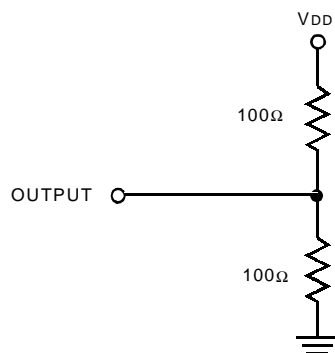
### NOTES:

1. See Test Loads and Waveforms for test load and termination.
2. Skew specifications apply under identical environments (loading, temperature, V<sub>DD</sub>, device speed grade).
3. Measured in open loop mode PLL\_EN = 0.
4. Jitter is characterized with Q output at 20MHz. See Frequency Selection Table for information on proper FREQ\_SEL level for specified input frequencies.
5. t<sub>PD</sub> measured at device inputs at 1.5V, Q output at 80MHz.

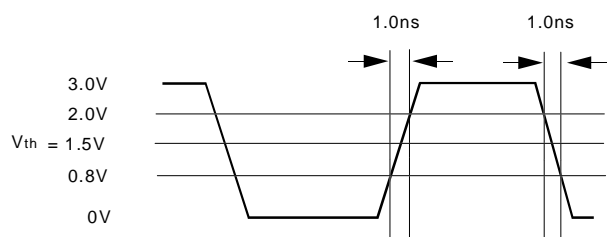
## AC TEST LOADS AND WAVEFORMS



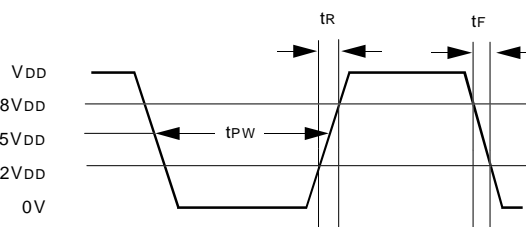
*Test Circuit 1*



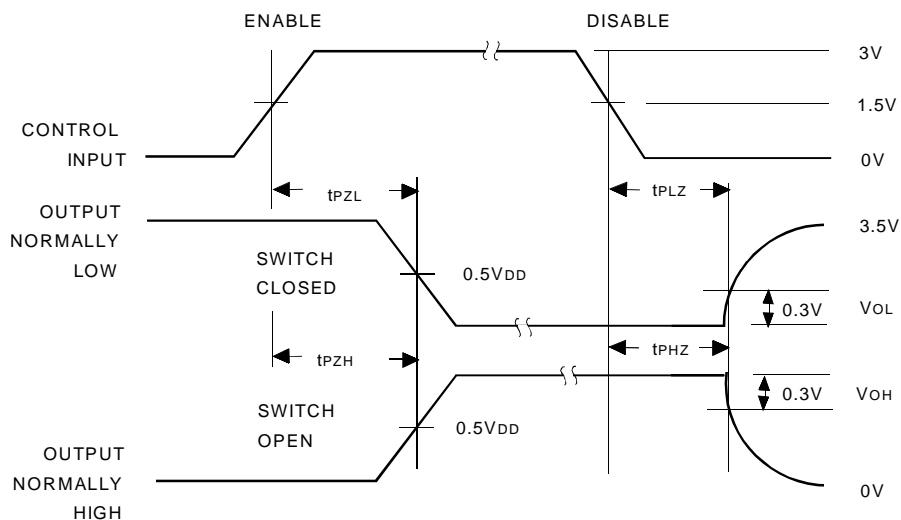
*Test Circuit 2*



*CMOS Input Test Waveform*



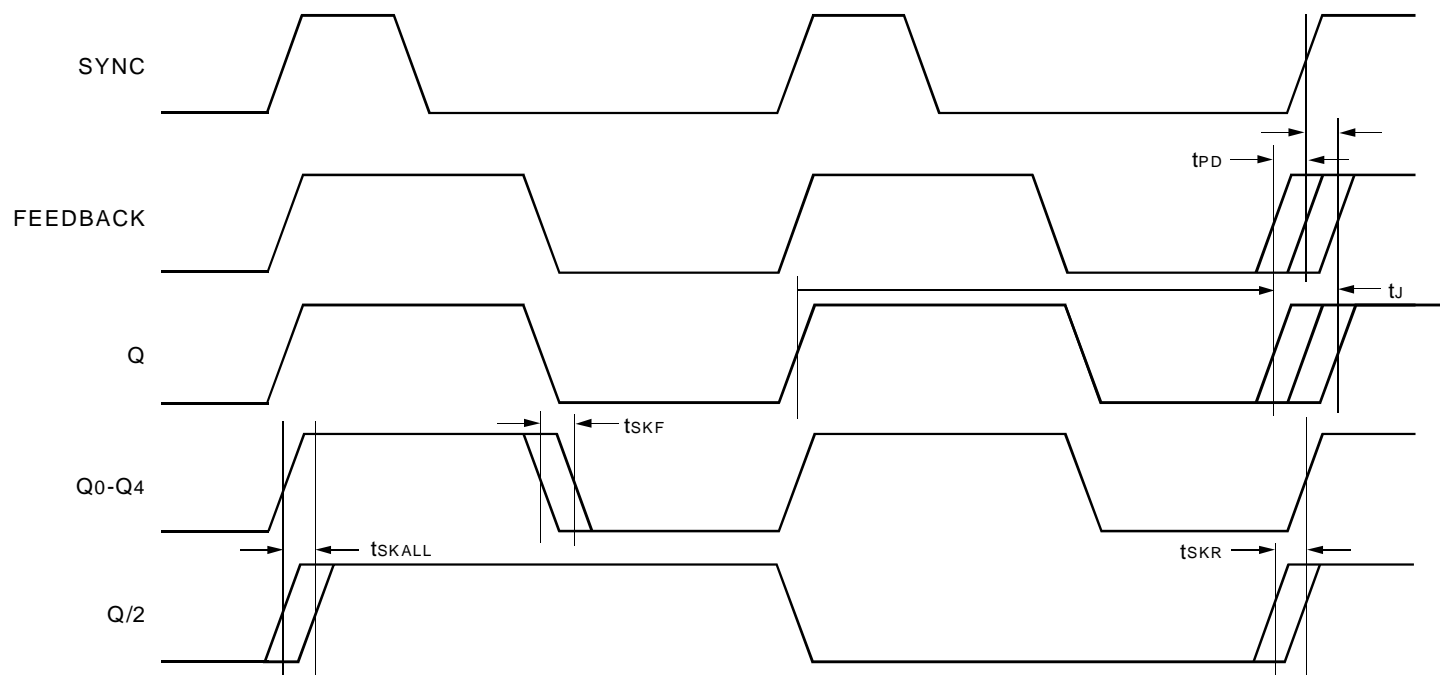
*CMOS Output Waveform*



*Enable and Disable Times*

TEST CIRCUIT 1 is used for output enable/disable parameters.  
TEST CIRCUIT 2 is used for all other timing parameters.

## AC TIMING DIAGRAM



### NOTES:

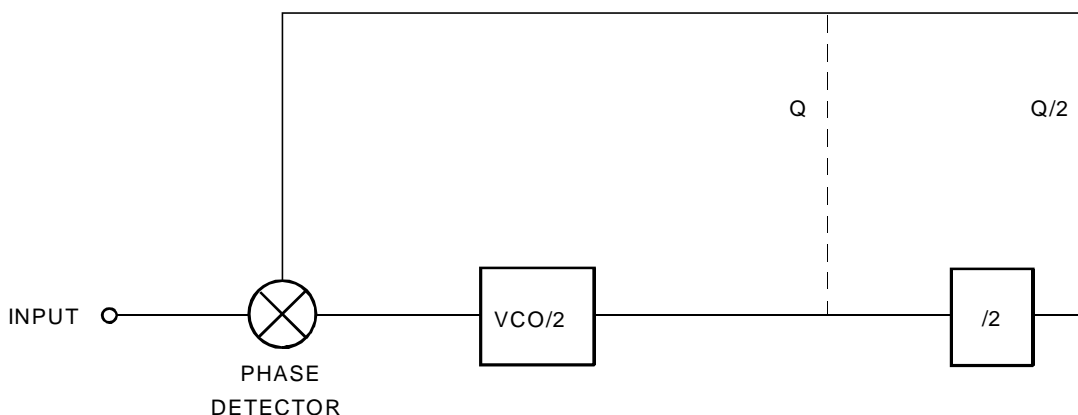
1. AC Timing Diagram applies to Q output connected to FEEDBACK and  $\overline{PE} = GND$ . For  $\overline{PE} = V_{DD}$ , the negative edge of FEEDBACK aligns with the negative edge of SYNC input, and the negative edges of the multiplied and divided outputs align with the negative edge of SYNC.
2. All parameters are measured at 0.5V<sub>DD</sub>.

## PLL OPERATION

The Phase Locked Loop (PLL) circuit included in the QS5931 provides for replication of incoming SYNC clock signals. Any manipulation of that signal, such as frequency multiplying, is performed by digital logic following the PLL (see the block diagram). The key advantage of

the PLL circuit is to provide an effective zero propagation delay between the output and input signals. In fact, adding delay circuits in the feedback path, 'propagation delay' can even be negative! A simplified schematic of the QS5931 PLL circuit is shown below:

## SIMPLIFIED DIAGRAM OF QS5931 FEEDBACK



The phase difference between the output and the input frequencies feeds the VCO which drives the outputs. Whichever output is fed back, it will stabilize at the same frequency as the input. Hence, this is a true negative feedback closed loop system. In most applications, the output will optimally have zero phase shift with respect to the input. In fact, the internal loop filter on the QS5931 typically provides within 150ps of phase shift between input and output.

If the user wishes to vary the phase difference (typically to compensate for backplane delays), this is most easily accomplished by adding delay circuits to the feedback path. The respective output used for feedback will be advanced by the amount of delay in the feedback path. All other outputs will retain their proper relationships to that output.

## ORDERING INFORMATION

| QS          | XXXX | X     | X       |      |  |
|-------------|------|-------|---------|------|--|
| Device Type |      | Speed | Package |      |  |
|             |      |       |         | Q    | Quarter Size Outline Package                               |
|             |      |       |         | -50  | 50 MHz. max. frequency                                     |
|             |      |       |         | -66  | 66 MHz. max. frequency                                     |
|             |      |       |         | -80  | 80 MHz. max. frequency                                     |
|             |      |       |         | 5931 | Low Skew CMOS PLL Clock Driver with Integrated Loop Filter |



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