LOW SKEW CLOCK DRIVER/BUFFER FOR DESKTOP PC WITH FOUR DIMMS

QS5818

FEATURES:

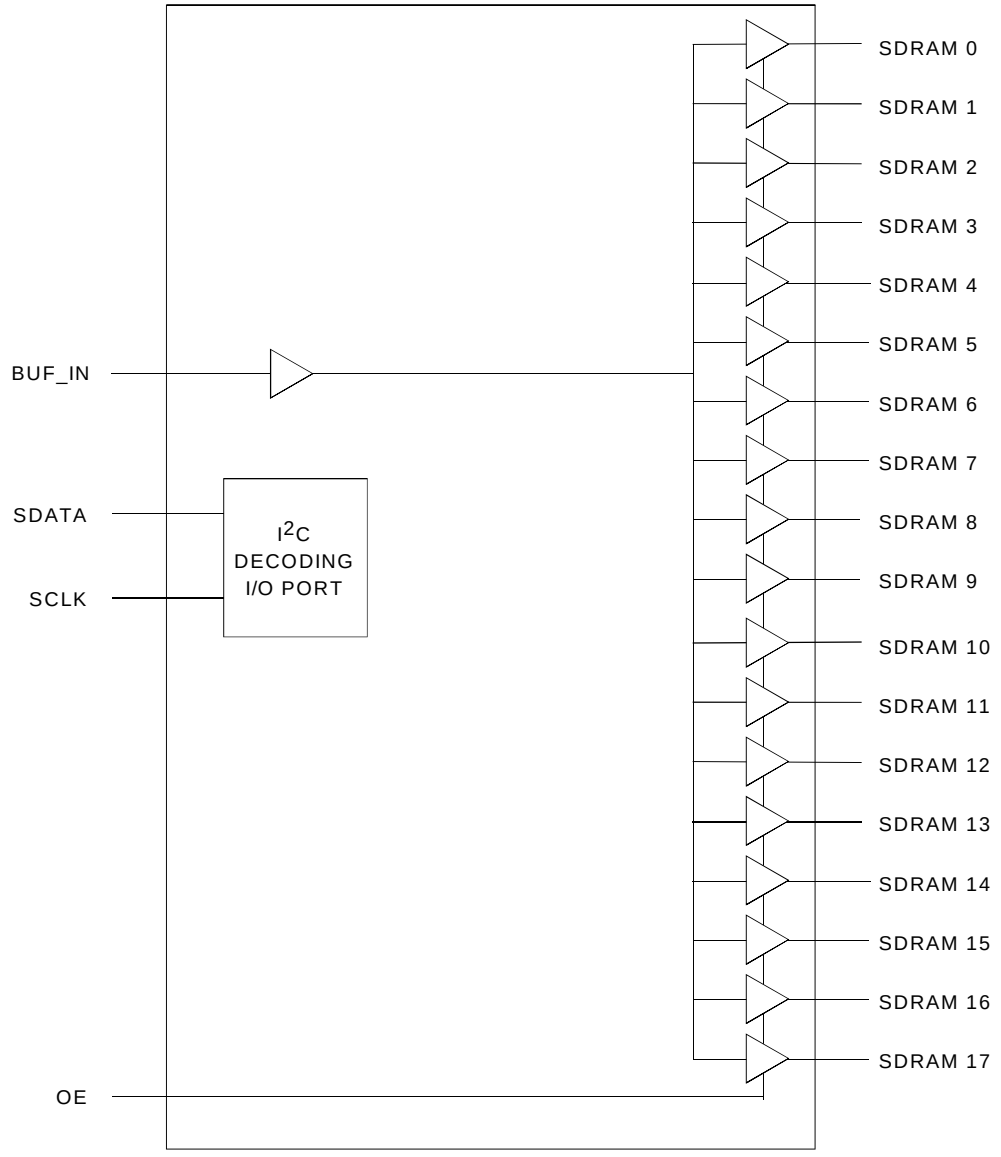
- 1 to 18 output buffer/driver
- Tri-state pin for testing
- I^2C programming capability
- Power Supply Voltage 3.3V ±5%
- Low skew output (<250 ps)
- Multiple V_{DD} and GND for noise reduction
- 48-pin SSOP package

DESCRIPTION:

The QS5818 is a high speed, low noise 1-18 non-inverting buffer designed for SDRAM clock buffer applications. Out of the 18 outputs 16 outputs may be used to drive up to four SDRAM DIMMs, and the remaining two can be used for external feedback to a PLL.

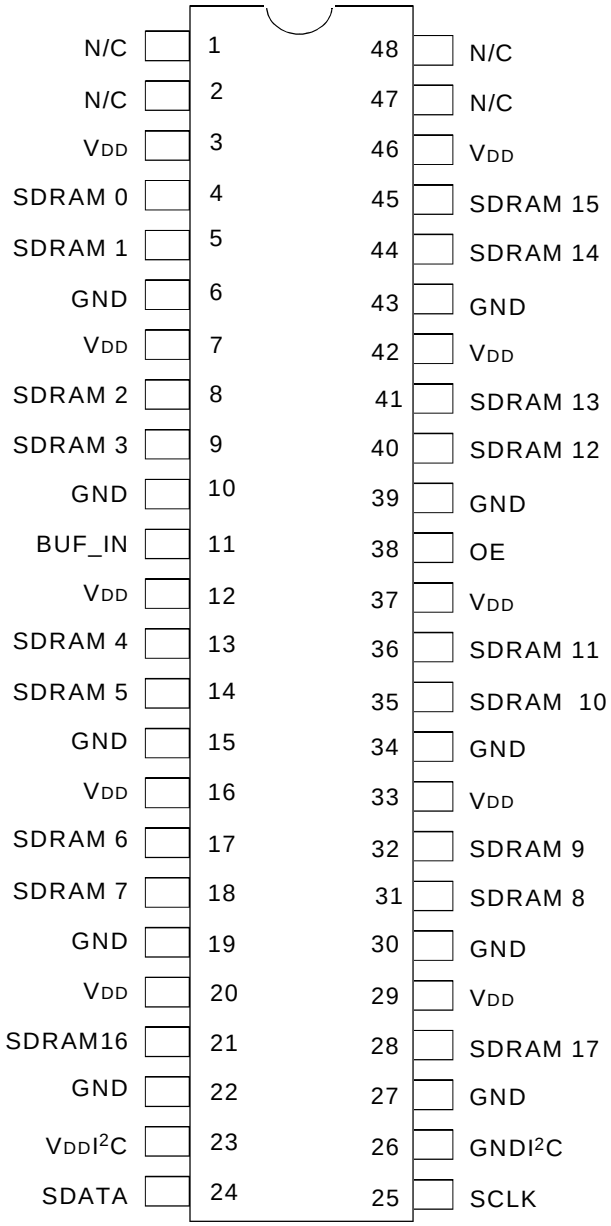
The QS5818 also includes an I^2C interface, which can enable or disable each output clock driver. Turning unused outputs off reduces Electro Magnetic Interference (EMI).

FUNCTIONAL BLOCK DIAGRAM



INDUSTRIAL TEMPERATURE RANGE **APRIL 2000**

PIN CONFIGURATION



SSOP
TOP VIEW

ABSOLUTE MAXIMUM RATING (1)

Symbol	Description	Max.	Unit
V_{DD}	Supply Voltage to Ground	– 0.5 to 4.6V	V
V_{OH}	DC Output Voltage V_{OUT}	– 0.5 to + 4.6V	V
V_{IL}	DC Output Voltage V_{IN}	– 0.5 to + 4.6	V
V_I	DC Input Diode Current with $V_I < 0$	– 20	mA
T_A	Maximum Power Dissipation at T_A = 85°C	600	mW
T_{STG}	T_{STG} Storage Temperature	–65 to 150	°C

NOTE:
1. Stresses greater than those listed under ABSOLUTE MAXIMUM RATINGS may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect reliability.

PIN DESCRIPTION

Pin Name	Description
N/C	Pins are not internally connected.
SDRAM (0:3)	SDRAM Byte 0 Clock Outputs.
SDRAM (4:7)	SDRAM Byte 1 Clock Outputs.
SDRAM (8:11)	SDRAM Byte 2 Clock Outputs.
SDRAM (12:15)	SDRAM Byte 3 Clock Outputs.
SDRAM (16:17)	SDRAM Clock Outputs useable for feedback.
BUF_IN	Input for Buffers.
OE	Tri-State Output Enable. Includes internal pull up to V_{DD}. When asserted LOW, clock outputs are high impedance.
SDATA	I^2C Data Pin. Includes internal pull up to V_{DD}.
SCLK	I^2C Clock Pin. Includes internal pull up to V_{DD}.
V_{DD}	3.3V power supply for output buffers.
GND	Ground for output buffers.
GND_{I^2C}	Ground for I^2C circuitry.
V_{DDI^2C}	3.3V Power Supply for I^2C circuitry.

DC ELECTRICAL CHARACTERISTICS OVER OPERATING RANGE

Following Conditions Apply Unless Otherwise Specified:

Operating Condition: T_A = – 40°C to +85°C

Symbol	Parameter	Test Conditions	Min.	Typ.(1)	Max.	Unit
V_{IH}	Input HIGH Voltage Level	For all Inputs	2	—	—	V
V_{IL}	Input LOW Voltage Level	For all inputs except I^2C inputs	—	—	0.8	V
		I^2C Inputs (SDATA and SCLK)	—	—	0.7	
I_{IH}	Input High Input Current	$V_{IN} = V_{DD}$	– 5	—	5	µA
I_{IL}	Input Low Current	V_{IN} = 0V; BUF_IN	– 5	—	5	µA
		V_{IN} = 0V; OE, SDATA, SCLK	– 100	—	0	
I_{DD}	Supply Current	C_L = 0pF; f_{IN}@66.66MHz(1)	—	50	70	mA
		C_L = 0pF; f_{IN}@100MHz(1)	—	75	105	
		C_L = 30pF; f_{IN}@66.66MHz(1)	—	160	180	
		C_L = 30pF; f_{IN}@100MHz(1)	—	240	270	
		BUF_IN = GND or V_{DD}, all other inputs at V_{DD}	—	—	500	
V_{OH}	Output High Voltage	SDRAM (0:17) I_{OH} = –36mA	2.4	—	—	V
V_{OL}	Output Low Voltage	SDRAM (0:17) I_{OL} = 25mA	—	—	0.4	V
V_{OLI^2C}	Output Low Voltage	SDATA I_{OLI^2C} = 3mA	—	—	0.4	V

NOTE:

1. Typical values are at V_{CC} = 3.3V, +25°C ambient.

OPERATING CHARACTERISTICS , T_A = 25ºC

Symbol	Parameter	Min.	Typ.	Max.	Unit
V_{CC}	Power Supply Voltage	3.135	3.3	3.465	V
T_A	Operating Temperature	-40	25	85	°C
C_L	Load Capacitance	—	—	30	pF
C_{IN}	Input Capacitance(1)	—	—	15	pF

AC ELECTRICAL CHARACTERISTICS OVER OPERATING RANGE

Symbol	Parameter	Test Conditions	Min.	Typ.(1)	Max.	Unit
tR	Rise Time(1)	0.4V to 2.4V; C_L = 30pF	—	—	2.2	ns
tF	Fall Time(1)	2.4V to 0.4V; C_L = 30pF	—	—	2.4	ns
Dt	Duty Cycle(1)	V_T = 1.5V; C_L = 30pF; with 50% Input Clock	45	50	55	%
tSK	Skew (output-output)(1)	V_T = 1.5V; C_L = 30pF for all outputs	—	—	250	ps
tPHL or tPLH	Propagation Delay	V_T = 1.5V	—	—	6	ns
tPROP EN	Enable Delay	V_T = 1.5V	—	—	8	ns
tPROP DIS	Disable Delay	V_T = 1.5V	—	—	8	ns

NOTE:
1. Guaranteed by design, not subject to 100% production testing.

I²C SERIAL INTERFACE CONTROL

The I²C interface permits individual enable/disable of each clock output: any unused outputs may be disabled to reduce the EMI. The QS5818 is a slave receiver device. It can read back the data stored in latches for verification.

The data transfer rate supported by the I²C interface is 100K bits/ sec. Data is transferred in bytes (with the addition of start, stop, acknowledge bits) in sequential order from the lowest to highest byte with the ability to stop after any complete byte has been transferred. The first two bytes transferred must be a Command Code followed by a Byte Count. Both of these bytes are ignored by the device.

The I²C address of the QS5818 is :

A7	A6	A5	A4	A3	A2	A1
1	1	0	1	0	0	1

Address A0 is the read/write bit and is set to 0 for writes and 1for reads. During read back, the first byte read is a Byte Count representing the number of bytes following (fixed at 3).

SERIAL CONFIGURATION COMMAND BITMAPS

Byte 0: SDRAM Active/Inactive Register (1 = Enable, 0 = Disable, Outputs held low), Default = Enable

Bit	Pin#	Description
Bit 7	18	SDRAM 7 (Active/Inactive)
Bit 6	17	SDRAM 6 (Active/Inactive)
Bit 5	14	SDRAM 5 (Active/Inactive)
Bit 4	13	SDRAM 4 (Active/Inactive)
Bit 3	9	SDRAM 3 (Active/Inactive)
Bit 2	8	SDRAM 2 (Active/Inactive)
Bit 1	5	SDRAM 1 (Active/Inactive)
Bit 0	4	SDRAM 0 (Active/Inactive)

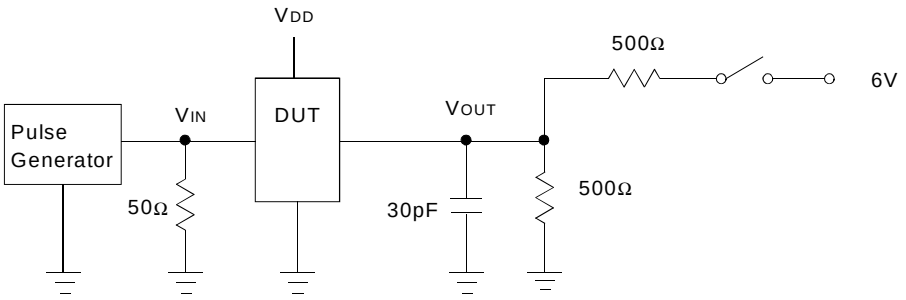
Byte 1: SDRAM Active/Inactive Register (1 = Enable, 0 = Disable, Outputs held low), Default = Enable

Bit	Pin#	Description
Bit 7	45	SDRAM 15 (Active/Inactive)
Bit 6	44	SDRAM 14 (Active/Inactive)
Bit 5	41	SDRAM 13 (Active/Inactive)
Bit 4	40	SDRAM 12 (Active/Inactive)
Bit 3	36	SDRAM 11 (Active/Inactive)
Bit 2	35	SDRAM 10 (Active/Inactive)
Bit 1	32	SDRAM 9 (Active/Inactive)
Bit 0	31	SDRAM 8 (Active/Inactive)

Byte 2: SDRAM Active/Inactive Register (1 = Enable, 0 = Disable, Outputs held low), Default = Enable

Bit	Pin#	Description
Bit 7	28	SDRAM 17 (Active/Inactive)
Bit 6	21	SDRAM 16 (Active/Inactive)
Bit 5	—	Reserved, 1 at power up, set to 0
Bit 4	—	Reserved, 1 at power up, set to 0
Bit 3	—	Reserved, 1 at power up, set to 0
Bit 2	—	Reserved, 1 at power up, set to 0
Bit 1	—	Reserved, 1 at power up, set to 0
Bit 0	—	Reserved, 1 at power up, set to 0

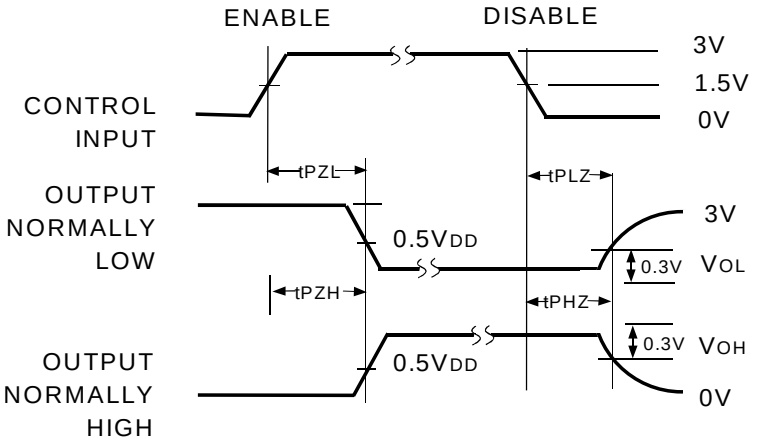
TEST CIRCUIT



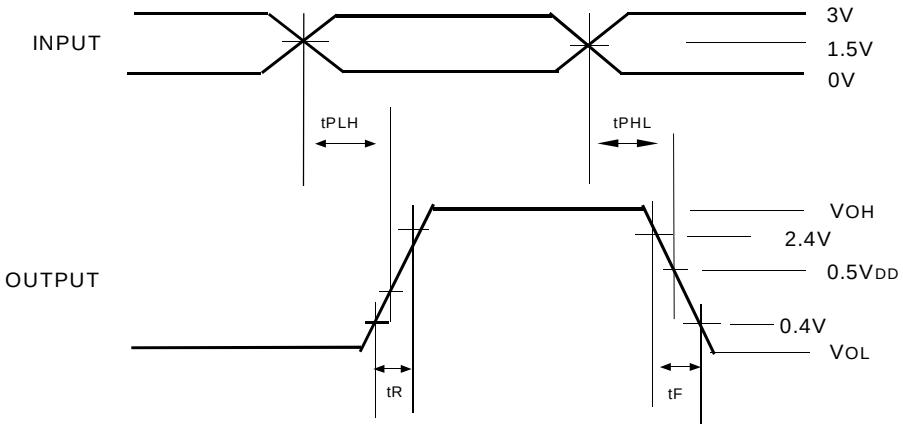
Parameter Tested	Switch Position
tPLZ, tPZL	Closed
All Others	Open

AC TIMING DIAGRAM

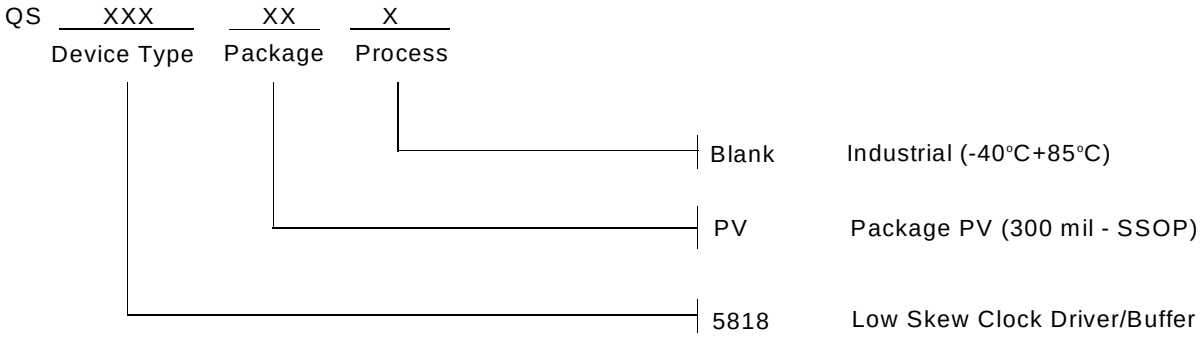
ENABLE AND DISABLE TIMES



PROPAGATION DELAY



ORDERING INFORMATION



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