FAST CMOS BUFFER/CLOCK DRIVER

IDT74FCT810BT/CT

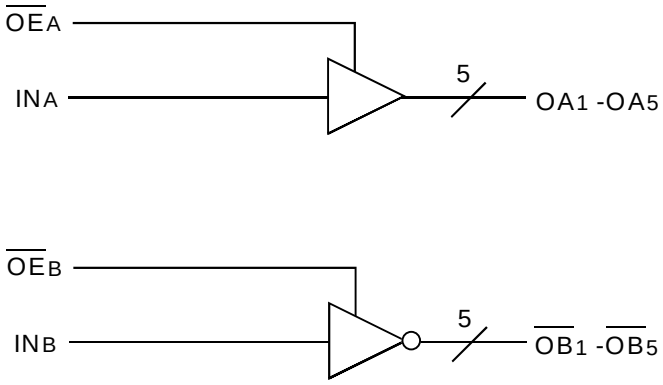
FEATURES:

- 0.5 MICRON CMOS technology
- Guaranteed low skew < 600ps (max.)
- Very low duty cycle distortion < 700ps (max.)
- Low CMOS power levels
- TTL compatible inputs and outputs
- TTL level output voltage swings
- High drive: –32mA I_{OH}, 48mA I_{OL}
- Two independent output banks with 3-state control
  - One 1:5 Inverting bank
  - One 1:5 Non-Inverting bank
- ESD > 2000V per MIL-STD-883, Method 3015; > 200V using machine model (C = 200pF, R = 0)
- Available in DIP, SOIC, SSOP, QSOP packages

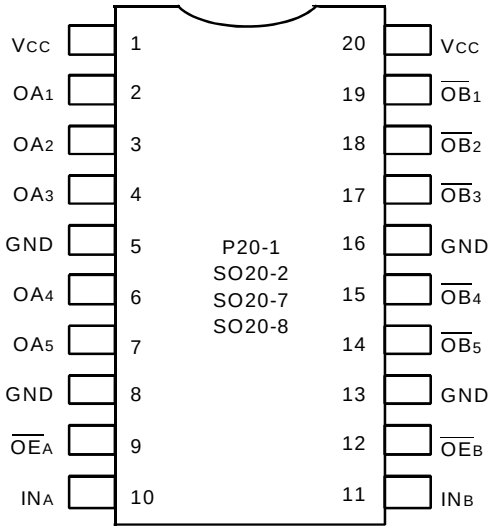
DESCRIPTION:

The 74FCT810BT/CT is a dual bank inverting/ non-inverting clock driver built using advanced dual metal CMOS technology. It consists of two banks of drivers, one inverting and one non-inverting. Each bank drives five output buffers from a standard TTL-compatible input. The FCT810BT/CT have low output skew, pulse skew and package skew. Inputs are designed with hysteresis circuitry for improved noise immunity. The outputs are designed with TTL output levels and controlled edge rates to reduce signal noise. The part has multiple grounds, minimizing the effects of ground inductance.

Functional Block Diagram



PIN CONFIGURATION



DIP/ SOIC/ SSOP/ QSOP
TOP VIEW

ABSOLUTE MAXIMUM RATINGS(1)

Symbol	Description	Max	Unit
V_{TERM}	Terminal Voltage with Respect to GND	–0.5 to +7.0	V
T_{STG}	Storage Temperature	–65 to +150	°C
I_{OUT}	DC Output Current	–60 to +120	mA

NOTE:
1. Stresses greater than those listed under ABSOLUTE MAXIMUM RATINGS may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect reliability. No terminal voltage may exceed Vcc by +0.5V unless otherwise noted.

PIN DESCRIPTION

Pin Names	Description
$\overline{OE}_A$, $\overline{OE}_B$	3-State Output Enable Inputs (Active LOW)
IN_A, IN_B	Clock Inputs
OA_n, $\overline{OB}_n$	Clock Outputs

CAPACITANCE (T_A = +25°C, f = 1.0MHz)

Symbol	Parameter(1)	Conditions	Typ.	Max.	Unit
C_{IN}	Input Capacitance	V_{IN} = 0V	4.5	6.0	pF
C_{OUT}	Output Capacitance	V_{OUT} = 0V	5.5	8.0	pF

NOTE:
1. This parameter is measured at characterization but not tested.

DC ELECTRICAL CHARACTERISTICS OVER OPERATING RANGE

Following Conditions Apply Unless Otherwise Specified
Commercial: T_A = 0°C to +70°C, V_{CC} = 5.0V ± 5%

Symbol	Parameter	Test Conditions(1)		Min.	Typ.(2)	Max.	Unit
V_{IH}	Input HIGH Level (Input pins)	Guaranteed Logic HIGH Level		2.0	—	—	V
V_{IL}	Input LOW Level	Guaranteed Logic LOW Level		—	—	0.8	V
I_{IH}	Input HIGH Current (Input pins)	V_{CC} = Max.	V_I = 2.7V	—	—	±1	µA
I_{IL}	Input LOW Current (Input pins)	V_{CC} = Max.	V_I = 0.5V	—	—	±1	µA
I_{OZH}	High Impedance Output Current	V_{CC} = Max.	V_O = 2.7V	—	—	±1	µA
I_{OZL}	(3-State Output pins)		V_O = 0.5V	—	—	±1	µA
I_I	Input HIGH Current	V_{CC} = Max., V_I = V_{CC} (Max.)		—	—	±1	µA
V_{IK}	Clamp Diode Voltage	V_{CC} = Min., I_{IN} = –18mA		—	–0.7	–1.2	V
I_{OS}	Short Circuit Current	V_{CC} = Max.(3), V_O = GND		–60	–120	–225	mA
V_{OH}	Output HIGH Voltage	V_{CC} = Min.	I_{OH} = –15mA	2.4	3.3	—	V
		V_{IN} = V_{IH} or V_{IL}	I_{OH} = –32mA(4)	2.0	3.0	—	
V_{OL}	Output LOW Voltage	V_{CC} = Min. V_{IN} = V_{IH} or V_{IL}	I_{OL} = 48mA	—	0.3	0.55	V
I_{OFF}	Input/Output Power Off Leakage	V_{CC} = 0V, V_{IN} or V_O ≤ 4.5V		—	—	±1	µA
V_H	Input Hysteresis for all inputs	—		—	150	—	mV
I_{CCL} I_{CCH} I_{CCZ}	Quiescent Power Supply Current	V_{CC} = Max. V_{IN} = GND or V_{CC}		—	5.0	500	µA

NOTES:
1. For conditions shown as Max. or Min., use appropriate value specified under Electrical Characteristics for the applicable device type.
2. Typical values are at V_{CC} = 5.0V, +25°C ambient.
3. Not more than one output should be tested at one time. Duration of the test should not exceed one second.
4. Duration of the condition can not exceed one second.

POWER SUPPLY CHARACTERISTICS

Symbol	Parameter	Test Conditions[1]		Min.	Typ.[2]	Max.	Unit
ΔI_{CC}	Quiescent Power Supply Current TTL Inputs HIGH	V_{CC} = Max. V_{IN} = 3.4V[3]		—	0.5	2.0	mA
I_{CCD}	Dynamic Power Supply Current[4]	V_{CC} = Max. Outputs Open $\overline{OE}_A$ = $\overline{OE}_B$ = GND 50% Duty Cycle	V_{IN} = V_{CC} V_{IN} = GND	—	60	100	µA/ MHz/bit
I_C	Total Power Supply Current[6]	V_{CC} = Max. Outputs Open fo= 25MHz 50% Duty Cycle $\overline{OE}_A$ = GND, $\overline{OE}_B$ =V_{CC}	V_{IN} = V_{CC} V_{IN} = GND V_{IN} = 3.4V V_{IN} = GND	— —	7.5 7.8	13 14.0	mA
		V_{CC} = Max. Outputs Open fo = 50MHz 50% Duty Cycle $\overline{OE}_A$ = $\overline{OE}_B$ = GND	V_{IN} = V_{CC} V_{IN} = GND V_{IN} = 3.4V V_{IN} = GND	— —	30.0 30.5	50.5[5] 52.5[5]	

NOTES:

1. For conditions shown as Max. or Min., use appropriate value specified under Electrical Characteristics for the applicable device type.
2. Typical values are at V_{CC} = 5.0V, +25°C ambient.
3. Per TTL driven input; (V_{IN} = 3.4V); all other inputs at V_{CC} or GND.
4. This parameter is not directly testable, but is derived for use in Total Power Supply Calculations.
5. Values for these conditions are examples of the I_{CC} formula. These limits are guaranteed but not tested.
6. $I_C = I_{QUIESCENT} + I_{INPUTS} + I_{DYNAMIC}$
   $I_C = I_{CC} + \Delta I_{CC} D_H N_T + I_{CCD} (f_O N_O)$
   I_{CC} = Quiescent Current (I_{CCL}, I_{CCH} and I_{CCZ})
   ΔI_{CC} = Power Supply Current for a TTL High Input (V_{IN} = 3.4V)
   D_H = Duty Cycle for TTL Inputs High
   N_T = Number of TTL Inputs at D_H
   I_{CCD} = Dynamic Current Caused by an Input Transition Pair (HLH or LHL)
   f_O= Output Frequency
   N_O= Number of Outputs at f_O
   All currents are in milliamps and all frequencies are in megahertz.

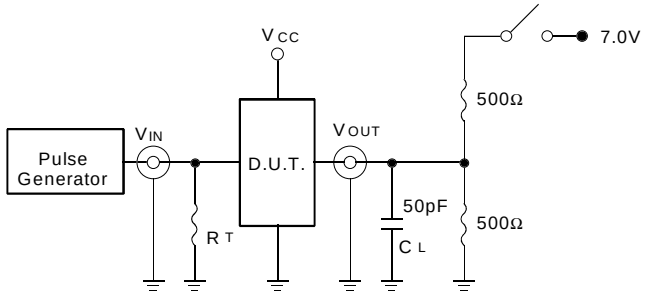
SWITCHING CHARACTERISTICS OVER OPERATING RANGE[3,4]

Symbol	Parameter	Condition[1]	FCT810BT		FCT810CT		Unit
			Min.[2]	Max.	Min.[2]	Max.	
t_{PLH} t_{PHL}	Propagation Delay IN_A to OA_n, IN_B to $\overline{OB}_n$	C_L = 50pF R_L = 500Ω	1.5	4.5	1.5	4.3	ns
t_R	Output Rise Time		—	1.5	—	1.5	ns
t_F	Output Fall Time		—	1.5	—	1.5	ns
$t_{SK1}(o)$	Output skew (same bank): skew between outputs of same bank and same package (same transition)		—	0.5	—	0.3	ns
$t_{SK2}(o)$	Output skew (all banks): skew between outputs of all banks of same package (inputs tied together)		—	0.7	—	0.6	ns
$t_{SK}(p)$	Pulse skew: skew between opposite transitions of same output $\lvert(t_{PHL}-t_{PLH})\rvert$		—	0.7	—	0.7	ns
$t_{SK}(t)$	Package skew: skew between outputs of different packages at same power supply voltage, temperature, package type and speed grade		—	1.2	—	1.0	ns
t_{PZL} t_{PZH}	Output Enable Time $\overline{OE}_A$ to OA_n, $\overline{OE}_B$ to $\overline{OB}_n$		1.5	6.0	1.5	5.0	ns
t_{PLZ} t_{PHZ}	Output Disable Time $\overline{OE}_A$ to OA_n, $\overline{OE}_B$ to $\overline{OB}_n$		1.5	6.0	1.5	5.0	ns

NOTES:
1. See test circuits and waveforms.
2. Minimum limits are guaranteed but not tested on Propagation Delays.
3. t_{PLH}, t_{PHL}, $t_{SK}(t)$ are production tested. All other parameters guaranteed but not production tested.
4. Propagation delay range indicated by Min. and Max. limit is due to V_{CC}, operating temperature and process parameters. These propagation delay limits do not imply skew.

TEST CIRCUITS AND WAVEFORMS

TEST CIRCUIT FOR ALL OUTPUTS



ENABLE AND DISABLE TIME SWITCH POSITION

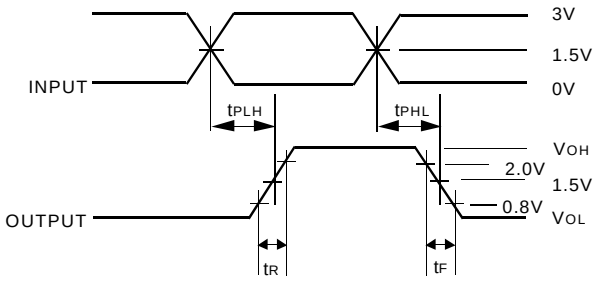
Test	Switch
Disable LOW Enable LOW	Closed
Disable HIGH Enable HIGH	Open

DEFINITIONS:

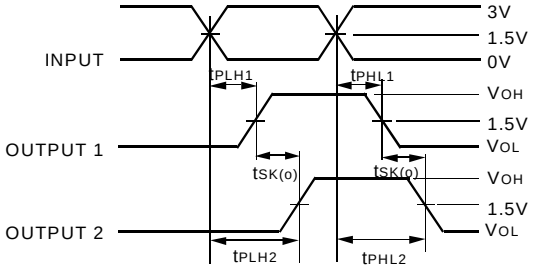
C_L = Load capacitance: includes jig and probe capacitance.

R_T = Termination resistance: should be equal to Z_{OUT} of the Pulse Generator.

PACKAGE DELAY

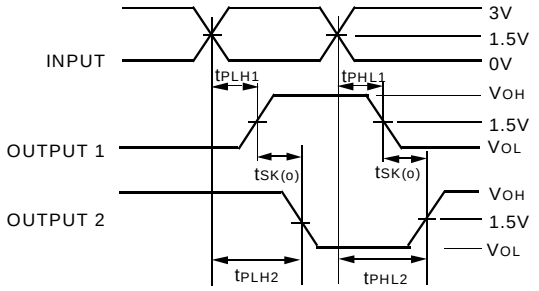


OUTPUT SKEW (SAME BANK) - $t_{SK1}(o)$



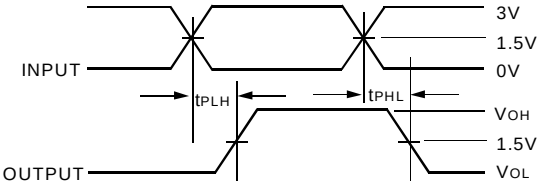
$t_{SK(o)} = |t_{PLH2} - t_{PLH1}|$ or $|t_{PHL2} - t_{PHL1}|$

OUTPUT SKEW (ALL BANKS) - $t_{SK2}(o)$



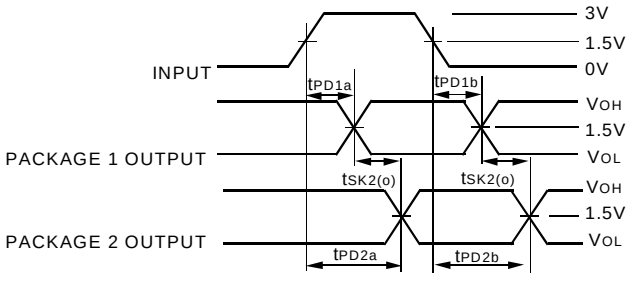
$t_{SK(o)} = |t_{PLH2} - t_{PLH1}|$ or $|t_{PHL2} - t_{PHL1}|$

PULSE SKEW - $t_{SK}(p)$



$t_{SK(p)} = |t_{PHL} - t_{PLH}|$

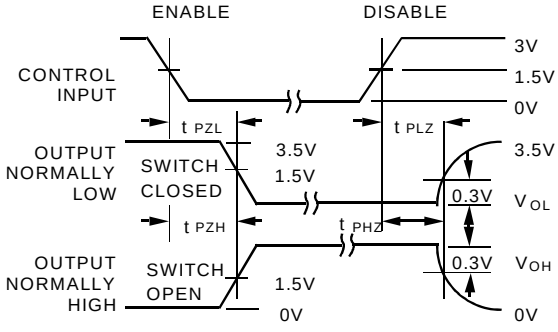
PACKAGE SKEW - $t_{SK}(t)$



$t_{SK(t)} = |t_{PD2a} - t_{PD1a}|$ or $|t_{PD2b} - t_{PD1b}|$

Package 1 and Package 2 are same device type and speed grade

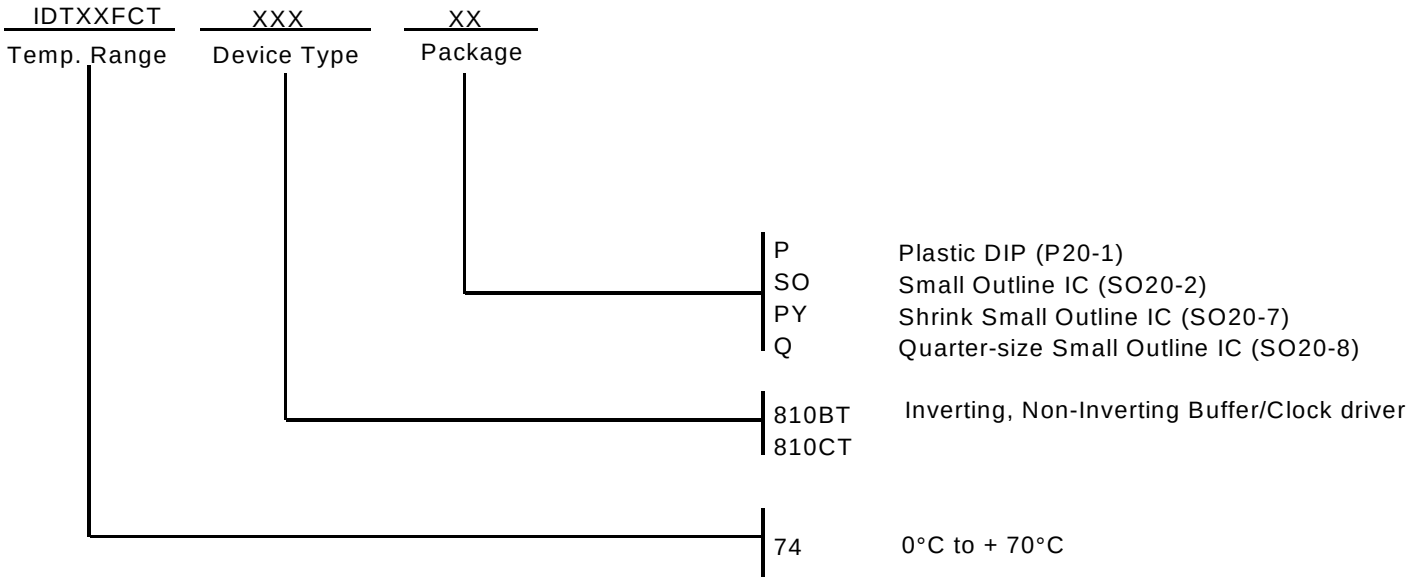
ENABLE AND DISABLE TIMES



NOTES:

1. Diagram shown for input Control Enable-LOW and input Control Disable-HIGH
2. Pulse Generator for All Pulses: $f \leq 1.0MHz$; $t_F \leq 2.5ns$; $t_R \leq 2.5ns$

ORDERING INFORMATION



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