



## 3.3V PROGRAMMABLE SKEW PLL CLOCK DRIVER TURBOCLOCK™ II JR.

**IDT5V9950**  
**PRELIMINARY**

### FEATURES:

- Ref input is 5V tolerant
- 4 pairs of programmable skew outputs
- Low skew: 185ps same pair, 250ps all outputs
- Selectable positive or negative edge synchronization:  
Excellent for DSP applications
- Synchronous output enable
- Input frequency: 6MHz to 200MHz
- Output frequency: 6MHz to 200MHz
- 2x, 4x, 1/2, and 1/4 outputs
- 3-level inputs for skew and PLL range control
- PLL bypass for DC testing
- External feedback, internal loop filter
- 12mA balanced drive outputs
- Low Jitter: <100ps cycle-to-cycle
- Available in TQFP package

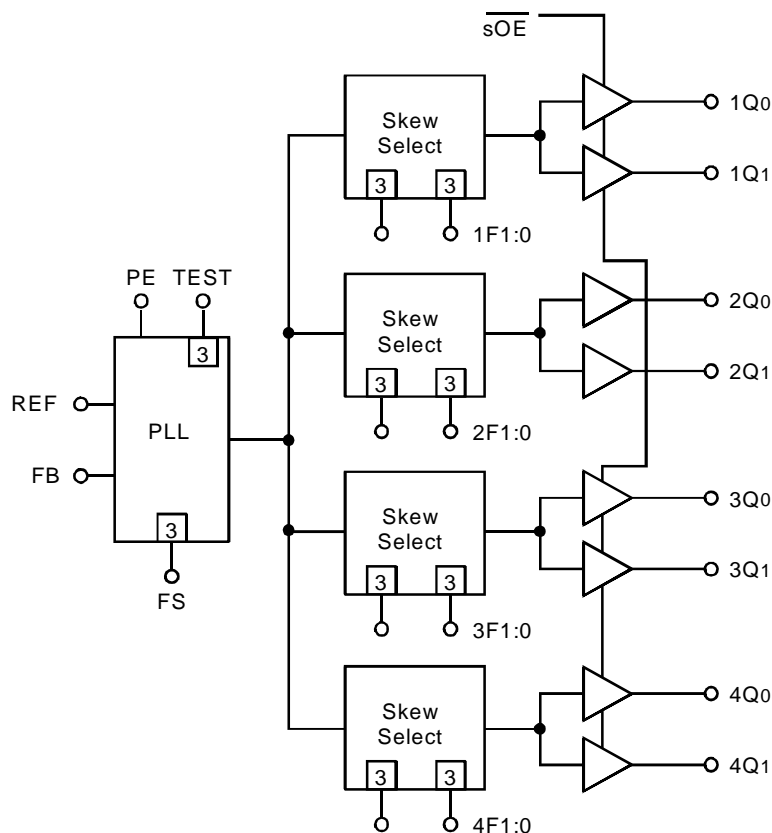
### DESCRIPTION:

The IDT5V9950 is a high fanout 3.3V PLL based clock driver intended for high performance computing and data-communications applications. A key feature of the programmable skew is the ability of outputs to lead or lag the REF input signal. The IDT5V9950 has eight programmable skew outputs in four banks of 2. Skew is controlled by 3-level input signals that may be hard-wired to appropriate HIGH-MID-LOW levels.

When the  $\overline{sOE}$  pin is held low, all the outputs are synchronously enabled. However, if  $\overline{sOE}$  is held high, all the outputs except 2Q0 and 2Q1 are synchronously disabled.

Furthermore, when PE is held high, all the outputs are synchronized with the positive edge of the REF clock input. When PE is held low, all the outputs are synchronized with the negative edge of REF. The IDT5V9950 has LVTTTL outputs with 12mA balanced drive outputs.

### FUNCTIONAL BLOCK DIAGRAM

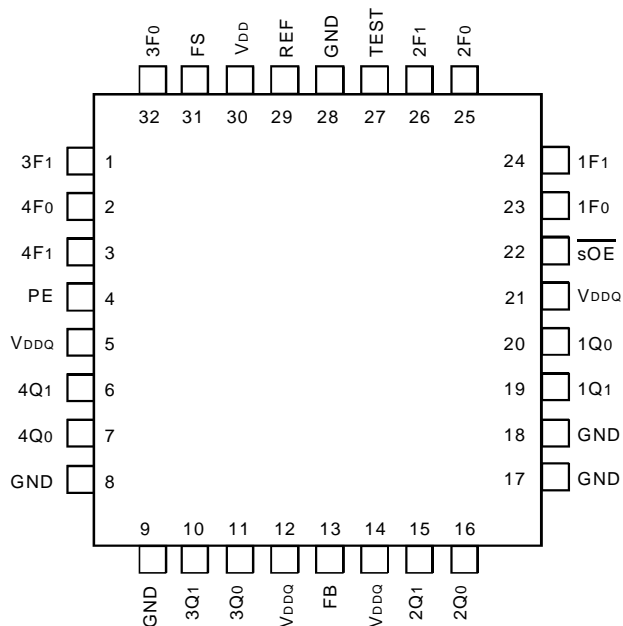


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**INDUSTRIAL TEMPERATURE RANGE**

**FEBRUARY 2002**

## PIN CONFIGURATION



TQFP  
TOP VIEW

## ABSOLUTE MAXIMUM RATINGS<sup>(1)</sup>

Symbol	Description		Max	Unit
V <sub>DDQ</sub> , V <sub>DD</sub>	Supply Voltage to Ground		−0.5 to +4.6	V
V <sub>I</sub>	DC Input Voltage		−0.5 to V <sub>DD</sub> +0.5	V
	REF Input Voltage		−0.5 to +5.5	V
	Maximum Power Dissipation	T <sub>A</sub> = 85°C	0.7	W
		T <sub>A</sub> = 55°C	1.1	
T <sub>STG</sub>	Storage Temperature Range		−65 to +150	°C

### NOTE:

- Stresses beyond those listed under ABSOLUTE MAXIMUM RATINGS may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.

## CAPACITANCE (T<sub>A</sub> = +25°C, f = 1MHz, V<sub>IN</sub> = 0V)

Parameter	Description	Typ.	Max.	Unit
C <sub>IN</sub>	Input Capacitance	5	7	pF

### NOTE:

- Capacitance applies to all inputs except TEST, FS, nF[1:0], and DS[1:0].

## PIN DESCRIPTION

Pin Name	Type	Description
REF	IN	Reference Clock Input
FB	IN	Feedback Input
TEST <sup>(1)</sup>	IN	When MID or HIGH, disables PLL (except for conditions of Note 1). REF goes to all outputs. Skew Selections (See Control Summary Table) remain in effect. Set LOW for normal operation.
sOE <sup>(1)</sup>	IN	Synchronous Output Enable. When HIGH, it stops clock outputs (except 2Q0 and 2Q1) in a LOW state (for PE = H) - 2Q0 and 2Q1 may be used as the feedback signal to maintain phase lock. When TEST is held at MID level and sOE is HIGH, the nF[1:0] pins act as output disable controls for individual banks when nF[1:0] = LL. Set sOE LOW for normal operation (has internal pull-down).
PE	IN	Selectable positive or negative edge control. When LOW/HIGH the outputs are synchronized with the negative/positive edge of the reference clock (has internal pull-up).
nF[1:0]	IN	3-level inputs for selecting 1 of 9 skew taps or frequency functions
FS	IN	Selects appropriate oscillator circuit based on anticipated frequency range. (See Programmable Skew Range.)
nQ[1:0]	OUT	Four banks of two outputs with programmable skew
V <sub>DDQ</sub>	PWR	Power supply for output buffers
V <sub>DD</sub>	PWR	Power supply for phase locked loop, lock output, and other internal circuitry
GND	PWR	Ground

### NOTE:

- When TEST = MID and sOE = HIGH, PLL remains active with nF[1:0] = LL functioning as an output disable control for individual output banks. Skew selections remain in effect unless nF[1:0] = LL.

## PROGRAMMABLE SKEW

Output skew with respect to the REF input is adjustable to compensate for PCB trace delays, backplane propagation delays or to accommodate requirements for special timing relationships between clocked components. Skew is selectable as a multiple of a time unit (tu) which ranges from 625ps to 1.3ns (see Programmable Skew Range and Resolution Table). There are nine skew configurations available for each output pair. These configurations are chosen by the nF<sub>1:0</sub> control pins. In order

to minimize the number of control pins, 3-level inputs (HIGH-MID-LOW) are used, they are intended for but not restricted to hard-wiring. Undriven 3-level inputs default to the MID level. Where programmable skew is not a requirement, the control pins can be left open for the zero skew default setting. The Control Summary Table shows how to select specific skew taps by using the nF<sub>1:0</sub> control pins.

## EXTERNAL FEEDBACK

By providing external feedback, the IDT5V9950 gives users flexibility with regard to skew adjustment. The FB signal is compared with the input REF signal at the phase detector in order to drive the VCO. Phase differences cause the VCO of the PLL to adjust upwards or downwards accordingly.

An internal loop filter moderates the response of the VCO to the phase detector. The loop filter transfer function has been chosen to provide minimal jitter (or frequency variation) while still providing accurate responses to input frequency changes.

## PROGRAMMABLE SKEW RANGE AND RESOLUTION TABLE

	FS = LOW	FS = MID	FS = HIGH	Comments
Timing Unit Calculation (tu)	$1/(32 \times F_{NOM})$	$1/(16 \times F_{NOM})$	$1/(8 \times F_{NOM})$	
VCO Frequency Range (F <sub>NOM</sub> ) <sup>(1,2)</sup>	24 to 50MHz	48 to 100MHz	96 to 200MHz	
Skew Adjustment Range <sup>(3)</sup>				
Max Adjustment:	±7.8125ns	±7.8125ns	±7.8125ns	ns
	±67.5°	±135°	±270°	Phase Degrees
	±18.75%	±37.5%	±75%	% of Cycle Time
Example 1, F <sub>NOM</sub> = 25MHz	tu = 1.25ns	—	—	
Example 2, F <sub>NOM</sub> = 37.5MHz	tu = 0.833ns	—	—	
Example 3, F <sub>NOM</sub> = 50MHz	tu = 0.625ns	tu = 1.25ns	—	
Example 4, F <sub>NOM</sub> = 75MHz	—	tu = 0.833ns	—	
Example 5, F <sub>NOM</sub> = 100MHz	—	tu = 0.625ns	tu = 1.25ns	
Example 6, F <sub>NOM</sub> = 150MHz	—	—	tu = 0.833ns	
Example 7, F <sub>NOM</sub> = 200MHz	—	—	tu = 0.625ns	

### NOTES:

- The device may be operated outside recommended frequency ranges without damage, but functional operation is not guaranteed.
- The level to be set on FS is determined by the nominal operating frequency of the VCO and Time Unit Generator. The VCO frequency always appears at 1Q<sub>1:0</sub>, 2Q<sub>1:0</sub>, and the higher outputs when they are operated in their undivided modes. The frequency appearing at the REF and FB inputs will be the same as VCO when the output connected to FB is undivided. The frequency of the REF and FB inputs will be 1/2 or 1/4 the VCO frequency when the part is configured for frequency multiplication by using a divided output as the FB input.
- Skew adjustment range assumes that a zero skew output is used for feedback. If a skewed Q output is used for feedback, then adjustment range will be greater. For example if a 4tu skewed output is used for feedback, all other outputs will be skewed -4tu in addition to whatever skew value is programmed for those outputs. 'Max adjustment' range applies to output pairs 3 and 4 where ± 6tu skew adjustment is possible and at the lowest F<sub>NOM</sub> value.

## CONTROL SUMMARY TABLE FOR FEEDBACK SIGNALS

nF1:0	Skew (Pair #1, #2)	Skew (Pair #3)	Skew (Pair #4)
LL <sup>(1)</sup>	-4t <sub>u</sub>	Divide by 2	Divide by 2
LM	-3t <sub>u</sub>	-6t <sub>u</sub>	-6t <sub>u</sub>
LH	-2t <sub>u</sub>	-4t <sub>u</sub>	-4t <sub>u</sub>
ML	-1t <sub>u</sub>	-2t <sub>u</sub>	-2t <sub>u</sub>
MM	Zero Skew	Zero Skew	Zero Skew
MH	1t <sub>u</sub>	2t <sub>u</sub>	2t <sub>u</sub>
HL	2t <sub>u</sub>	4t <sub>u</sub>	4t <sub>u</sub>
HM	3t <sub>u</sub>	6t <sub>u</sub>	6t <sub>u</sub>
HH	4t <sub>u</sub>	Divide by 4	Inverted <sup>(2)</sup>

### NOTES:

- LL disables outputs if TEST = MID and  $\overline{sOE}$  = HIGH.
- When pair #4 is set to HH (inverted),  $\overline{sOE}$  disables pair #4 HIGH when PE = HIGH,  $\overline{sOE}$  disables pair #4 LOW when PE = LOW.

## RECOMMENDED OPERATING RANGE

Symbol	Description	Min.	Typ.	Max.	Unit
V <sub>DD</sub> /V <sub>DDQ</sub>	Power Supply Voltage	3	3.3	3.6	V
T <sub>A</sub>	Ambient Operating Temperature	-40	+25	+85	°C

## DC ELECTRICAL CHARACTERISTICS OVER OPERATING RANGE

Symbol	Parameter	Conditions	Min.	Max.	Unit
V <sub>IH</sub>	Input HIGH Voltage	Guaranteed Logic HIGH (REF, FB Inputs Only)	2	—	V
V <sub>IL</sub>	Input LOW Voltage	Guaranteed Logic LOW (REF, FB Inputs Only)	—	0.8	V
V <sub>IHH</sub>	Input HIGH Voltage <sup>(1)</sup>	3-Level Inputs Only	V <sub>DD</sub> -0.6	—	V
V <sub>IMM</sub>	Input MID Voltage <sup>(1)</sup>	3-Level Inputs Only	V <sub>DD</sub> /2-0.3	V <sub>DD</sub> /2+0.3	V
V <sub>ILL</sub>	Input LOW Voltage <sup>(1)</sup>	3-Level Inputs Only	—	0.6	V
I <sub>IN</sub>	Input Leakage Current (REF, FB Inputs Only)	V <sub>IN</sub> = V <sub>DD</sub> or GND V <sub>DD</sub> = Max.	-5	+5	μA
I <sub>3</sub>	3-Level Input DC Current (TEST, FS, nF[1:0])	V <sub>IN</sub> = V <sub>DD</sub> HIGH Level	—	+200	μA
		V <sub>IN</sub> = V <sub>DD</sub> /2 MID Level	-50	+50	
		V <sub>IN</sub> = GND LOW Level	-200	—	
I <sub>PU</sub>	Input Pull-Up Current (PE)	V <sub>DD</sub> = Max., V <sub>IN</sub> = GND	-100	—	μA
I <sub>PD</sub>	Input Pull-Down Current ( $\overline{sOE}$ )	V <sub>DD</sub> = Max., V <sub>IN</sub> = V <sub>DD</sub>	—	+100	μA
V <sub>OH</sub>	Output HIGH Voltage	V <sub>DDQ</sub> = Min., I <sub>OH</sub> = -12mA	2.4	—	V
V <sub>OL</sub>	Output LOW Voltage	V <sub>DDQ</sub> = Min., I <sub>OL</sub> = 12mA	—	0.4	V

### NOTE:

- These inputs are normally wired to V<sub>DD</sub>, GND, or unconnected. Internal termination resistors bias unconnected inputs to V<sub>DD</sub>/2. If these inputs are switched, the function and timing of the outputs may be glitched, and the PLL may require an additional lock time before all datasheet limits are achieved.

## POWER SUPPLY CHARACTERISTICS

Symbol	Parameter	Test Conditions <sup>(1)</sup>	Typ. <sup>(2)</sup>	Max.	Unit
I <sub>DDQ</sub>	Quiescent Power Supply Current	V <sub>DD</sub> = Max., TEST = MID, REF = LOW, PE = LOW, $\overline{\text{SOE}}$ = LOW, FS = MID All outputs unloaded	20	30	mA
$\Delta$ I <sub>DD</sub>	Power Supply Current per Input HIGH (REF and FB inputs only)	V <sub>IN</sub> = 3V, V <sub>DD</sub> = Max., TEST = HIGH	1	30	$\mu$ A
I <sub>DDD</sub>	Dynamic Power Supply Current per Output	FS = L	190	290	$\mu$ A/MHz
		FS = M	150	230	
		FS = H	130	200	
I <sub>TOT</sub>	Total Power Supply Current	FS = L, F <sub>VCO</sub> = 50MHz, C <sub>L</sub> = 0pF	56	—	mA
		FS = M, F <sub>VCO</sub> = 100MHz, C <sub>L</sub> = 0pF	80	—	
		FS = H, F <sub>VCO</sub> = 200MHz, C <sub>L</sub> = 0pF	125	—	

### NOTES:

- Measurements are for divide-by-1 outputs and nF<sub>[1:0]</sub> = MM.
- For nominal voltage and temperature.

## INPUT TIMING REQUIREMENTS

Symbol	Description <sup>(1)</sup>		Min.	Max.	Unit
t <sub>R</sub> , t <sub>F</sub>	Maximum input rise and fall times, 0.8V to 2V		—	10	ns/V
t <sub>PWC</sub>	Input clock pulse, HIGH or LOW		2	—	ns
D <sub>H</sub>	Input duty cycle		10	90	%
F <sub>REF</sub>	Reference clock input frequency	FS = LOW	6	50	MHz
		FS = MID	12	100	
		FS = HIGH	24	200	

### NOTE:

- Where pulse width implied by D<sub>H</sub> is less than t<sub>PWC</sub> limit, t<sub>PWC</sub> limit applies.

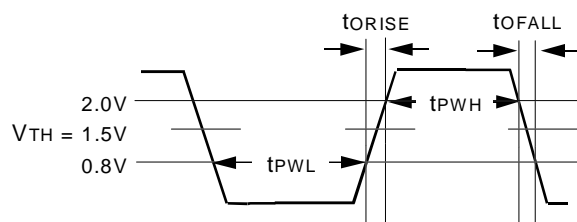
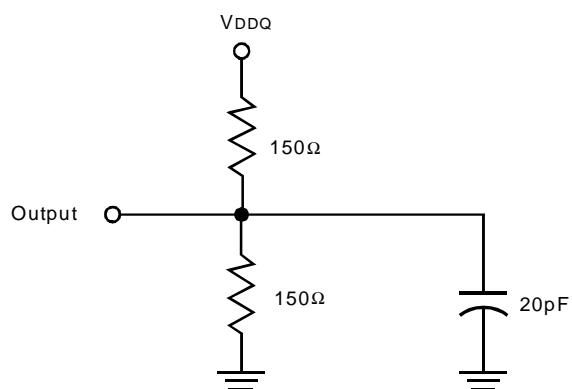
## SWITCHING CHARACTERISTICS OVER OPERATING RANGE

Symbol	Parameter	Min.	Typ.	Max.	Unit
F <sub>NOM</sub>	VCO Frequency Range	See Programmable Skew Range and Resolution Table			
t <sub>RPWH</sub>	REF Pulse Width HIGH <sup>(1)</sup>	2	—	—	ns
t <sub>RPWL</sub>	REF Pulse Width LOW <sup>(1)</sup>	2	—	—	ns
t <sub>U</sub>	Programmable Skew Time Unit	See Control Summary Table			
t <sub>SKWPR</sub>	Zero Output Matched-Pair Skew (xQ0, xQ1) <sup>(2,3)</sup>	—	50	185	ps
t <sub>SKW0</sub>	Zero Output Skew (All Outputs) <sup>(4)</sup>	—	0.1	0.25	ns
t <sub>SKW1</sub>	Output Skew (Rise-Rise, Fall-Fall, Same Class Outputs) <sup>(5)</sup>	—	0.1	0.25	ns
t <sub>SKW2</sub>	Output Skew (Rise-Fall, Nominal-Inverted, Divided-Divided) <sup>(5)</sup>	—	0.2	0.5	ns
t <sub>SKW3</sub>	Output Skew (Rise-Rise, Fall-Fall, Different Class Outputs) <sup>(5)</sup>	—	0.15	0.5	ns
t <sub>SKW4</sub>	Output Skew (Rise-Fall, Nominal-Divided, Divided-Inverted) <sup>(2)</sup>	—	0.3	0.9	ns
t <sub>DEV</sub>	Device-to-Device Skew <sup>(2,6)</sup>	—	—	0.75	ns
t <sub>φ</sub>	REF Input to FB Static Phase Offset <sup>(7)</sup>	−0.25	—	0.25	ns
t <sub>ODCV</sub>	Output Duty Cycle Variation from 50%	−1	0	1	ns
t <sub>PWH</sub>	Output HIGH Time Deviation from 50% <sup>(8)</sup>	—	—	1.5	ns
t <sub>PWL</sub>	Output LOW Time Deviation from 50% <sup>(9)</sup>	—	—	2	ns
t <sub>ORISE</sub>	Output Rise Time	0.15	0.7	1.5	ns
t <sub>OFALL</sub>	Output Fall Time	0.15	0.7	1.5	ns
t <sub>LOCK</sub>	PLL Lock Time <sup>(10)</sup>	—	—	0.5	ms
t <sub>CCJH</sub>	Cycle-to-Cycle Output Jitter (peak-to-peak) (divide by 1 output frequency, FS = H, FB divide-by-n=1,2)	—	—	100	ps
t <sub>CCJM</sub>	Cycle-to-Cycle Output Jitter (peak-to-peak) (divide by 1 output frequency, FS = M)	—	—	150	
t <sub>CCJL</sub>	Cycle-to-Cycle Output Jitter (peak-to-peak) (divide by 1 output frequency, FS = L, F <sub>REF</sub> > 3MHz)	—	—	200	

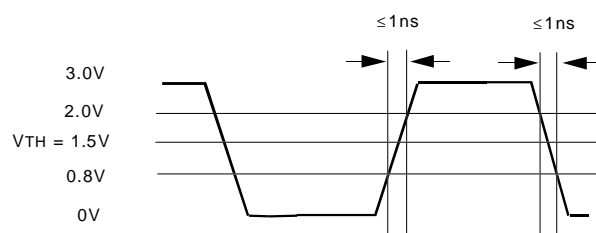
### NOTES:

1. Refer to Input Timing Requirements table for more detail.
2. Skew is the time between the earliest and the latest output transition among all outputs for which the same t<sub>U</sub> delay has been selected when all are loaded with the specified load.
3. t<sub>SKWPR</sub> is the skew between a pair of outputs (xQ0 and xQ1) when all eight outputs are selected for 0t<sub>U</sub>.
4. t<sub>SK(0)</sub> is the skew between outputs when they are selected for 0t<sub>U</sub>.
5. There are 3 classes of outputs: Nominal (multiple of t<sub>U</sub> delay), Inverted (4Q0 and 4Q1 only with 4F0 = 4F1 = HIGH), and Divided (3Qx and 4Qx only in Divide-by-2 or Divide-by-4 mode). Test condition: nF0:1=MM is set on unused outputs.
6. t<sub>DEV</sub> is the output-to-output skew between any two devices operating under the same conditions (V<sub>DDQ</sub>, V<sub>DD</sub>, ambient temperature, air flow, etc.)
7. t<sub>φ</sub> is measured with REF input rise and fall times (from 0.8V to 2V) of 0.5ns. Measured from 1.5V on REF to 1.5V on FB.
8. Measured at 2V.
9. Measured at 0.8V.
10. t<sub>LOCK</sub> is the time that is required before synchronization is achieved. This specification is valid only after V<sub>DD</sub>/V<sub>DDQ</sub> is stable and within normal operating limits. This parameter is measured from the application of a new signal or frequency at REF or FB until t<sub>PD</sub> is within specified limits.

## AC TEST LOADS AND WAVEFORMS

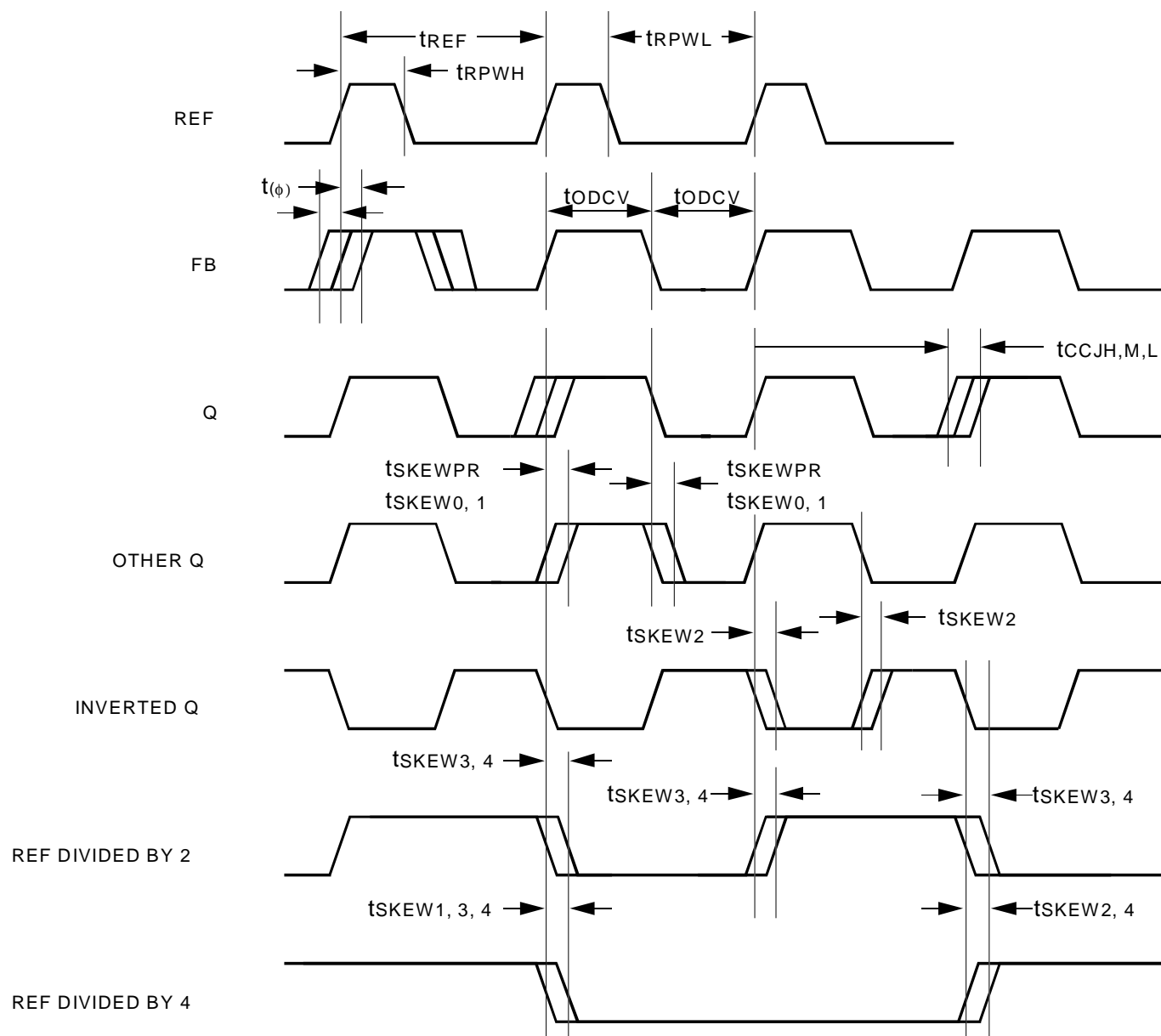


*LVTTL Output Waveform*



*LVTTL Input Test Waveform*

## AC TIMING DIAGRAM



### NOTES:

PE: The AC Timing Diagram applies to PE=VDD. For PE=GND, the negative edge of FB aligns with the negative edge of REF, divided outputs change on the negative edge of REF, and the positive edges of the divide-by-2 and the divide-by-4 signals align.

Skew: The time between the earliest and the latest output transition among all outputs for which the same  $t_u$  delay has been selected when all are loaded with 20pF and terminated with 75Ω to VDDQ/2.

tSKEWPR: The skew between a pair of outputs (xQ0 and xQ1) when all eight outputs are selected for 0tu.

tSKEW0: The skew between outputs when they are selected for 0tu.

tDEV: The output-to-output skew between any two devices operating under the same conditions (VDDQ, VDD, ambient temperature, air flow, etc.)

tODCV: The deviation of the output from a 50% duty cycle. Output pulse width variations are included in tSKEW2 and tSKEW4 specifications.

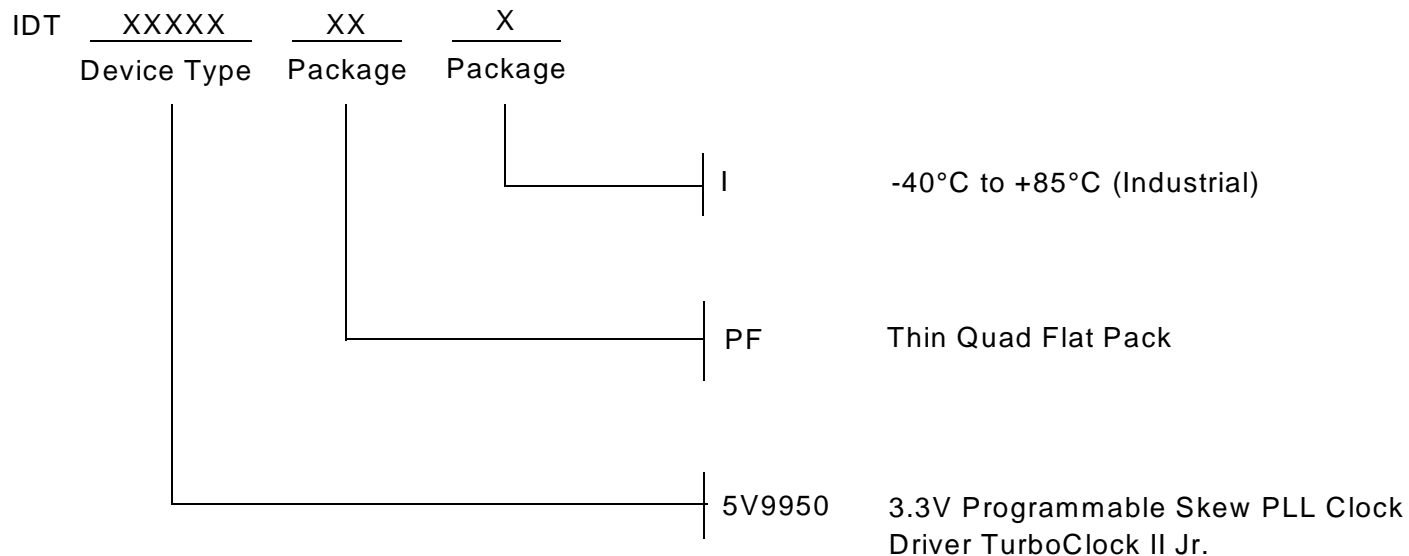
TPWH is measured at 2V.

TPWL is measured at 0.8V.

torise and tofall are measured between 0.8V and 2V.

tLOCK: The time that is required before synchronization is achieved. This specification is valid only after VDD/VDDQ is stable and within normal operating limits. This parameter is measured from the application of a new signal or frequency at REF or FB until tPD is within specified limits.

## ORDERING INFORMATION



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