HIGH-SPEED 3.3V 16K x 16 SYNCHRONOUS PIPELINED DUAL-PORT STATIC RAM
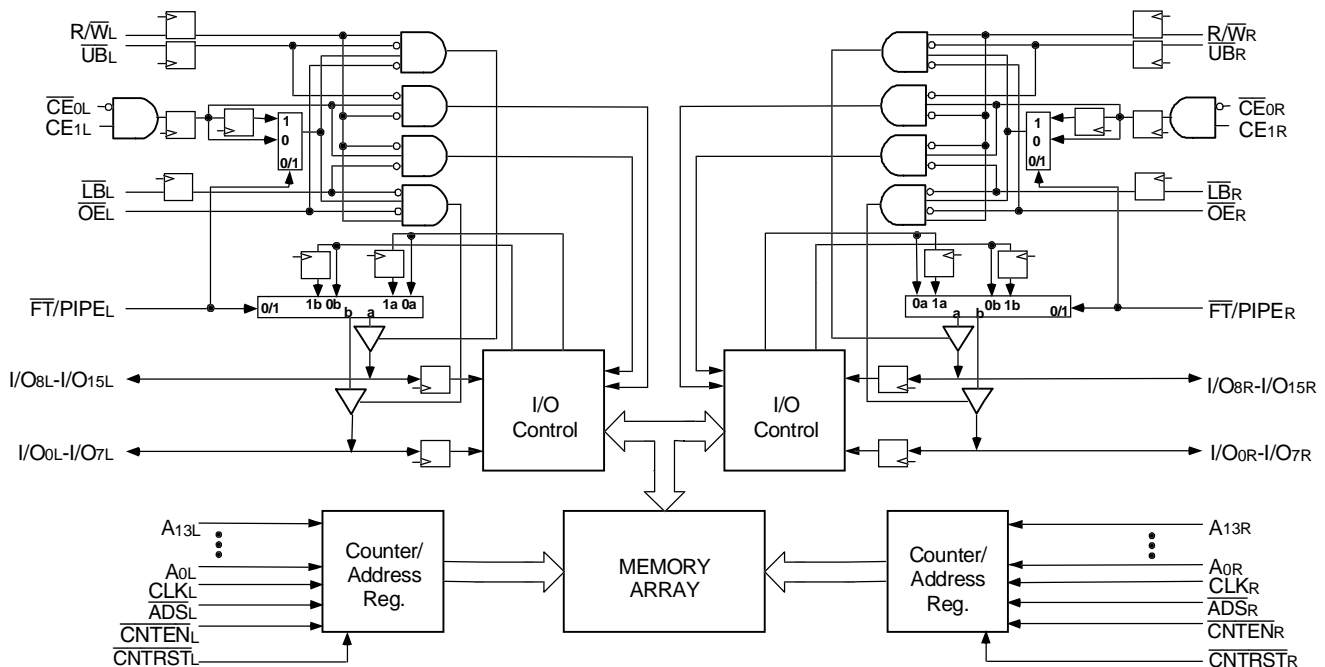
IDT70V9269S/L

Features:

- True Dual-Ported memory cells which allow simultaneous access of the same memory location
- High-speed clock to data access
  - Commercial: 9/12/15ns (max.)
- Low-power operation
  - IDT70V9269S
    Active: 429mW (typ.)
    Standby: 3.3mW (typ.)
  - IDT70V9269L
    Active: 429mW (typ.)
    Standby: 1.32mW (typ.)
- Flow-through or Pipelined output mode on either port via the $\overline{FT}$/PIPE pin
- Counter enable and reset features
- Dual chip enables allow for depth expansion without additional logic
- Full synchronous operation on both ports
  - 4ns setup to clock and 1ns hold on all Control, data, and address inputs
  - Data input, address, and control registers
  - Fast 9ns clock to data out in the Pipelined output mode
  - Self-timed write allows fast cycle time
  - 15ns cycle time, 66MHz operation in Pipelined output mode
- Separate upper-byte and lower-byte controls for multiplexed bus and bus matching compatibility
- LVTTL- compatible, single 3.3V (±0.3V) power supply
- Industrial temperature range (–40°C to +85°C) is available for selected speeds
- Available in a 128-pin Thin Quad Flatpack (TQFP) package

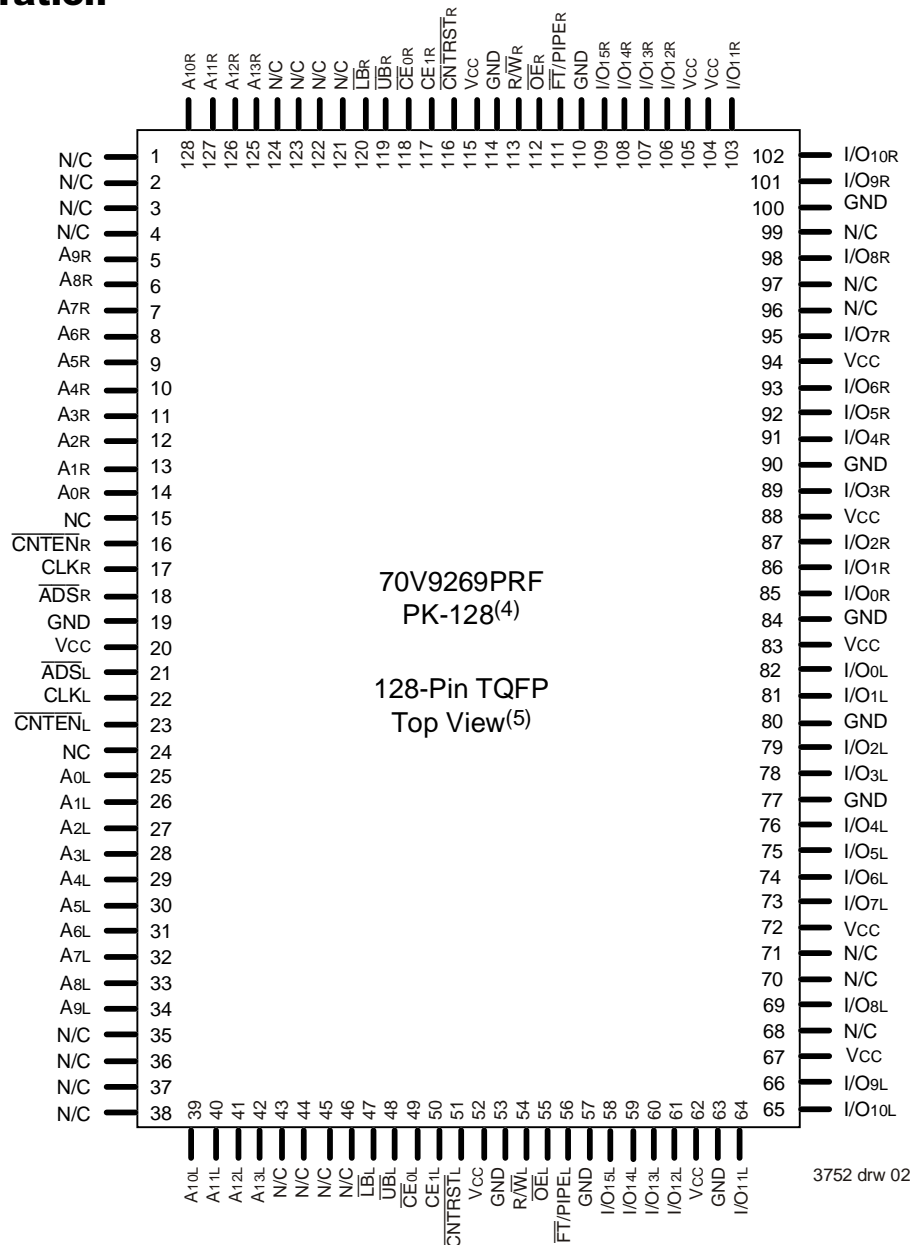## Functional Block Diagram

3752 drw 01

JANUARY 2001

DSC 3752/6

Description:

The IDT70V9269 is a high-speed 16K x 16 bit synchronous Dual-Port RAM. The memory array utilizes Dual-Port memory cells to allow simultaneous access of any address from both ports. Registers on control, data, and address in-puts provide minimal setup and hold times. The timing latitude provided by this approach allows systems to be designed with very short cycle times.

With an input data register, the IDT70V9269 has been optimized for applications having unidirectional or bidirectional data flow in bursts. An automatic power down feature, controlled by $\overline{CE}_0$ and CE_1, permits the on-chip circuitry of each port to enter a very low standby power mode. Fabricated using IDT's CMOS high-performance technology, these devices typically operate on only 429mW of power.

Pin Configuration[1,2,3]

70V9269PRF
PK-128[4]

128-Pin TQFP
Top View[5]

Left side (pins 1–38):

Pin	Signal
1	N/C
2	N/C
3	N/C
4	N/C
5	A_{9R}
6	A_{8R}
7	A_{7R}
8	A_{6R}
9	A_{5R}
10	A_{4R}
11	A_{3R}
12	A_{2R}
13	A_{1R}
14	A_{0R}
15	NC
16	$\overline{CNTEN}_R$
17	CLK_R
18	$\overline{ADS}_R$
19	GND
20	V_{CC}
21	$\overline{ADS}_L$
22	CLK_L
23	$\overline{CNTEN}_L$
24	NC
25	A_{0L}
26	A_{1L}
27	A_{2L}
28	A_{3L}
29	A_{4L}
30	A_{5L}
31	A_{6L}
32	A_{7L}
33	A_{8L}
34	A_{9L}
35	N/C
36	N/C
37	N/C
38	N/C

Top side (pins 128–103):

Pin	Signal
128	A_{10R}
127	A_{11R}
126	A_{12R}
125	A_{13R}
124	N/C
123	N/C
122	N/C
121	N/C
120	$\overline{LB}_R$
119	$\overline{UB}_R$
118	$\overline{CE}_{0R}$
117	CE_{1R}
116	$\overline{CNTRST}_R$
115	V_{CC}
114	GND
113	$R/\overline{W}_R$
112	$\overline{OE}_R$
111	$FT/\overline{PIPE}_R$
110	GND
109	I/O_{15R}
108	I/O_{14R}
107	I/O_{13R}
106	I/O_{12R}
105	V_{CC}
104	V_{CC}
103	I/O_{11R}

Right side (pins 102–65):

Pin	Signal
102	I/O_{10R}
101	I/O_{9R}
100	GND
99	N/C
98	I/O_{8R}
97	N/C
96	N/C
95	I/O_{7R}
94	V_{CC}
93	I/O_{6R}
92	I/O_{5R}
91	I/O_{4R}
90	GND
89	I/O_{3R}
88	V_{CC}
87	I/O_{2R}
86	I/O_{1R}
85	I/O_{0R}
84	GND
83	V_{CC}
82	I/O_{0L}
81	I/O_{1L}
80	GND
79	I/O_{2L}
78	I/O_{3L}
77	GND
76	I/O_{4L}
75	I/O_{5L}
74	I/O_{6L}
73	I/O_{7L}
72	V_{CC}
71	N/C
70	N/C
69	I/O_{8L}
68	N/C
67	V_{CC}
66	I/O_{9L}
65	I/O_{10L}

Bottom side (pins 39–64):

Pin	Signal
39	A_{10L}
40	A_{11L}
41	A_{12L}
42	A_{13L}
43	N/C
44	N/C
45	N/C
46	N/C
47	$\overline{LB}_L$
48	$\overline{UB}_L$
49	$\overline{CE}_{0L}$
50	CE_{1L}
51	$\overline{CNTRST}_L$
52	V_{CC}
53	GND
54	$R/\overline{W}_L$
55	$\overline{OE}_L$
56	$FT/\overline{PIPE}_L$
57	GND
58	I/O_{15L}
59	I/O_{14L}
60	I/O_{13L}
61	I/O_{12L}
62	V_{CC}
63	GND
64	I/O_{11L}

3752 drw 02

NOTES:
1. All Vcc pins must be connected to power supply.
2. All GND pins must be connected to ground supply.
3. Package body is approximately 14mm x 20mm x 1.4mm.
4. This package code is used to reference the package diagram.
5. This text does not indicate orientation of the actual part-marking.

Pin Names

Left Port	Right Port	Names
$\overline{CE}_{0L}$, CE_{1L}	$\overline{CE}_{0R}$, CE_{1R}	Chip Enables
$R/\overline{W}_L$	$R/\overline{W}_R$	Read/Write Enable
$\overline{OE}_L$	$\overline{OE}_R$	Output Enable
A_{0L} - A_{13L}	A_{0R} - A_{13R}	Address
I/O_{0L} - I/O_{15L}	I/O_{0R} - I/O_{15R}	Data Input/Output
CLK_L	CLK_R	Clock
$\overline{UB}_L$	$\overline{UB}_R$	Upper Byte Select
$\overline{LB}_L$	$\overline{LB}_R$	Lower Byte Select
$\overline{ADS}_L$	$\overline{ADS}_R$	Address Strobe Enable
$\overline{CNTEN}_L$	$\overline{CNTEN}_R$	Counter Enable
$\overline{CNTRST}_L$	$\overline{CNTRST}_R$	Counter Reset
$\overline{FT}/PIPE_L$	$\overline{FT}/PIPE_R$	Flow-Through / Pipeline
V_{CC}		Power
GND		Ground

3752 tbl 01

Truth Table I—Read/Write and Enable Control[1,2,3]

$\overline{OE}$	CLK	$\overline{CE}_0$	CE_1	$\overline{UB}$	$\overline{LB}$	$R/\overline{W}$	Upper Byte I/O$_{8-15}$	Lower Byte I/O$_{0-7}$	MODE
X	↑	H	X	X	X	X	High-Z	High-Z	Deselected–Power Down
X	↑	X	L	X	X	X	High-Z	High-Z	Deselected–Power Down
X	↑	L	H	H	H	X	High-Z	High-Z	Both Bytes Deselected
X	↑	L	H	L	H	L	DATA$_{IN}$	High-Z	Write to Upper Byte Only
X	↑	L	H	H	L	L	High-Z	DATA$_{IN}$	Write to Lower Byte Only
X	↑	L	H	L	L	L	DATA$_{IN}$	DATA$_{IN}$	Write to Both Bytes
L	↑	L	H	L	H	H	DATA$_{OUT}$	High-Z	Read Upper Byte Only
L	↑	L	H	H	L	H	High-Z	DATA$_{OUT}$	Read Lower Byte Only
L	↑	L	H	L	L	H	DATA$_{OUT}$	DATA$_{OUT}$	Read Both Bytes
H	↑	L	H	L	L	X	High-Z	High-Z	Outputs Disabled

3752 tbl 02

NOTES:
1. "H" = V_{IH}, "L" = V_{IL}, "X" = Don't Care.
2. $\overline{ADS}$, $\overline{CNTEN}$, $\overline{CNTRST}$ = X.
3. $\overline{OE}$ is an asynchronous input signal.

Truth Table II—Address Counter Control[1,2]

Address	Previous Address	Addr Used	CLK	$\overline{ADS}$	$\overline{CNTEN}$	$\overline{CNTRST}$	I/O[3]	MODE
X	X	0	↑	X	X	L	D$_{I/O}$(0)	Counter Reset to Address 0
An	X	An	↑	L[4]	X	H	D$_{I/O}$(n)	External Address Loaded into Counter
An	Ap	Ap	↑	H	H	H	D$_{I/O}$(p)	External Address Blocked—Counter disabled (Ap reused)
X	Ap	Ap + 1	↑	H	L[5]	H	D$_{I/O}$(p+1)	Counter Enabled—Internal Address generation

3752 tbl 03

NOTES:
1. "H" = V$_{IH}$, "L" = V$_{IL}$, "X" = Don't Care.
2. $\overline{CE}_0$, $\overline{LB}$, $\overline{UB}$, and $\overline{OE}$ = V$_{IL}$; CE$_1$ and R/$\overline{W}$ = V$_{IH}$.
3. Outputs configured in Flow-Through Output mode; if outputs are in Pipelined mode the data out will be delayed by one cycle.
4. $\overline{ADS}$ is independent of all other signals including $\overline{CE}_0$, CE$_1$, $\overline{UB}$ and $\overline{LB}$.
5. The address counter advances if $\overline{CNTEN}$ = V$_{IL}$ on the rising edge of CLK, regardless of all other signals including $\overline{CE}_0$, CE$_1$, $\overline{UB}$ and $\overline{LB}$.

Recommended Operating Temperature and Supply Voltage[1,2]

Grade	Ambient Temperature	GND	Vcc
Commercial	0°C to +70°C	0V	3.3V ± 0.3V
Industrial	-40°C to +85°C	0V	3.3V ± 0.3V

3752 tbl 04

NOTE:
1. Industrial temperature: for specific speeds, packages and powers contact your sales office.
2. This is the parameter T$_A$. This is the "instant on" case temperature.

Recommend DC Operating Conditions

Symbol	Parameter	Min.	Typ.	Max.	Unit
V$_{CC}$	Supply Voltage	3.0	3.3	3.6	V
GND	Ground	0	0	0	V
V$_{IH}$	Input High Voltage	2.2	—	Vcc+0.3V[2]	V
V$_{IL}$	Input Low Voltage	-0.3[1]	—	0.8	V

3752 tbl 05

NOTES:
1. V$_{IL}$ ≥ -1.5V for pulse width less than 10 ns.
2. V$_{TERM}$ must not exceed Vcc + 0.3V.

Absolute Maximum Ratings[1]

Symbol	Rating	Commercial & Industrial	Unit
V$_{TERM}$[2]	Terminal Voltage with Respect to GND	-0.5 to +4.6	V
T$_{BIAS}$	Temperature Under Bias	-55 to +125	°C
T$_{STG}$	Storage Temperature	-65 to +150	°C
I$_{OUT}$	DC Output Current	50	mA

3752 tbl 06

NOTES:
1. Stresses greater than those listed under ABSOLUTE MAXIMUM RATINGS may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect reliability.
2. V$_{TERM}$ must not exceed V$_{CC}$ + 0.3V for more than 25% of the cycle time or 10ns maximum, and is limited to ≤ 20mA for the period of V$_{TERM}$ ≥ V$_{CC}$ + 0.3V.

Capacitance[1] (T$_A$ = +25°C, f = 1.0MHz)

Symbol	Parameter	Conditions[2]	Max.	Unit
C$_{IN}$	Input Capacitance	V$_{IN}$ = 3dV	9	pF
C$_{OUT}$[3]	Output Capacitance	V$_{OUT}$ = 3dV	10	pF

3752 tbl 07

NOTES:
1. These parameters are determined by device characterization, but are not production tested.
2. 3dV references the interpolated capacitance when the input and output switch from 0V to 3V or from 3V to 0V.
3. C$_{OUT}$ also references C$_{I/O}$.

DC Electrical Characteristics Over the Operating Temperature and Supply Voltage Range (Vcc = 3.3V ± 0.3V)

Symbol	Parameter	Test Conditions	70V9269S		70V9269L		Unit
			Min.	Max.	Min.	Max.	
$|I_{LI}|$	Input Leakage Current[1]	V_{CC} = 3.6V, V_{IN} = 0V to V_{CC}	—	10	—	5	µA
$|I_{LO}|$	Output Leakage Current	$\overline{CE}$ = V_{IH} or CE1 = V_{IL}, V_{OUT} = 0V to V_{CC}	—	10	—	5	µA
V_{OL}	Output Low Voltage	I_{OL} = +4mA	—	0.4	—	0.4	V
V_{OH}	Output High Voltage	I_{OH} = -4mA	2.4	—	2.4	—	V

3752 tbl 08

NOTE:
1. At $V_{CC} \leq 2.0V$ input leakages are undefined.

DC Electrical Characteristics Over the Operating Temperture and Supply Voltage Range[3,6,7] (Vcc = 3.3V ± 0.3V)

Symbol	Parameter	Test Condition	Version		70V9269X9 Com'l Only		70V9269X12 Com'l Only		70V9269X15 Com'l Only		Unit
					Typ.[4]	Max.	Typ.[4]	Max.	Typ.[4]	Max.	
I_{CC}	Dynamic Operating Current (Both Ports Active)	$\overline{CE}_L$ and $\overline{CE}_R$= V_{IL}, Outputs Disabled, f = f$_{MAX}$[1]	COM'L	S L	180 180	260 225	150 150	240 205	130 130	220 185	mA
			IND	S L	— —	— —	— —	— —	— —	— —	
I_{SB1}	Standby Current (Both Ports - TTL Level Inputs)	$\overline{CE}_L$ = $\overline{CE}_R$ = V_{IH} f = f$_{MAX}$[1]	COM'L	S L	50 50	75 65	40 40	65 50	30 30	55 35	mA
			IND	S L	— —	— —	— —	— —	— —	— —	
I_{SB2}	Standby Current (One Port - TTL Level Inputs)	$\overline{CE}$"A" = V_{IL} and $\overline{CE}$"B" = V_{IH}[5] Active Port Outputs Disabled, f=f$_{MAX}$[1]	COM'L	S L	110 110	170 150	100 100	160 140	90 90	150 130	mA
			IND	S L	— —	— —	— —	— —	— —	— —	
I_{SB3}	Full Standby Current (Both Ports - CMOS Level Inputs)	Both Ports $\overline{CE}_L$ and $\overline{CE}_R \geq V_{CC}$ - 0.2V, $V_{IN} \geq V_{CC}$ - 0.2V or $V_{IN} \leq 0.2V$, f = 0[2]	COM'L	S L	1.0 0.4	5 3	1.0 0.4	5 3	1.0 0.4	5 3	mA
			IND	S L	— —	— —	— —	— —	— —	— —	
I_{SB4}	Full Standby Current (One Port - CMOS Level Inputs)	$\overline{CE}$"A" $\leq 0.2V$ and $\overline{CE}$"B" $\geq V_{CC}$ - 0.2V[5] $V_{IN} \geq V_{CC}$ - 0.2V or $V_{IN} \leq 0.2V$, Active Port, Outputs Disabled, f = f$_{MAX}$[1]	COM'L	S L	100 100	160 140	90 90	150 130	80 80	140 120	mA
			IND	S L	— —	— —	— —	— —	— —	— —	

3752 tbl 09

NOTES:
1. At f = f$_{MAX}$, address and control lines (except Output Enable) are cycling at the maximum frequency clock cycle of 1/t$_{CYC}$, using "AC TEST CONDITIONS" at input levels of GND to 3V.
2. f = 0 means no address, clock, or control lines change. Applies only to input at CMOS level standby.
3. Port "A" may be either left or right port. Port "B" is the opposite from port "A".
4. V_{CC} = 3.3V, T_A = 25°C for Typ, and are not production tested. Icc DC(f=0) = 90mA (Typ).
5. $\overline{CE}$x = V_{IL} means $\overline{CE}$0x = V_{IL} and CE1x = V_{IH}
   $\overline{CE}$x = V_{IH} means $\overline{CE}$0x = V_{IH} or CE1x = V_{IL}
   $\overline{CE}$x $\leq 0.2V$ means $\overline{CE}$0x $\leq 0.2V$ and CE1x $\geq V_{CC}$ - 0.2V
   $\overline{CE}$x $\geq V_{CC}$ - 0.2V means $\overline{CE}$0x $\geq V_{CC}$ - 0.2V or CE1x $\leq 0.2V$
   'X' represents "L" for left port or "R" for right port.
6. 'X' in part number indicates power rating (S or L).
7. Industrial temperature: for specific speeds, packages and powers contact your sales office.
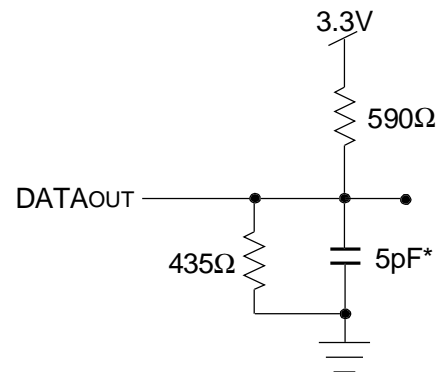
AC Test Conditions

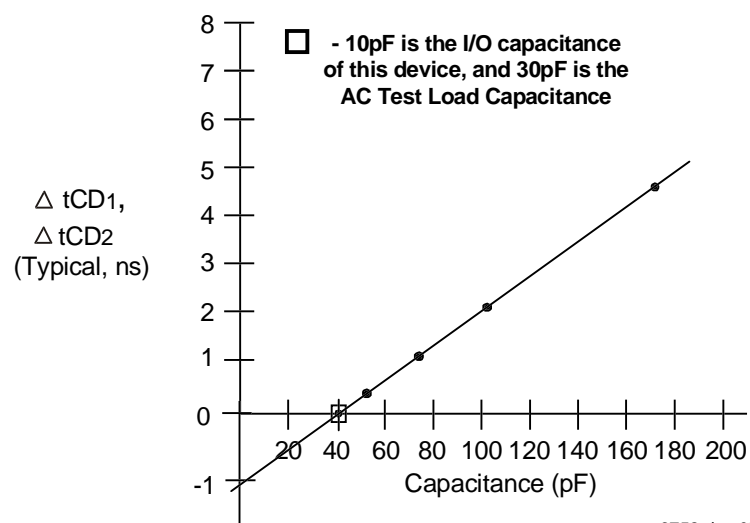|	
Input Pulse Levels	GND to 3.0V
Input Rise/Fall Times	3ns
Input Timing Reference Levels	1.5V
Output Reference Levels	1.5V
Output Load	Figures 1, 2, and 3

3752 tbl 10
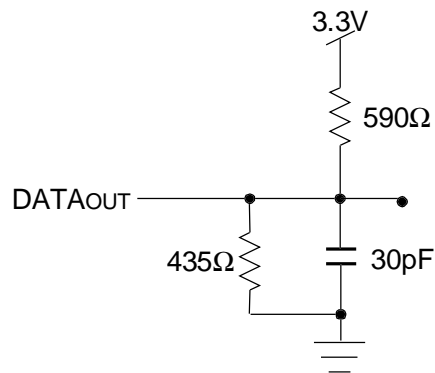
3752 drw 03

Figure 1. AC Output Test load.

3752 drw 04

Figure 2. Output Test Load
(For tCKLZ, tCKHZ, tOLZ, and tOHZ).
*Including scope and jig.

3752 drw 05

Figure 3. Typical Output Derating (Lumped Capacitive Load).

AC Electrical Characteristics Over the Operating Tempurature Range (Read and Write Cycle Timing)[3,4,5] $(V_{CC} = 3.3V \pm 0.3v, T_A = 0°C \text{ to } +70°C)$

Symbol	Parameter	70V9269X9 Com'l Only Min.	70V9269X9 Com'l Only Max.	70V9269X12 Com'l Only Min.	70V9269X12 Com'l Only Max.	70V9269X15 Com'l Only Min.	70V9269X15 Com'l Only Max.	Unit
t_{CYC1}	Clock Cycle Time (Flow-Through)[2]	25	—	30	—	35	—	ns
t_{CYC2}	Clock Cycle Time (Pipelined)[2]	15	—	20	—	25	—	ns
t_{CH1}	Clock High Time (Flow-Through)[2]	12	—	12	—	12	—	ns
t_{CL1}	Clock Low Time (Flow-Through)[2]	12	—	12	—	12	—	ns
t_{CH2}	Clock High Time (Pipelined)[2]	6	—	8	—	10	—	ns
t_{CL2}	Clock Low Time (Pipelined)[2]	6	—	8	—	10	—	ns
t_R	Clock Rise Time	—	3	—	3	—	3	ns
t_F	Clock Fall Time	—	3	—	3	—	3	ns
t_{SA}	Address Setup Time	4	—	4	—	4	—	ns
t_{HA}	Address Hold Time	1	—	1	—	1	—	ns
t_{SC}	Chip Enable Setup Time	4	—	4	—	4	—	ns
t_{HC}	Chip Enable Hold Time	1	—	1	—	1	—	ns
t_{SW}	R/$\overline{W}$ Setup Time	4	—	4	—	4	—	ns
t_{HW}	R/$\overline{W}$ Hold Time	1	—	1	—	1	—	ns
t_{SD}	Input Data Setup Time	4	—	4	—	4	—	ns
t_{HD}	Input Data Hold Time	1	—	1	—	1	—	ns
t_{SAD}	$\overline{ADS}$ Setup Time	4	—	4	—	4	—	ns
t_{HAD}	$\overline{ADS}$ Hold Time	1	—	1	—	1	—	ns
t_{SCN}	$\overline{CNTEN}$ Setup Time	4	—	4	—	4	—	ns
t_{HCN}	$\overline{CNTEN}$ Hold Time	1	—	1	—	1	—	ns
t_{SRST}	$\overline{CNTRST}$ Setup Time	4	—	4	—	4	—	ns
t_{HRST}	$\overline{CNTRST}$ Hold Time	1	—	1	—	1	—	ns
t_{OE}	Output Enable to Data Valid	—	12	—	12	—	15	ns
t_{OLZ}	Output Enable to Output Low-Z[1]	2	—	2	—	2	—	ns
t_{OHZ}	Output Enable to Output High-Z[1]	1	7	1	7	1	7	ns
t_{CD1}	Clock to Data Valid (Flow-Through)[2]	—	20	—	25	—	30	ns
t_{CD2}	Clock to Data Valid (Pipelined)[2]	—	9	—	12	—	15	ns
t_{DC}	Data Output Hold After Clock High	2	—	2	—	2	—	ns
t_{CKHZ}	Clock High to Output High-Z[1]	2	9	2	9	2	9	ns
t_{CKLZ}	Clock High to Output Low-Z[1]	2	—	2	—	2	—	ns
Port-to-Port Delay								
t_{CWDD}	Write Port Clock High to Read Data Delay	—	35	—	40	—	50	ns
t_{CCS}	Clock-to-Clock Setup Time	—	15	—	15	—	20	ns

70V9269 tbl 11

NOTES:
1. Transition is measured 0mV from Low or High-Impedance voltage with the Output Test Load (Figure 2). This parameter is guaranteed by device characterization, but is not production tested.
2. The Pipelined output parameters (t_{CYC2}, t_{CD2}) apply to either or both left and right when $\overline{FT}$/PIPE = V_{IH}. Flow-through parameters (t_{CYC1}, t_{CD1}) apply when $\overline{FT}$/PIPE = V_{IL} for that port.
3. All input signals are synchronous with respect to the clock except for the asynchronous Output Enable ($\overline{OE}$) and $\overline{FT}$/PIPEx.
4. 'X' in part number indicates power rating (S or L).
5. Industrial temperature: for specific speeds, packages and powers contact your sales office.

Timing Waveform of Read Cycle for Flow-through Output on Either Port ($\overline{FT}$/PIPEx = V_{IL})[3]
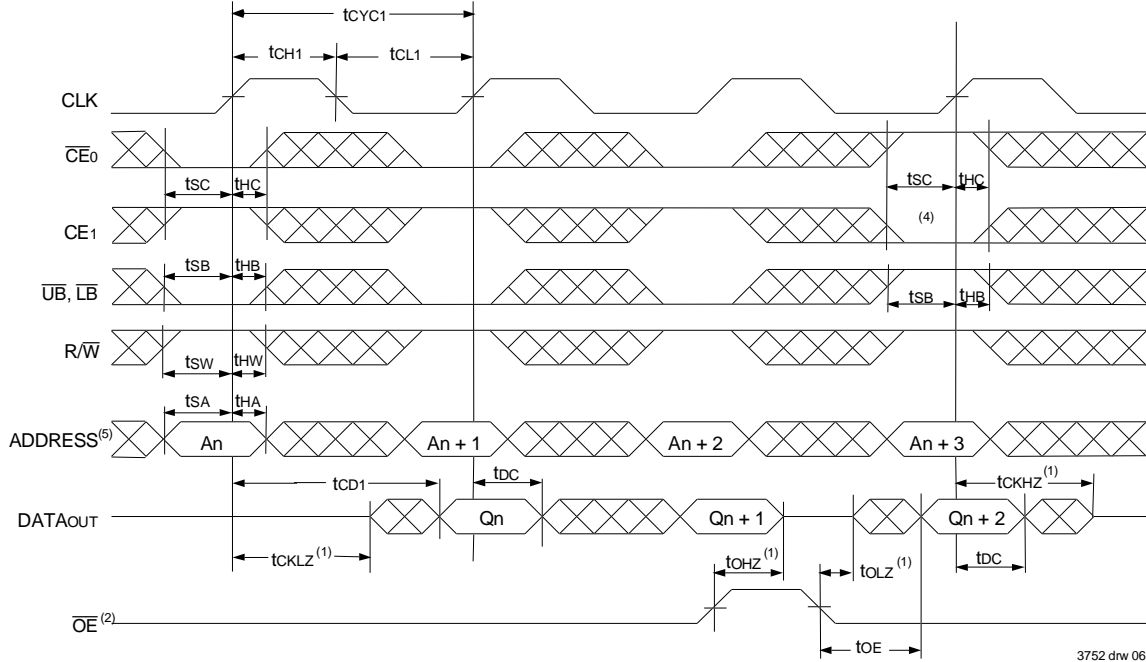
3752 drw 06

Timing Waveform of Read Cycle for Pipelined Operation on Either Port ($\overline{FT}$/PIPEx = V_{IH})[3]
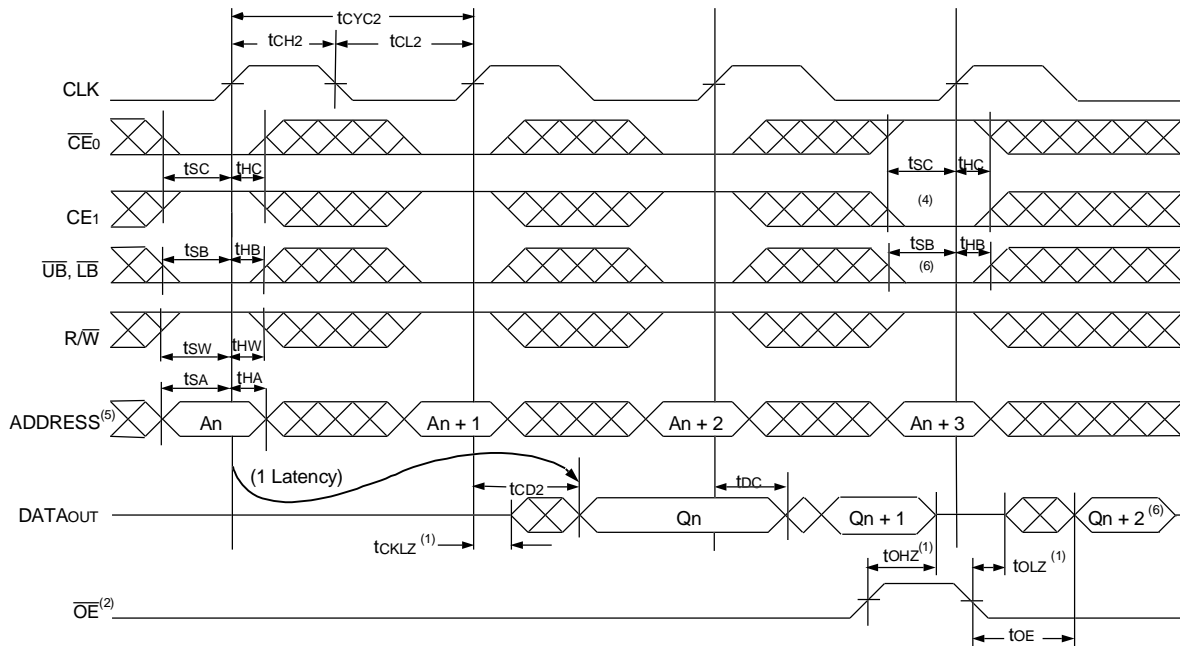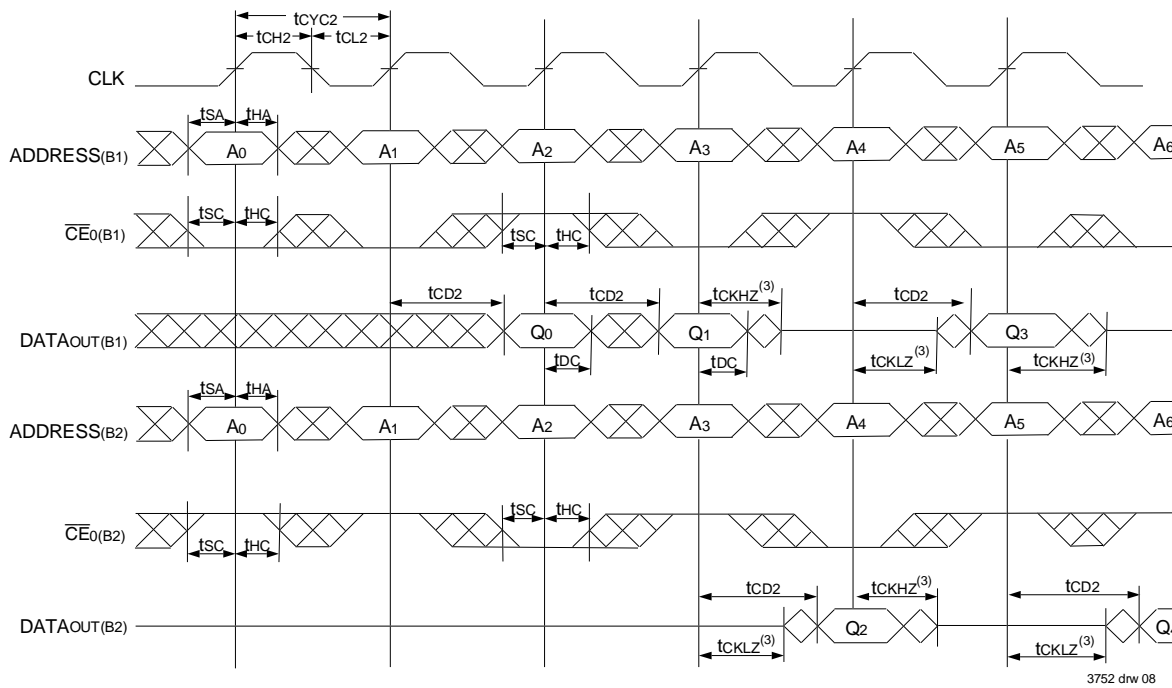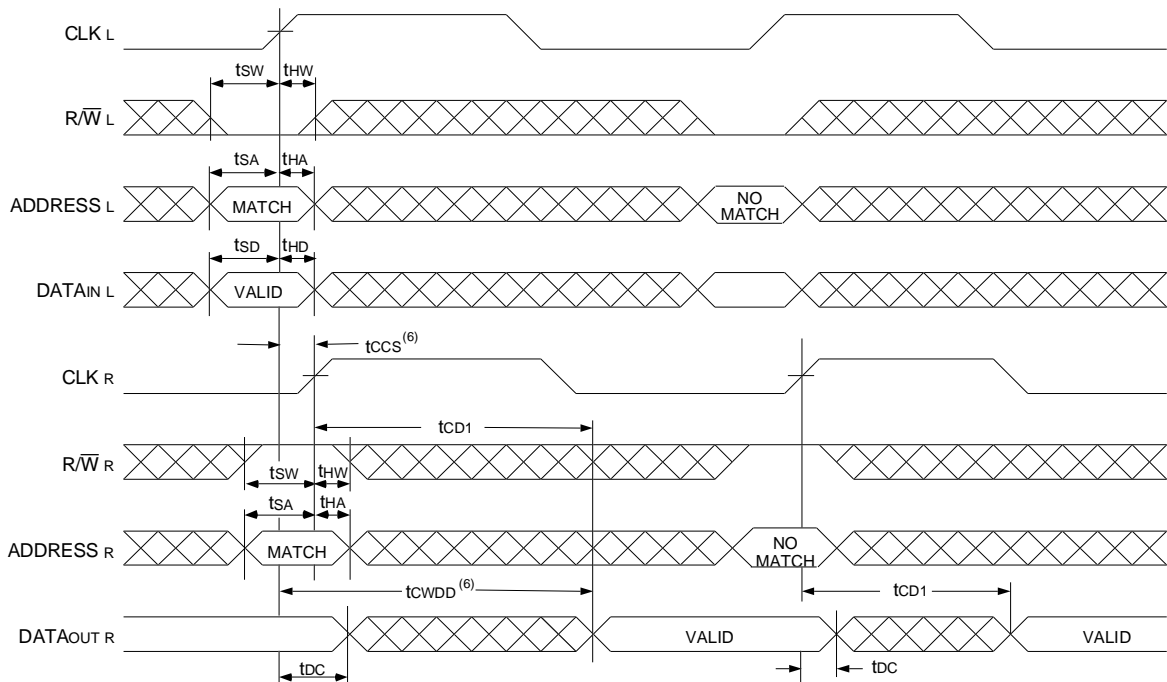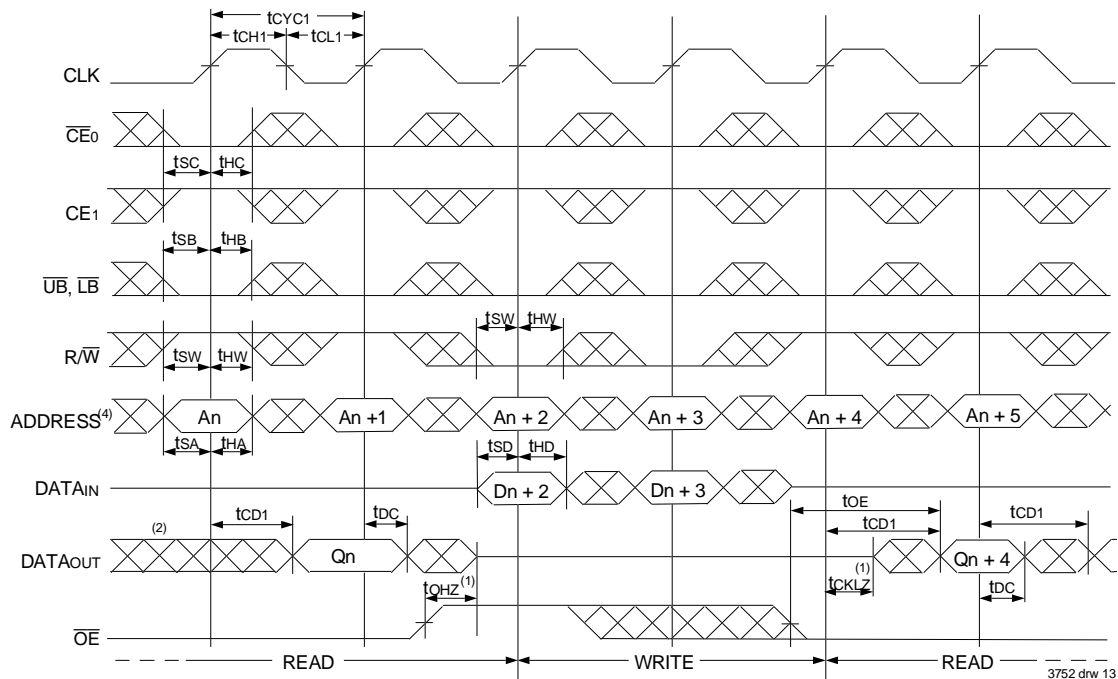

3752 drw 07

NOTES:
1. Transition is measured 0mV from Low or High-impedance voltage with the Output Test Load (Figure 2).
2. $\overline{OE}$ is asynchronously controlled; all other inputs are synchronous to the rising clock edge.
3. $\overline{ADS}$ = V_{IL}, $\overline{CNTEN}$ and $\overline{CNTRST}$ = V_{IH}.
4. The output is disabled (High-Impedance state) by $\overline{CE}_0$ = V_{IH}, CE1 = V_{IL}, $\overline{UB}$ = V_{IH}, or $\overline{LB}$ = V_{IH} following the next rising edge of the clock. Refer to Truth Table 1.
5. Addresses do not have to be accessed sequentially since $\overline{ADS}$ = V_{IL} constantly loads the address on the rising edge of the CLK; numbers are for reference use only.
6. If $\overline{UB}$ or $\overline{LB}$ was HIGH, then the Upper Byte and/or Lower Byte of DATA$_{OUT}$ for Qn + 2 would be disabled (High-Impedance state).

Timing Waveform of a Multi-device Pipelined Read[1,2]

3752 drw 08

Timing Waveform of Left Port Write to Flow-through Right Port Read[4,5]

3752 drw 09

NOTES:
1. B1 Represents Device #1; B2 Represents Device #2. Each Device consists of one IDT70V9269 for this waveform, and are setup for depth expansion in this example. ADDRESS(B1) = ADDRESS(B2) in this situation.
2. $\overline{UB}$, $\overline{LB}$, $\overline{OE}$, and $\overline{ADS}$ = V_IL; CE1(B1), CE1(B2), R/$\overline{W}$, $\overline{CNTEN}$, and $\overline{CNTRST}$ = V_IH.
3. Transition is measured 0mV from Low or High-Impedance voltage with the Output Test Load (Figure 2).
4. $\overline{CE}_0$, $\overline{UB}$, $\overline{LB}$, and $\overline{ADS}$ = V_IL; CE1, $\overline{CNTEN}$, and $\overline{CNTRST}$ = V_IH.
5. $\overline{OE}$ = V_IL for the Right Port, which is being read from. $\overline{OE}$ = V_IH for the Left Port, which is being written to.
6. If tCCS ≤ maximum specified, then data from right port READ is not valid until the maximum specified for tCWDD.
   If tCCS > maximum specified, then data from right port READ is not valid until tCCS + tCD1. tCWDD does not apply in this case.

Timing Waveform of Pipelined Read-to-Write-to-Read ($\overline{OE}$ = V_{IL})[3]
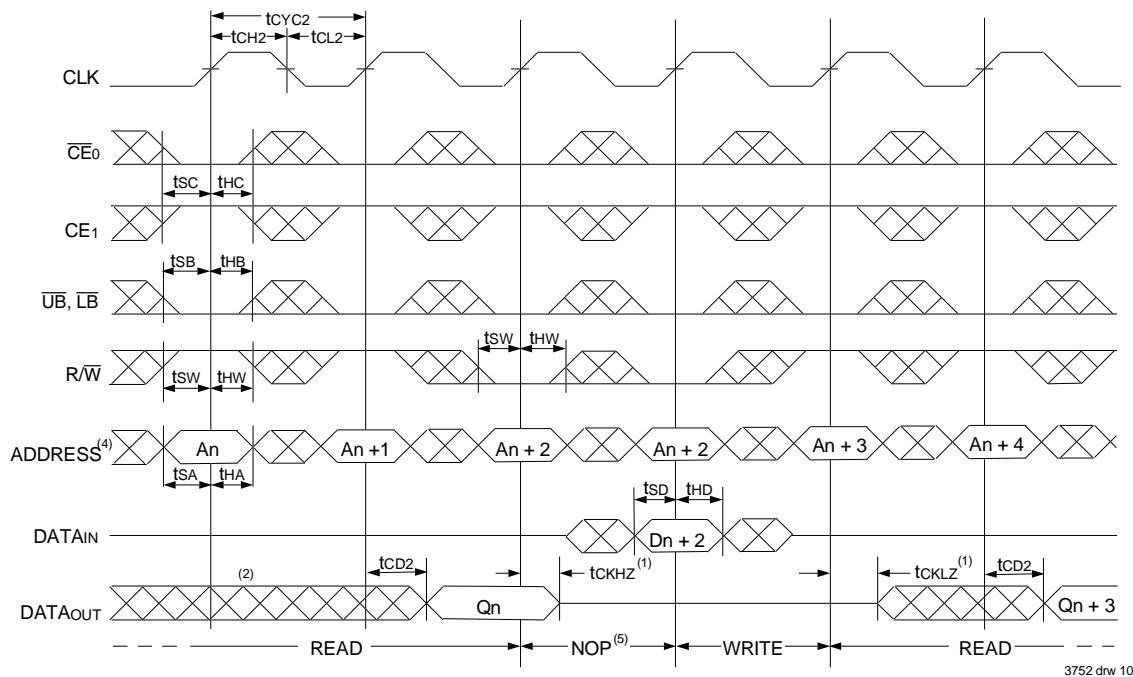
3752 drw 10

Timing Waveform of Pipelined Read-to-Write-to-Read ($\overline{OE}$ Controlled)[3]


3752 drw 11
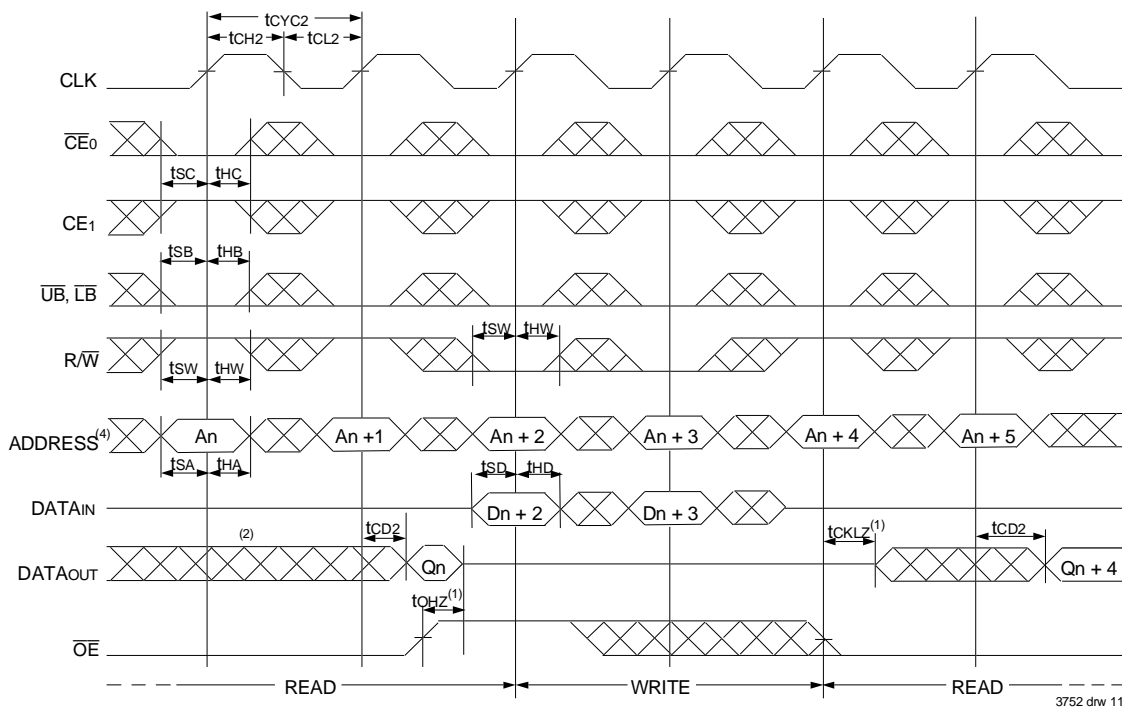
NOTES:
1. Transition is measured 0mV from Low or High-impedance voltage with the Output Test Load (Figure 2).
2. Output state (High, Low, or High-impedance) is determined by the previous cycle control signals.
3. $\overline{CE_0}$, $\overline{UB}$, $\overline{LB}$, and $\overline{ADS}$ = V_{IL}; CE_1, $\overline{CNTEN}$, and $\overline{CNTRST}$ = V_{IH}. "NOP" is "No Operation".
4. Addresses do not have to be accessed sequentially since ADS = V_{IL} constantly loads the address on the rising edge of the CLK; numbers are for reference use only.
5. "NOP" is "No Operation." Data in memory at the selected address may be corrupted and should be re-written to guarantee data integrity.

Timing Waveform of Flow-through Read-to-Write-to-Read ($\overline{OE}$ = V$_{IL}$)[3]

3752 drw 12
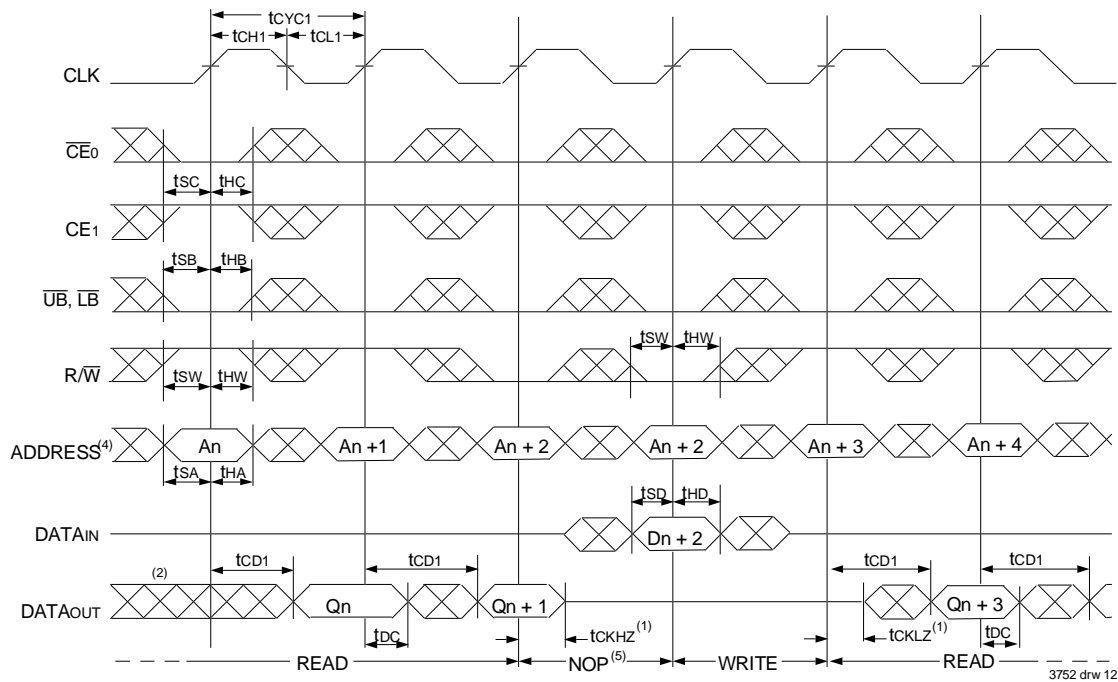
Timing Waveform of Flow-through Read-to-Write-to-Read ($\overline{OE}$ Controlled)[3]

3752 drw 13

NOTES:
1. Transition is measured 0mV from Low or High-impedance voltage with the Output Test Load (Figure 2).
2. Output state (High, Low, or HIgh-impedance) is determined by the previous cycle control signals.
3. $\overline{CE0}$, $\overline{UB}$, $\overline{LB}$, and $\overline{ADS}$ = V$_{IL}$; CE1, $\overline{CNTEN}$, and $\overline{CNTRST}$ = V$_{IH}$.
4. Addresses do not have to be accessed sequentially since $\overline{ADS}$ = V$_{IL}$ constantly loads the address on the rising edge of the CLK; numbers are for reference use only.
5. "NOP" is "No Operation." Data in memory at the selected address may be corrupted and should be re-written to guarantee data integrity.

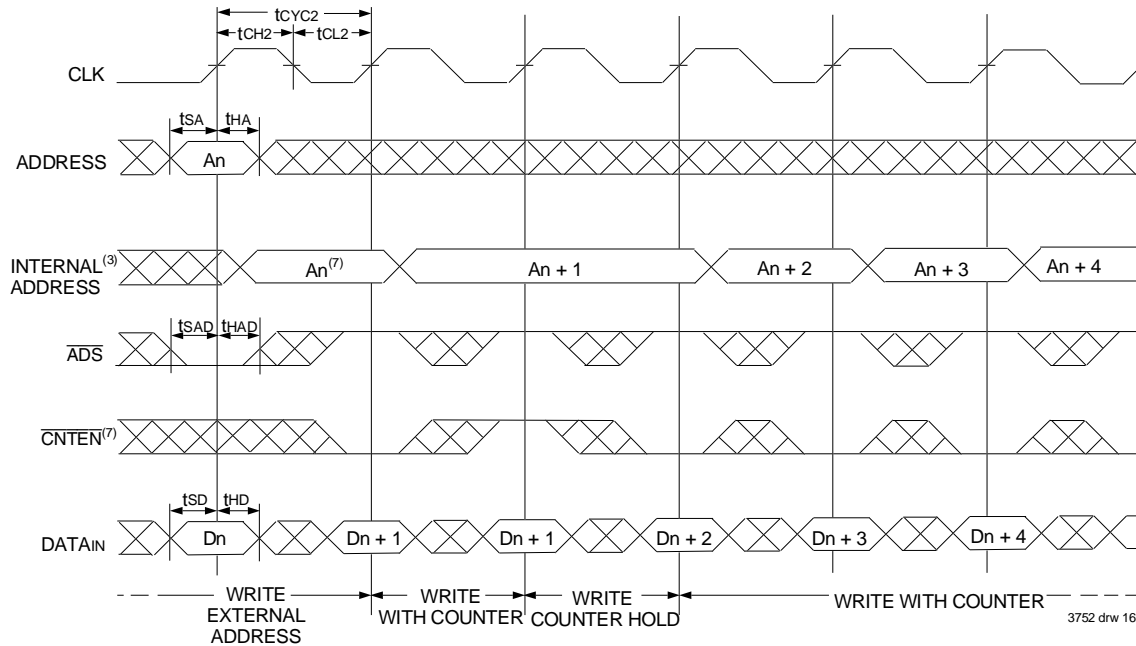# Timing Waveform of Pipelined Read with Address Counter Advance[(1)]

3752 drw 14
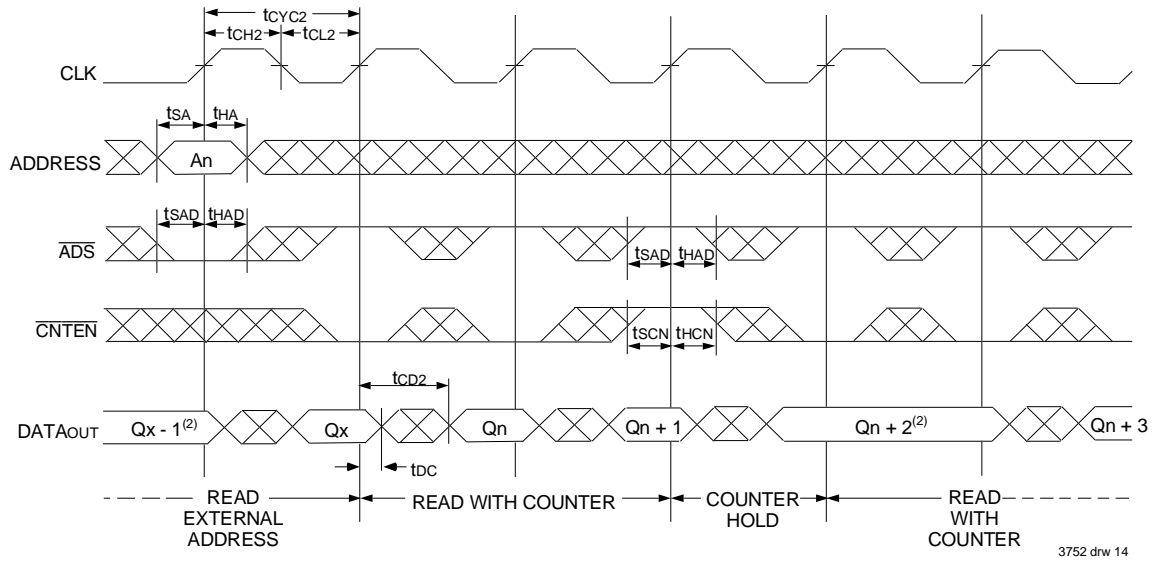
Timing Waveform of Flow-through Read with Address Counter Advance[(1)]

3752 drw 15
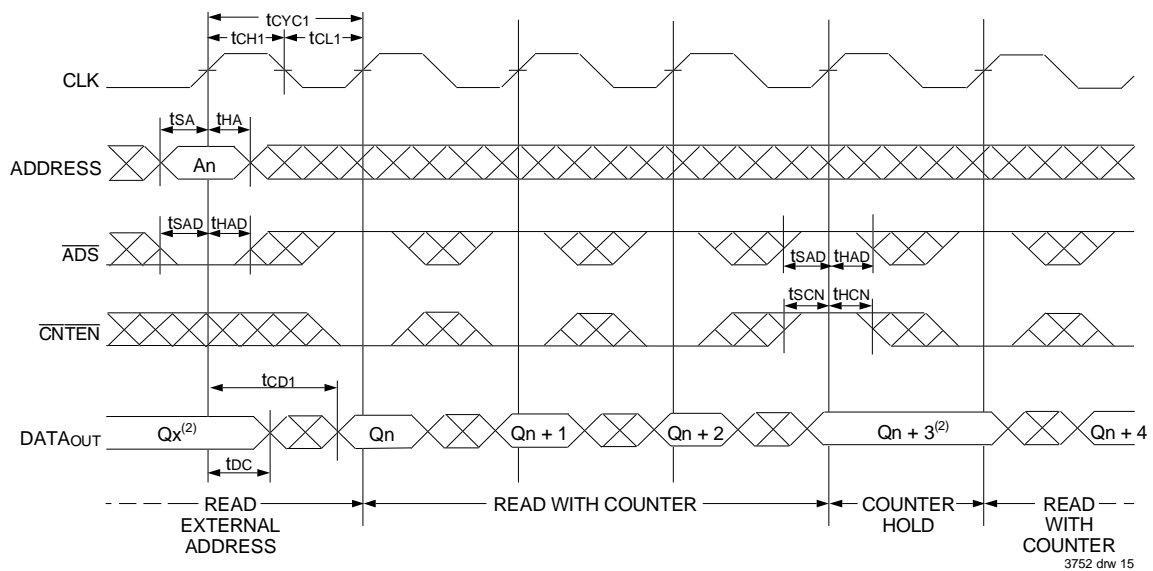
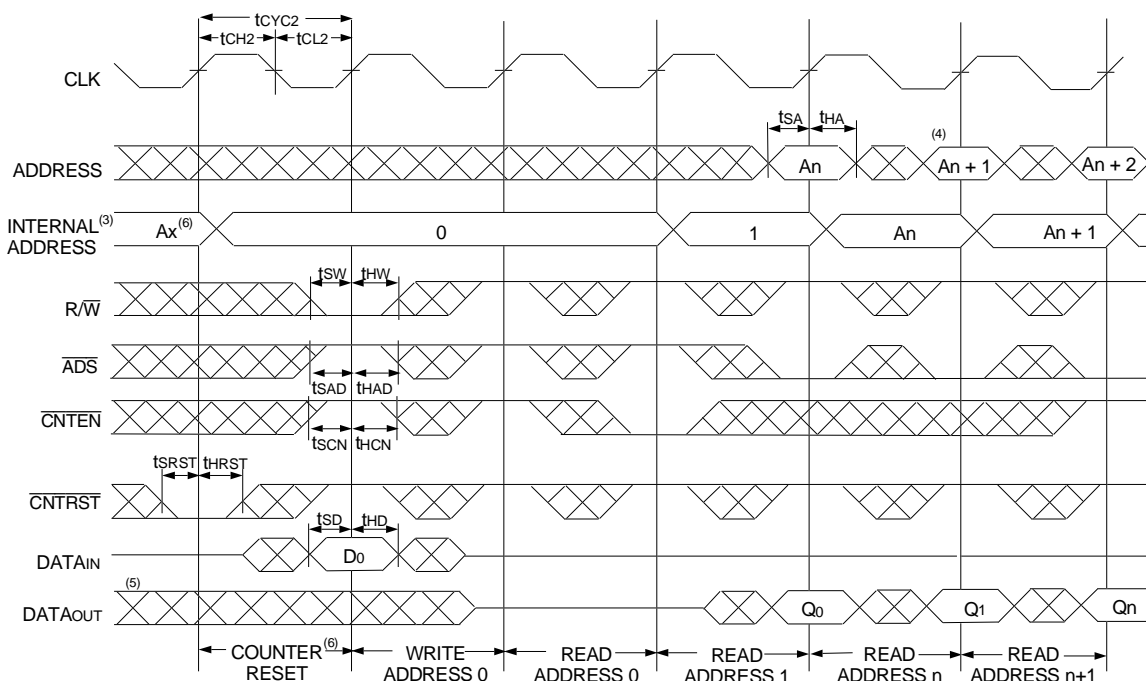**NOTES:**
1. $\overline{CE}_0$, $\overline{OE}$, $\overline{UB}$, and $\overline{LB}$ = V_{IL}; CE_1, $R/\overline{W}$, and $\overline{CNTRST}$ = V_{IH}.
2. If there is no address change via $\overline{ADS}$ = V_{IL} (loading a new address) or $\overline{CNTEN}$ = V_{IL} (advancing the address, i.e. $\overline{ADS}$ = V_{IH} and $\overline{CNTEN}$ = V_{IH}, then the data output remains constant for subsequent clocks.

Timing Waveform of Write with Address Counter Advance (Flow-Through or Pipelined Outputs)[1]

3752 drw 16

Timing Waveform of Counter Reset (Pipelined Outputs)[2]

3752 drw 17

NOTES:
1. $\overline{CE}_0$, $\overline{UB}$, $\overline{LB}$, and R/$\overline{W}$ = V$_{IL}$; CE1 and $\overline{CNTRST}$ = V$_{IH}$.
2. $\overline{CE}_0$, $\overline{UB}$, $\overline{LB}$ = V$_{IL}$; CE1 = V$_{IH}$.
3. The "Internal Address" is equal to the "External Address" when $\overline{ADS}$ = V$_{IL}$ and equals the counter output when $\overline{ADS}$ = V$_{IH}$.
4. Addresses do not have to be accessed sequentially since $\overline{ADS}$ = V$_{IL}$ constantly loads the address on the rising edge of the CLK; numbers are for reference use only.
5. Output state (High, Low, or High-impedance) is determined by the previous cycle control signals.
6. No dead cycle exists during counter reset. A READ or WRITE cycle may be coincidental with the counter reset cycle. ADDR0 will be accessed. Extra cycles are shown here simply for clarification.
7. $\overline{CNTEN}$ = V$_{IL}$ advances Internal Address from 'An' to 'An + 1'. The transition show indicates the time required for the counter to advance. The 'An +1' Address is written to during this cycle.

Functional Description

The IDT70V9269 provides a true synchronous Dual-Port Static RAM interface. Registered inputs provide minimal set-up and hold times on address, data, and all critical control inputs. All internal registers are clocked on the rising edge of the clock signal, however, the self-timed internal write pulse is independent of the LOW to HIGH transition of the clock signal.

An asynchronous output enable is provided to ease asynchronous bus interfacing. Counter enable inputs are also provided to stall the operation of the address counters for fast interleaved memory applications.

A HIGH on $\overline{CE}_0$ or a LOW on CE_1 for one clock cycle will power down the internal circuitry to reduce static power consumption. Multiple Chip Enables allow easier banking of multiple IDT70V9269's for depth expansion configurations. When the Pipelined output mode is enabled, two cycles are required with $\overline{CE}_0$ LOW and CE_1 HIGH to re-activate the outputs.

Depth and Width Expansion

The IDT70V9269 features dual chip enables (refer to Truth Table 1) in order to facilitate rapid and simple depth expansion with no requirements for external logic. Figure 4 illustrates how to control the various chip enables in order to expand two devices in depth.

The IDT70V9269 can also be used in applications requiring expanded width, as indicated in Figure 4. Since the banks are allocated at the discretion of the user, the external controller can be set up to drive the input signals for the various devices as required to allow for 32-bit or wider applications.
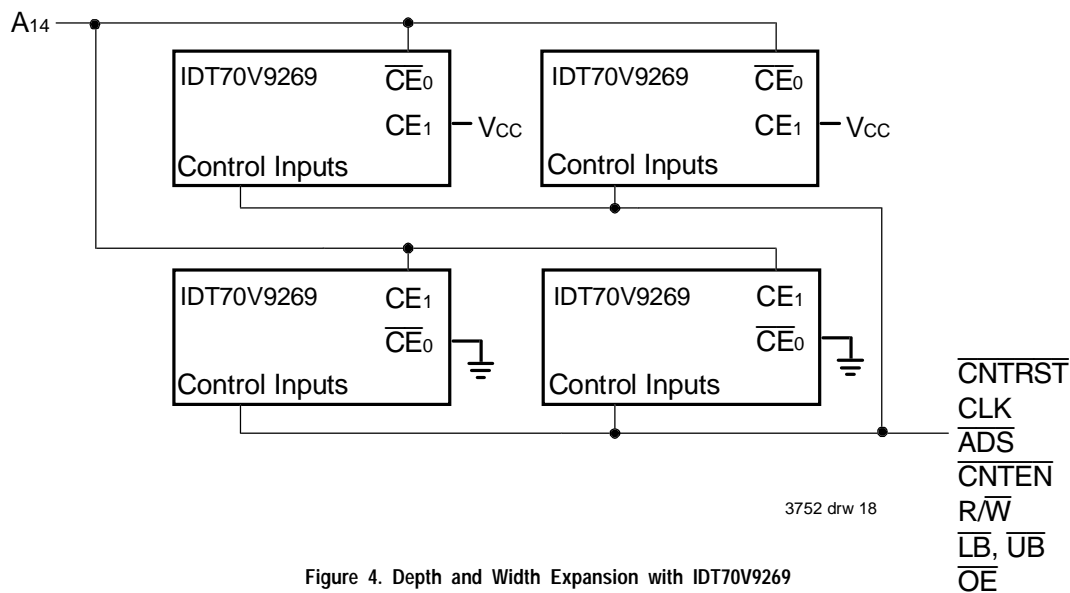

3752 drw 18

Figure 4. Depth and Width Expansion with IDT70V9269

Ordering Information

```
IDT   XXXXX     A      99      A        A
      Device   Power  Speed  Package  Process/
      Type                            Temperature
                                      Range
```

Blank	Commercial (0°C to +70°C)
I [1]	Industrial (-40°C to +85°C)

PRF	128-pin TQFP (PK128-1)

9	Commercial Only	
12	Commercial Only	Speed in nanoseconds
15	Commercial Only	

S	Standard Power
L	Low Power

70V9269	256K (16K x 16-Bit) Synchronous Dual-Port RAM

3752 drw 19

NOTE:
1. Industrial temperature range is available.
   For specific speeds, packages and powers contact your sales office.

Datasheet Document History

1/12/99:	Initiated datasheet document history
	Converted to new format
	Cosmetic and typographical corrections
	Added additional notes to pin configurations
	Page 14 Added Depth and Width Expansion section
6/15/99:	Page 4 Deleted note 6 for Table II
8/20/99:	Fixed Pin Configuration
4/4/00:	Replaced IDT logo
	Added $\overline{FT}$/PIPE to left port
	Changed ±200mV to 0mV in notes
1/17/01:	Page 4 Changed information in Truth Table II
	Increased storage temperature parameters
	Clarified TA parameter
	Page 5 DC Electrical parameters–changed wording from "open" to "disabled"
	Removed Preliminary status