

RIC7113E4

RADIATION HARDENED HIGH AND LOW SIDE GATE DRIVER

Features

- Total dose capability to 100K Rad (Si)
- Floating channel designed for bootstrap operation
- Fully operational to +400V
- Tolerant to negative transient voltage
- dV/dt immune
- Gate drive supply range from 10 to 20V
- Undervoltage lockout for both channels
- Separate logic supply range from 5 to 20V
Logic and power ground $\pm 5V$ offset
- CMOS Schmitt-triggered inputs with pull-down
- Cycle by cycle edge-triggered shutdown logic
- Matched propagation delay for both channels
- Outputs in phase with inputs
- Hermetically Sealed
- Lightweight

Product Summary

V_{OFFSET}	400V max.
I_{O+/-}	2A / 2A
V_{OUT}	10 - 20V
t_{on/off} (typ.)	120 & 100 ns
Delay Matching(typ.)	5 ns

Description

The RIC7113E4 is a high voltage, high speed power MOSFET and IGBT driver with independent high and low side referenced output channels. Proprietary HVIC and latch immune CMOS technologies enable ruggedized monolithic construction. Logic inputs are compatible with standard CMOS or LSTTL outputs. The output drivers feature a high pulse current buffer stage designed for minimum driver cross-conduction. Propagation delays are matched to simplify use in high frequency applications. The floating channel can be used to drive an N-channel power MOSFET or IGBT in the high side configuration which operates up to 400 volts.

Absolute Maximum Ratings

Absolute Maximum Ratings indicate sustained limits beyond which damage to the device may occur. All voltage parameters are absolute voltages referenced to COM. The Thermal Resistance and Power Dissipation ratings are measured under board mounted and still air conditions.

Symbol	Parameter	Min.	Max.	Units
V _B	High Side Floating Supply Voltage	-0.5	V _S + 20	V
V _S	High Side Floating Supply Offset Voltage	—	400	
V _{HO}	High Side Floating Output Voltage	V _S - 0.5	V _B + 0.5	
V _{CC}	Low Side Fixed Supply Voltage	-0.5	20	
V _{LO}	Low Side Output Voltage	-0.5	V _{CC} + 0.5	
V _{DD}	Logic Supply Voltage	-0.5	V _{SS} + 20	
V _{SS}	Logic Supply Offset Voltage	V _{CC} - 20	V _{CC} + 0.5	
V _{IN}	Logic Input Voltage (HIN, LIN & SD)	V _{SS} - 0.5	V _{DD} + 0.5	
dV _S /dt	Allowable Offset Supply Voltage Transient (Figure 2)	—	50	V/ns
P _D	Package Power Dissipation @ T _A ≤ +25°C	—	1.6	W
R _{thJA}	Thermal Resistance, Junction to Ambient	—	125	°C/W
T _J	Junction Temperature	-55	125	°C
T _S	Storage Temperature	-55	150	
T _L	Lead Temperature (Soldering, 10 seconds)	—	300	
	Weight	0.42 (typical)		g

Recommended Operating Conditions

The Input/Output logic timing diagram is shown in Figure 1. The VS and VSS offset ratings are tested with all supplies biased at 15V differential.

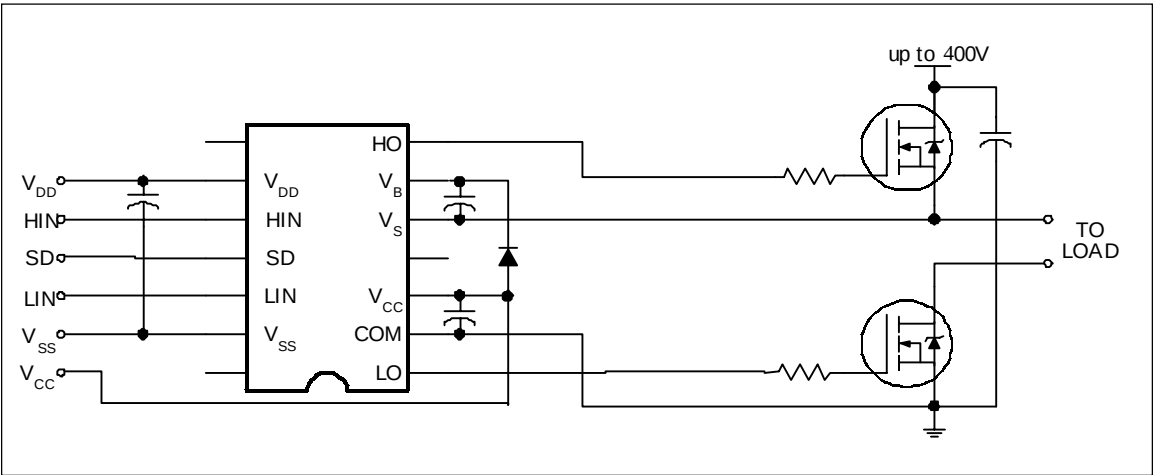
Symbol	Parameter	Min.	Max.	Units
VB	High Side Floating Supply Absolute Voltage	VS + 10	VS + 20	V
VS	High Side Floating Supply Offset Voltage	-4	400	
VHO	High Side Floating Output Voltage	VS	VB	
VCC	Low Side Fixed Supply Voltage	10	20	
VLO	Low Side Output Voltage	0	VCC	
VDD	Logic Supply Voltage	VSS + 5	VSS + 20	
VSS	Logic Supply Offset Voltage	-5	5	
VIN	Logic Input Voltage (HIN, LIN & SD)	VSS	VDD	

Dynamic Electrical Characteristics

VBIAS (VCC, VBS, VDD) = 15V, and VSS = COM unless otherwise specified. The dynamic electrical characteristics are measured using the test circuit shown in Figure 3.

Symbol	Parameter	Tj = 25°C			Tj = -55 to 125°C		Units	Test Conditions
		Min.	Typ.	Max.	Min.	Max.		
t _{on}	Turn-On Propagation Delay	—	120	150	—	260	ns	VS = 0V
t _{off}	Turn-Off Propagation Delay	—	100	125	—	220		VS = 400V
t _{sd}	Shutdown Propagation Delay	—	110	140	—	235		VS = 400V
t _r	Turn-On Rise Time	—	25	35	—	50		CL = 1000pf
t _f	Turn-Off Fall Time	—	17	25	—	40		CL = 1000pf
MT	Delay Matching, HS & LS Turn-On/Off	—	5	20	—	—		t _{ton} - t _{tonl} or t _{toff} - t _{toffl}

Typical Connection



Static Electrical Characteristics

V_{BIAS} (V_{CC}, V_{BS}, V_{DD}) = 15V, unless otherwise specified. The V_{IN}, V_{TH} and I_{IN} parameters are referenced to V_{SS} and are applicable to all three logic input pins: HIN, LIN and SD. The V_O and I_O parameters are referenced to COM or V_S and are applicable to the respective output pins: HO or LO.

Symbol	Parameter	T _j = 25°C		T _j = -55 to 125°C		Units	Test Conditions
		Min.	Typ.	Min.	Max.		
V _{IH}	Logic "1" Input Voltage	3.1	—	3.3	—	V	V _{DD} = 5V
		6.4	—	6.8	—		V _{DD} = 10V
		9.5	—	10	—		V _{DD} = 15V
		12.5	—	13.3	—		V _{DD} = 20V
V _{IL}	Logic "0" Input Voltage	—	1.8	—	1.7	V	V _{DD} = 5V
		—	3.8	—	3.6		V _{DD} = 10V
		—	6.0	—	5.7		V _{DD} = 15V
		—	8.3	—	7.9		V _{DD} = 20V
V _{OH}	High Level Output Voltage, V _{BIAS} - V _O	—	1.2	—	1.5	μA	V _{IN} = V _{IH} , I _O = 0A
V _{OL}	Low Level Output Voltage, V _O	—	0.1	—	0.1		V _{IN} = V _{IH} , I _O = 0A
I _{LK}	Offset Supply Leakage Current	—	50	—	250		V _B = V _S = 400V
I _{QBS}	Quiescent V _{BS} Supply Current	—	230	—	500		V _{IN} = 0V, or V _{DD}
I _{QCC}	Quiescent V _{CC} Supply Current	—	340	—	600	μA	V _{IN} = 0V, or V _{DD}
I _{QDD}	Quiescent V _{DD} Supply Current	—	30	—	60		V _{IN} = 0V, or V _{DD}
I _{IN+}	Logic "1" Input Bias Current	—	40	—	70		V _{IN} = V _{DD}
I _{IN-}	Logic "0" Input Bias Current	—	1.0	—	10		V _{IN} = 0V
V _{BSUV+}	V _{BS} Supply Undervoltage Positive Going Threshold	7.5	9.7	—	—	V	
V _{BSUV-}	V _{BS} Supply Undervoltage Negative Going Threshold	7.0	9.4	—	—		
V _{CCUV+}	V _{CC} Supply Undervoltage Positive Going Threshold	7.4	9.6	—	—		
V _{CCUV-}	V _{CC} Supply Undervoltage Negative Going Threshold	7.0	9.4	—	—		
I _{O+}	Output High Short Circuit Pulsed Current	2.0	—	—	—	A	V _O = 0V, V _{IN} = V _{DD} PW ≤ 10 μs
I _{O-}	Output Low Short Circuit Pulsed Current	2.0	—	—	—		V _O = 15V, V _{IN} = 0V PW ≤ 10 μs

Radiation Performance

International Rectifier Radiation Hardened gate drivers are tested to verify their hardness capability. The hardness assurance program at International rectifier uses a Cobalt-60 (^{60}Co) source and heavy ion irradiation.

Every wafer shall be tested per MIL-STD-883, Method 1019, test condition A "Ionizing Radiation (Total Dose) Test Procedure".

Both pre- and post- irradiation performances are tested and specified using the same drive circuitry and test conditions to provide a direct comparison.

For Static Irradiation Test Conditions refer to figure 7.

Static Electrical Characteristics		T _j = 25°C			
Symbol	Parameter	100K Rads (Si)		Units	Test Conditions
		Min	Max		
V _{IH}	Logic “1” Input Voltage	3.1	—	V	VDD = 5V
		6.4	—		VDD = 10V
		9.5	—		VDD = 15V
		12.5	—		VDD = 20V
V _{IL}	Logic “0” Input Voltage	—	1.8	V	VDD = 5V
		—	3.8		VDD = 10V
			6.0		VDD = 15V
		—	8.3		VDD = 20V
V _{OH}	High Level Output Voltage, V _{BIAS} - V _O	—	1.2		V _{IN} =V _{IH} , I _O = 0A
V _{OL}	Low Level Output Voltage, V _O	—	0.1		V _{IN} =V _{IH} , I _O = 0A
I _{LK}	Offset Supply Leakage Current	—	50	μA	VB =VS = 400A
I _{QBS}	Quiescent V _{BS} Supply Current	—	230		VIN =0V or VDD
I _{QCC}	Quiescent V _{CC} Supply Current	—	340		VIN =0V or VDD
I _{QDD}	Quiescent V _{DD} Supply Current	—	30		VIN =0V or VDD
I _{IN+}	Logic “1” Input Bias Current	—	40		VIN =VDD
I _{IN-}	Logic “0” Input Bias Current	—	1.0		VIN =0V
V _{BSUV+}	V _{BS} Supply Undervoltage Positive Going Threshold	7.5	9.7	V	
V _{BSUV-}	V _{BS} Supply Undervoltage Negative Going Threshold	7.0	9.4		
V _{CCUV+}	V _{CC} Supply Undervoltage Positive Going Threshold	7.4	9.6		
V _{CCUV-}	V _{CC} Supply Undervoltage Negative Going Threshold	7.0	9.4		
I _{O+}	Output High Short Circuit Pulsed Current	2.0	—	A	VO =0V, VIN =VDD PW ≤ 10 μs
I _{O-}	Output Low Short Circuit Pulsed Current	2.0	—		VO =15V, VIN =0V PW ≤ 10 μs

Radiation characteristics

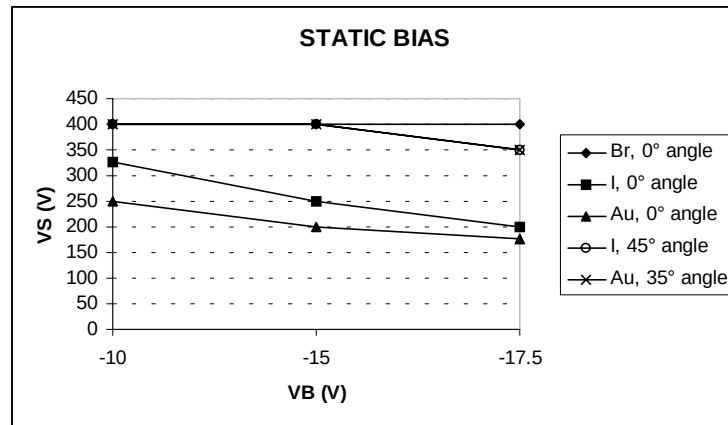
RIC7113E4

International Rectifier radiation hardened Gate Drivers have been characterized in heavy ion environment for Single Event Effects (SEE). Single Event Effects characterization data is illustrated below. For Static Bias Test Conditions refer to figure 8.

Single Event Effect Safe Operating Area

Ion	LET MeV/(mg/cm ²))	Energy (MeV)	Angle (degrees)	V _s (V)		
				@V _{BS} = -10V	@V _{BS} = -15V	@V _{BS} = -17.5V
Br	37	284	0	400	400	400
I	60	344	0	325	250	200
Au	82	346	0	250	200	175
I	85	344	45	400	400	350
Au	100	346	35	400	400	350

Note: VCC/VDD = 20V, except for LET=100, then VCC/VDD = 17.5V



Single Event Effect, Safe Operating Area

RIC7113E4

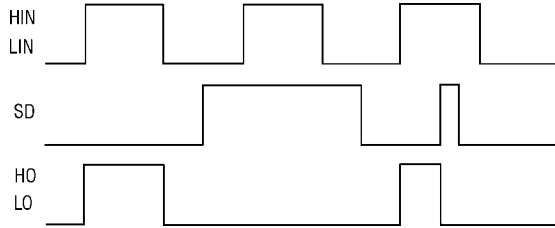


Figure 1. Input/Output Logic Timing Diagram

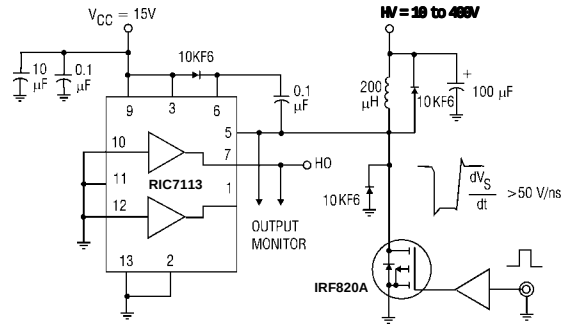


Figure 2. Floating Supply Voltage Transient Test Circuit

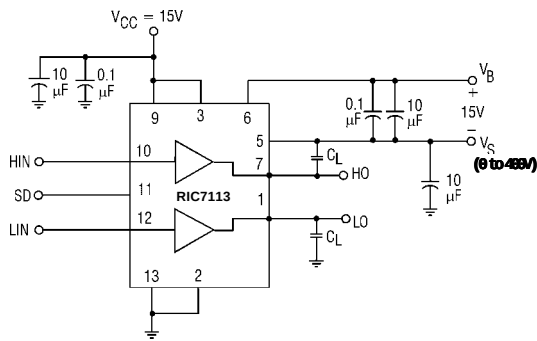


Figure 3. Switching Time Test Circuit

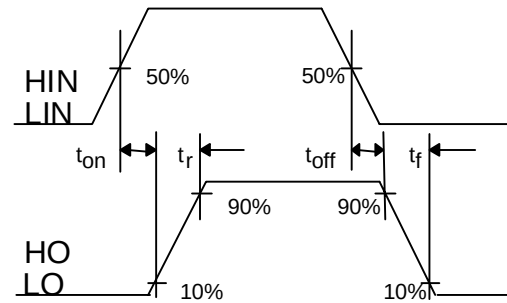


Figure 4. Switching Time Waveform Definition

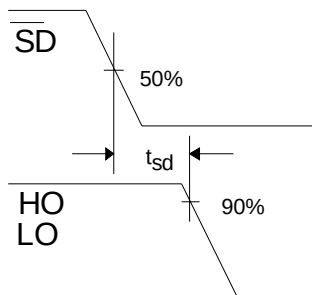


Figure 5. Shutdown Waveform Definitions

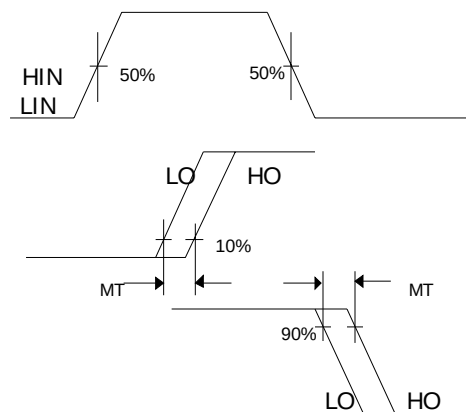


Figure 6. Delay Matching Waveform Definitions

RIC7113E4

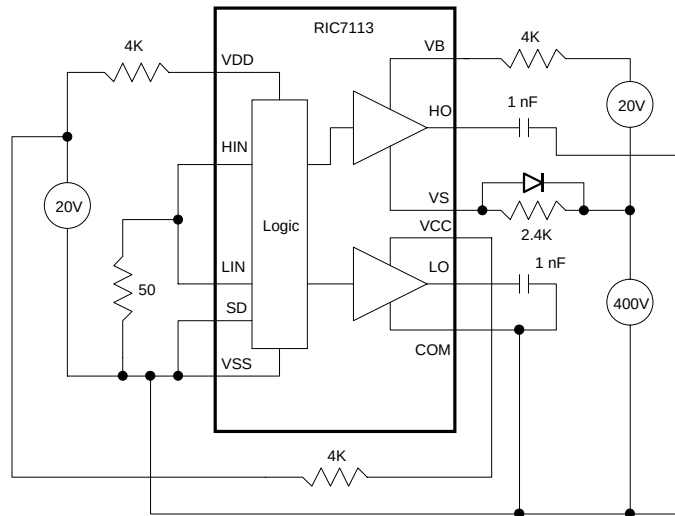


Figure 7. Static Bias Conditions for Total Ionizing Dose Test

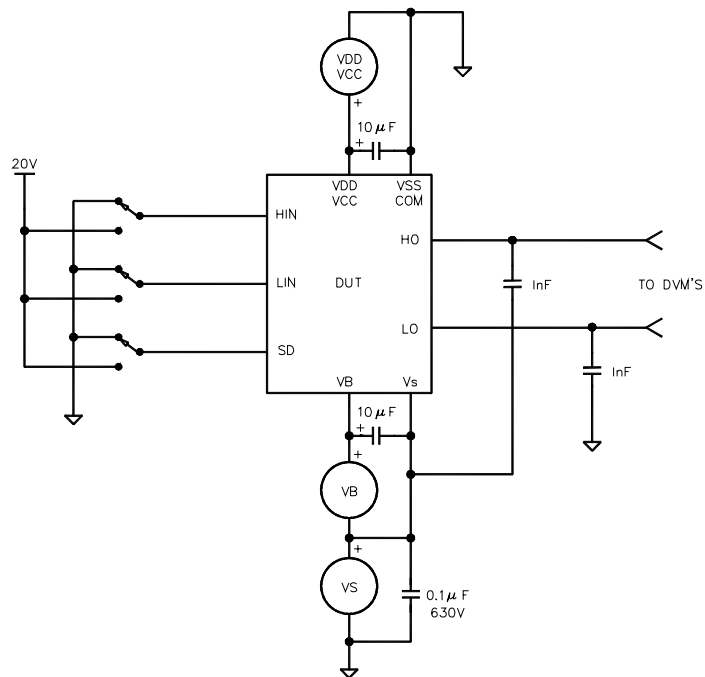
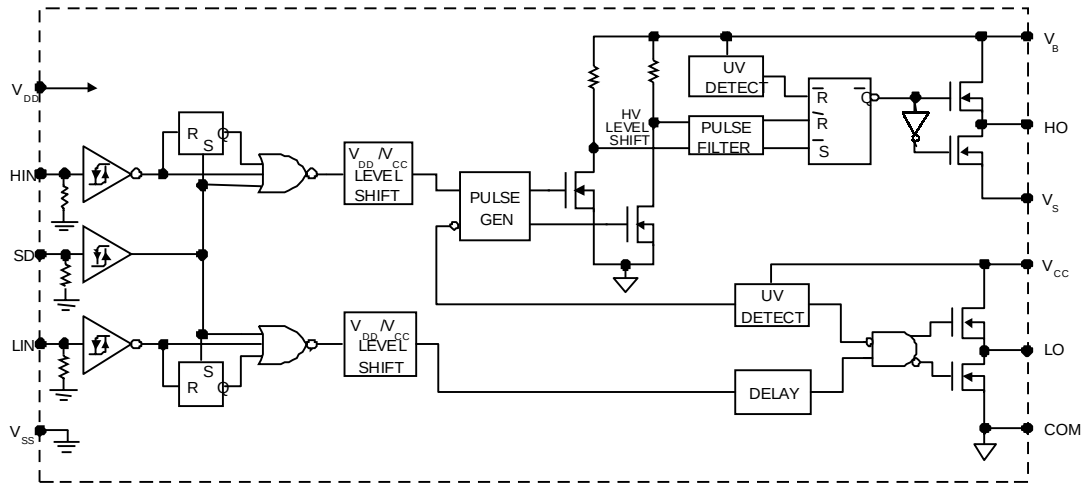


Figure 8. Static Bias Conditions for Single Event Effect Test

RIC7113E4

Functional Block Diagram

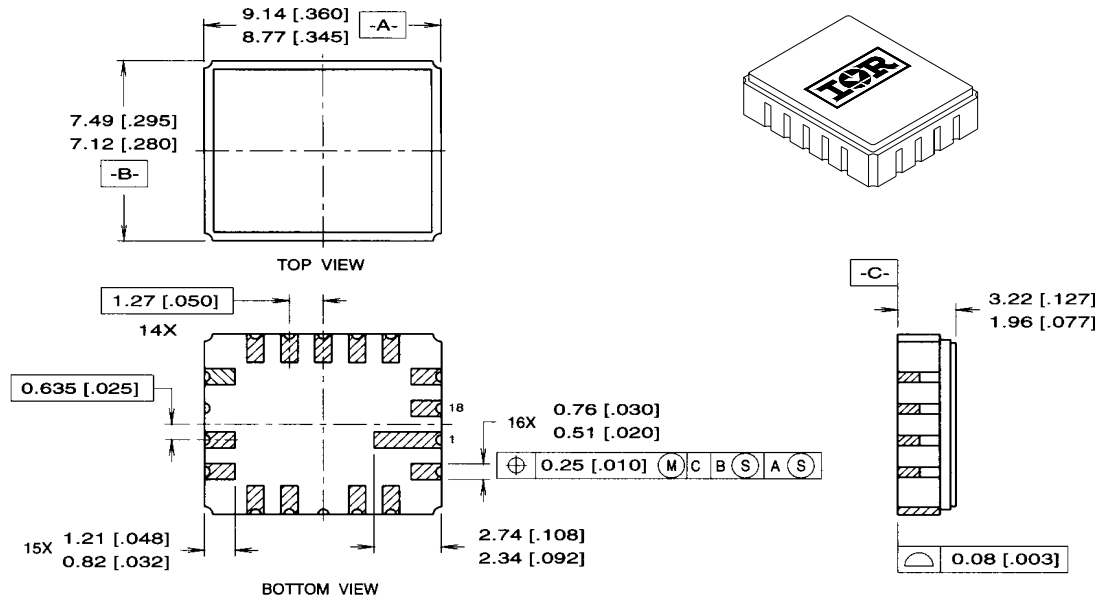


Lead Definitions

Lead	
Symbol	Description
V _{DD}	Logic supply
HIN	Logic input for high side gate driver output (HO), in phase
SD	Logic input for shutdown
LIN	Logic input for low side gate driver output (LO), in phase
V _{SS}	Logic ground
V _B	High side floating supply
HO	High side gate drive output
V _S	High side floating supply return
V _{CC}	Low side supply
LO	Low side gate drive output
COM	Low side return

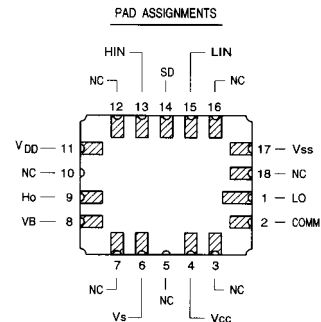
Case Outline and Dimensions — Leadless chip carrier (LCC) package

RIC7113E4



NOTES:

1. DIMENSIONING & TOLERANCING PER ANSI Y14.5M-1982.
2. CONTROLLING DIMENSION: INCH.
3. DIMENSIONS ARE SHOWN IN MILLIMETERS [INCHES].



International
IR Rectifier

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Data and specifications subject to change without notice. 5/00