International Rectifier

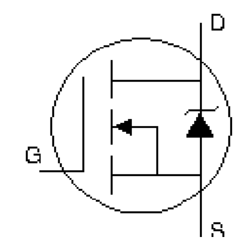
PD - ____

PRELIMINARY

IRLP2505

HEXFET® Power MOSFET

- Logic-Level Gate Drive
- Advanced Process Technology
- Ultra Low On-Resistance
- Dynamic dv/dt Rating
- 175°C Operating Temperature
- Fast Switching
- Fully Avalanche Rated



V_{DSS} = 55V

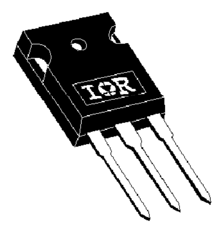
$R_{DS(on)}$ = 0.008Ω

I_D = 90A⑤

Description

Fifth Generation HEXFETs from International Rectifier utilize advanced processing techniques to achieve the lowest possible on-resistance per silicon area. This benefit, combined with the fast switching speed and ruggedized device design that HEXFET Power MOSFETs are well known for, provides the designer with an extremely efficient device for use in a wide variety of applications.

The TO-247 package is preferred for commercial-industrial applications where higher power levels preclude the use of TO-220 devices. The TO-247 is similar but superior to the earlier TO-218 package because of its isolated mounting hole.



TO-247AC

Absolute Maximum Ratings

	Parameter	Max.	Units
I_D @ T_C = 25°C	Continuous Drain Current, V_{GS} @ 10V	90⑤	A
I_D @ T_C = 100°C	Continuous Drain Current, V_{GS} @ 10V	64	
I_{DM}	Pulsed Drain Current ①	360	
P_D @T_C = 25°C	Power Dissipation	150	W
	Linear Derating Factor	1.0	W/°C
V_{GS}	Gate-to-Source Voltage	±20	V
E_{AS}	Single Pulse Avalanche Energy ②	500	mJ
I_{AR}	Avalanche Current①	54	A
E_{AR}	Repetitive Avalanche Energy①	15	mJ
dv/dt	Peak Diode Recovery dv/dt ③	2.9	V/ns
T_J T_{STG}	Operating Junction and Storage Temperature Range	-55 to + 175	°C
	Soldering Temperature, for 10 seconds	300 (1.6mm from case)	
	Mounting torque, 6-32 or M3 screw.	10 lbf•in (1.1N•m)	

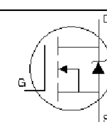
Thermal Resistance

	Parameter	Min.	Typ.	Max.	Units
$R_{\theta JC}$	Junction-to-Case	——	——	1.0	°C/W
$R_{\theta CS}$	Case-to-Sink, Flat, Greased Surface	——	0.24	——	
$R_{\theta JA}$	Junction-to-Ambient	——	——	40	

Electrical Characteristics @ T_J = 25°C (unless otherwise specified)

	Parameter	Min.	Typ.	Max.	Units	Conditions
$V_{(BR)DSS}$	Drain-to-Source Breakdown Voltage	55	——	——	V	V_{GS} = 0V, I_D = 250µA
$\Delta V_{(BR)DSS}/\Delta T_J$	Breakdown Voltage Temp. Coefficient	——	0.035	——	V/°C	Reference to 25°C, I_D = 1mA
$R_{DS(on)}$	Static Drain-to-Source On-Resistance	——	——	0.008	Ω	V_{GS} = 10V, I_D = 54A ④
		——	——	0.010		V_{GS} = 5.0V, I_D = 54A ④
		——	——	0.013		V_{GS} = 4.0V, I_D = 45A ④
$V_{GS(th)}$	Gate Threshold Voltage	1.0	——	2.0	V	V_{DS} = V_{GS}, I_D = 250µA
g_{fs}	Forward Transconductance	59	——	——	S	V_{DS} = 25V, I_D = 54A
I_{DSS}	Drain-to-Source Leakage Current	——	——	25	µA	V_{DS} = 55V, V_{GS} = 0V
		——	——	250		V_{DS} = 44V, V_{GS} = 0V, T_J = 150°C
I_{GSS}	Gate-to-Source Forward Leakage	——	——	100	nA	V_{GS} = 20V
	Gate-to-Source Reverse Leakage	——	——	-100		V_{GS} = -20V
Q_g	Total Gate Charge	——	——	130	nC	I_D = 54A
Q_{gs}	Gate-to-Source Charge	——	——	25		V_{DS} = 44V
Q_{gd}	Gate-to-Drain ("Miller") Charge	——	——	67		V_{GS} = 5.0V, See Fig. 6 and 13 ④
$t_{d(on)}$	Turn-On Delay Time	——	12	——	ns	V_{DD} = 28V
t_r	Rise Time	——	160	——		I_D = 54A
$t_{d(off)}$	Turn-Off Delay Time	——	43	——		R_G = 1.3Ω, V_{GS} = 5.0V
t_f	Fall Time		84			R_D = 0.50Ω, See Fig. 10 ④
L_D	Internal Drain Inductance	——	5.0	——	nH	Between lead, 6mm (0.25in.) 
L_S	Internal Source Inductance	——	13	——		from package and center of die contact
C_{iss}	Input Capacitance	——	5000	——	pF	V_{GS} = 0V
C_{oss}	Output Capacitance	——	1100	——		V_{DS} = 25V
C_{rss}	Reverse Transfer Capacitance	——	390	——		f = 1.0MHz, See Fig. 5

Source-Drain Ratings and Characteristics

	Parameter	Min.	Typ.	Max.	Units	Conditions
I_S	Continuous Source Current (Body Diode)	——	——	90⑤	A	MOSFET symbol showing the 
I_{SM}	Pulsed Source Current (Body Diode) ①	——	——	360		integral reverse p-n junction diode.
V_{SD}	Diode Forward Voltage	——	——	1.3	V	T_J = 25°C, I_S = 54A, V_{GS} = 0V ④
t_{rr}	Reverse Recovery Time	——	140	210	ns	T_J = 25°C, I_F = 54A
Q_{rr}	Reverse Recovery Charge	——	650	970	nC	di/dt = 100A/µs ④

Notes:

① Repetitive rating; pulse width limited by max. junction temperature. (See fig. 11)

② V_{DD} = 25V, starting T_J = 25°C, L = 240µH R_G = 25Ω, I_{AS} = 54A. (See Figure 12)

③ $I_{SD} \le$ 54A, di/dt $\le$ 130A/µs, $V_{DD} \le V_{(BR)DSS}$, $T_J \le$ 175°C

④ Pulse width $\le$ 300µs; duty cycle $\le$ 2%.

⑤ Caculated continuous current based on maximum allowable junction temperature;for recommended current-handling of the package refer to Design Tip # 93-4

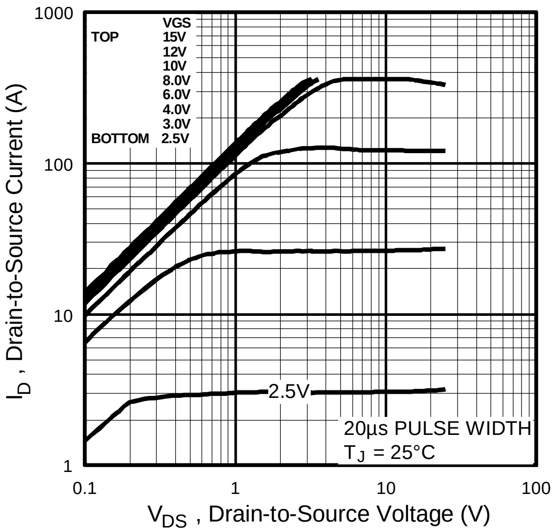


Fig 1. Typical Output Characteristics, $T_J = 25^oC$

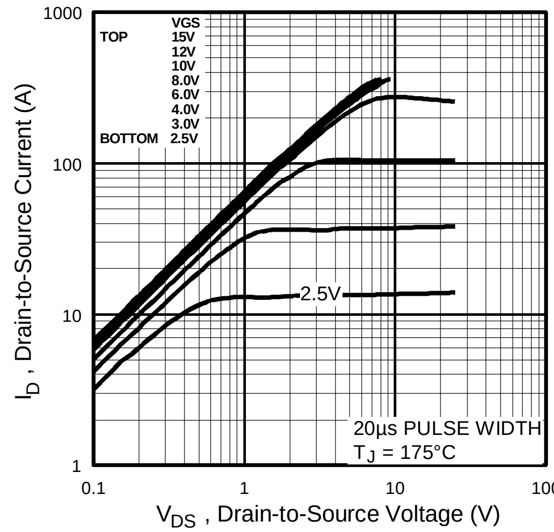


Fig 2. Typical Output Characteristics, $T_J = 175^oC$

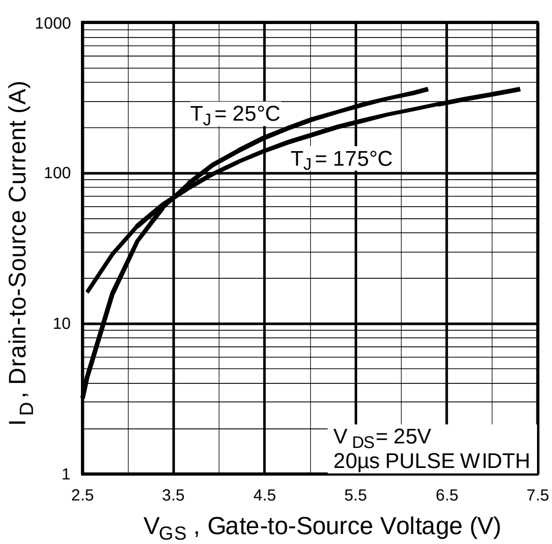


Fig 3. Typical Transfer Characteristics

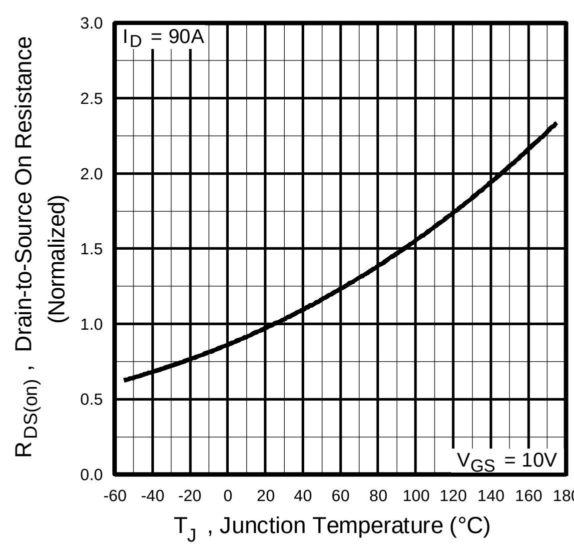


Fig 4. Normalized On-Resistance Vs. Temperature

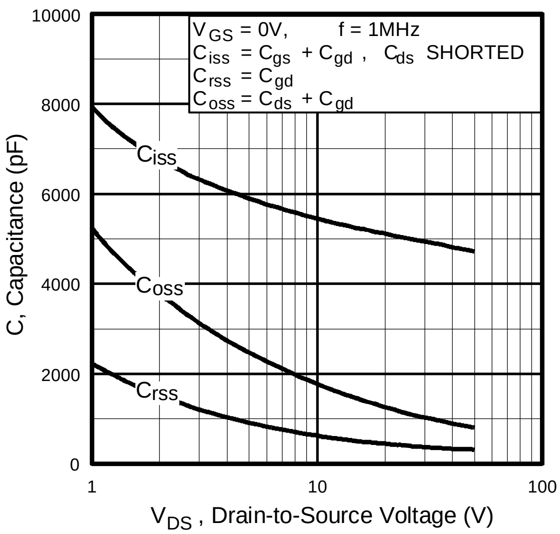


Fig 5. Typical Capacitance Vs. Drain-to-Source Voltage

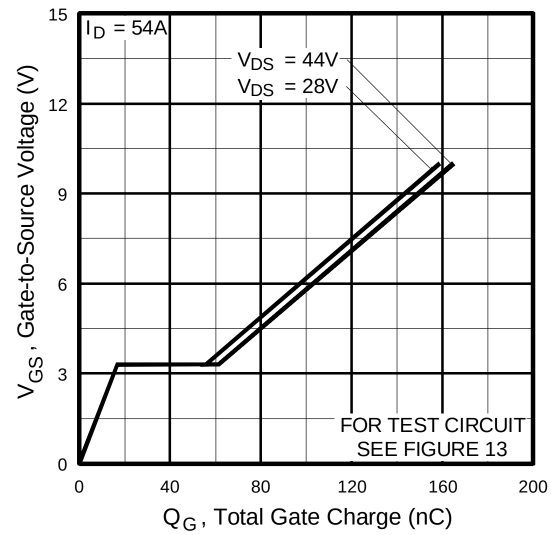


Fig 6. Typical Gate Charge Vs. Gate-to-Source Voltage

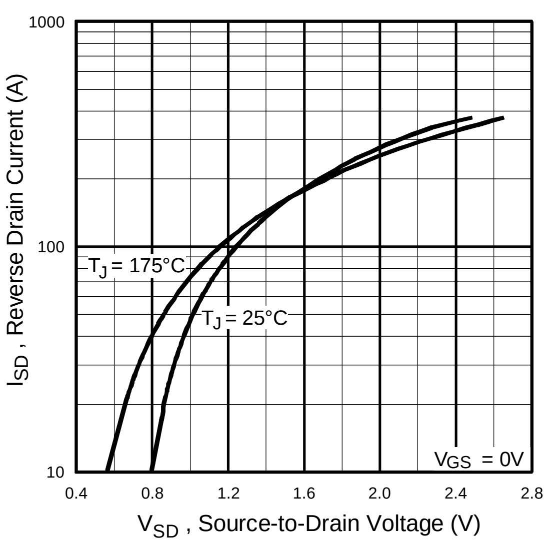


Fig 7. Typical Source-Drain Diode Forward Voltage

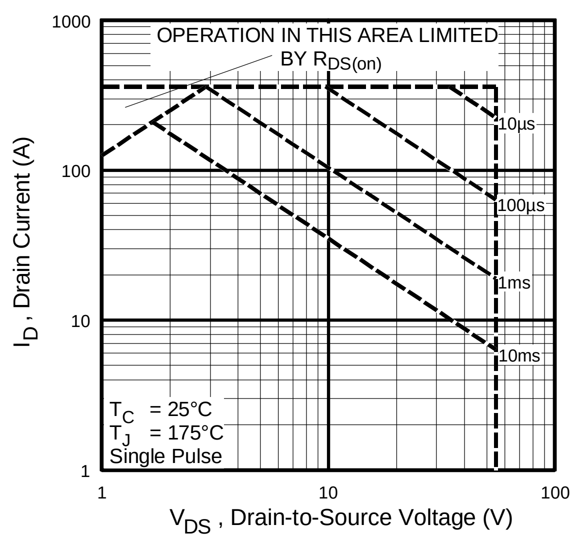


Fig 8. Maximum Safe Operating Area

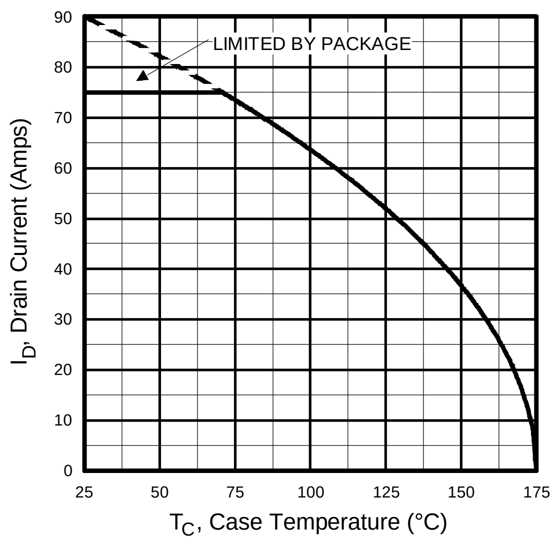


Fig 9. Maximum Drain Current Vs. Case Temperature

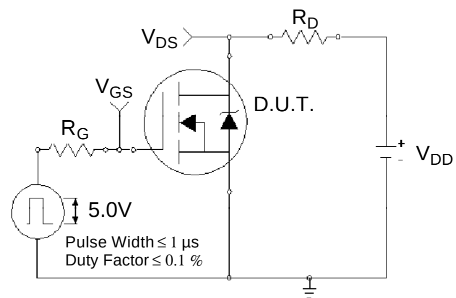


Fig 10a. Switching Time Test Circuit

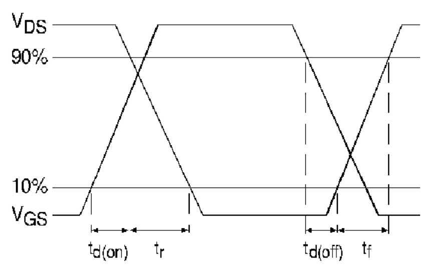


Fig 10b. Switching Time Waveforms

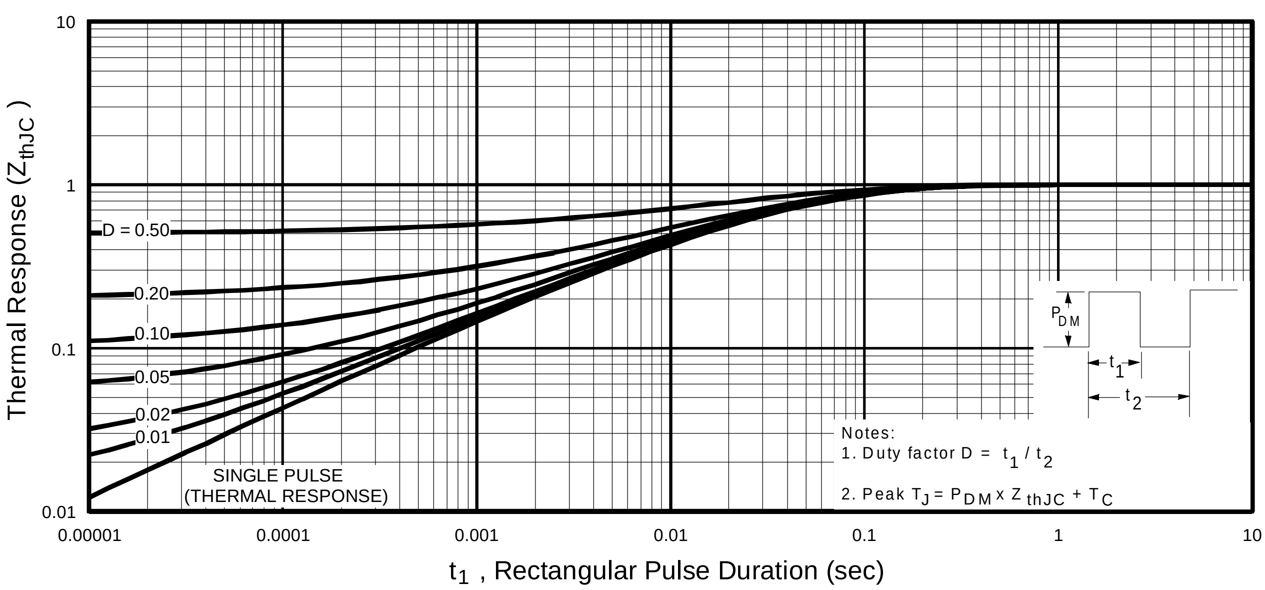


Fig 11. Maximum Effective Transient Thermal Impedance, Junction-to-Case

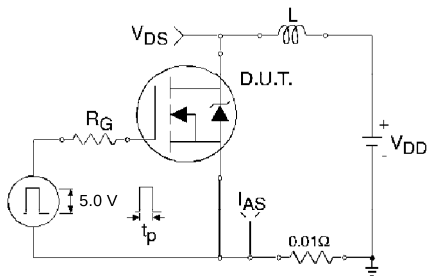


Fig 12a. Unclamped Inductive Test Circuit

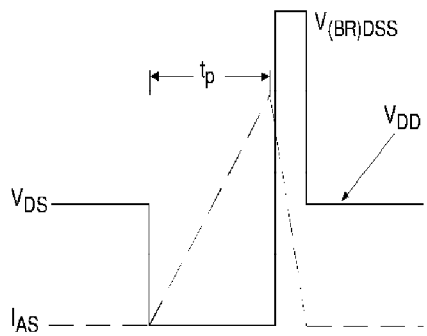


Fig 12b. Unclamped Inductive Waveforms

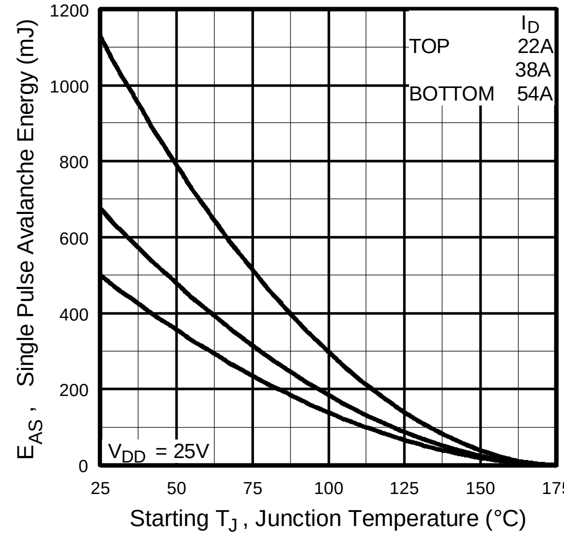


Fig 12c. Maximum Avalanche Energy Vs. Drain Current

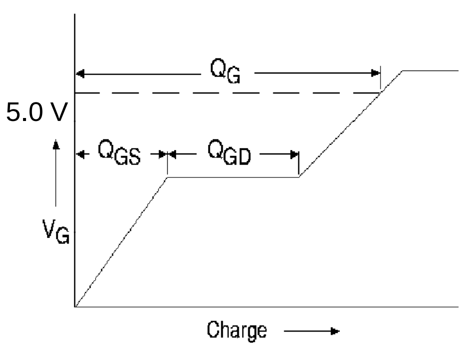


Fig 13a. Basic Gate Charge Waveform

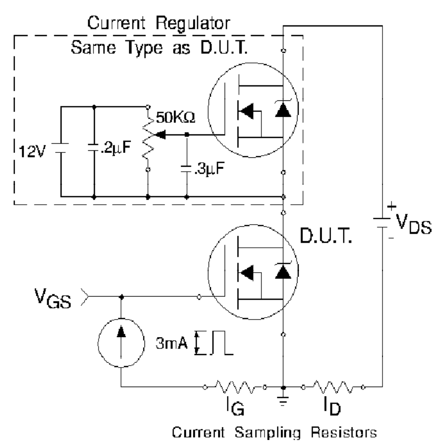
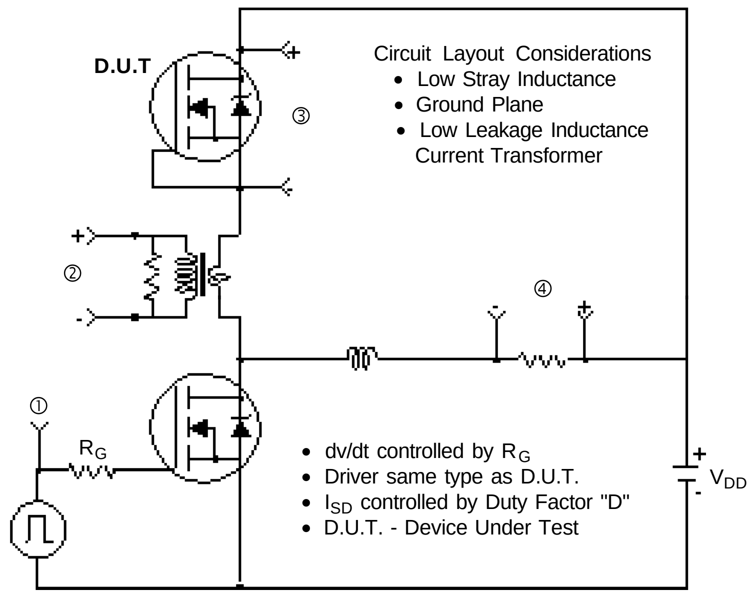
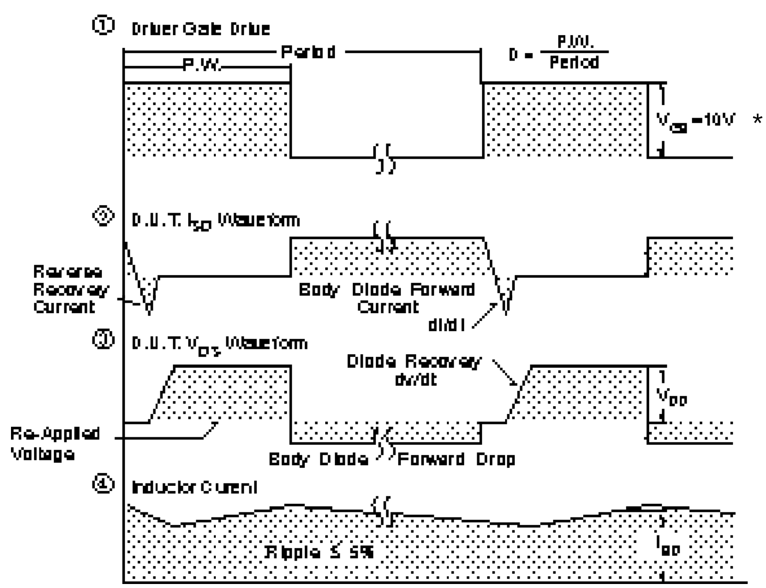


Fig 13b. Gate Charge Test Circuit

Peak Diode Recovery dv/dt Test Circuit





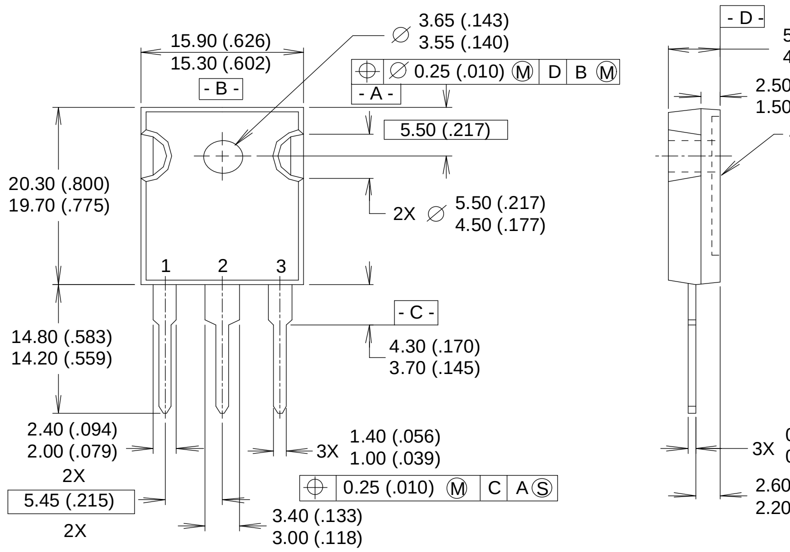
* V_{GS} = 5V for Logic Level Devices

Fig 14. For N-Channel HEXFETS

Package Outline

TO-247AC Outline

Dimensions are shown in millimeters (inches)



NOTES:

1 DIMENSIONING & TOLERANCING PER ANSI Y14.5M, 1982.
2 CONTROLLING DIMENSION : INCH.
3 CONFORMS TO JEDEC OUTLINE TO-247-AC.

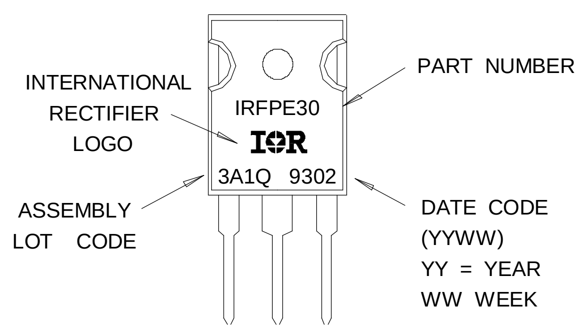
LEAD ASSIGNMENTS

1 - GATE
2 - DRAIN
3 - SOURCE
4 - DRAIN

Part Marking Information

TO-247AC

EXAMPLE : THIS IS AN IRFPE30 WITH ASSEMBLY LOT CODE 3A1Q



International Rectifier

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