

International **IR** Rectifier

PD - 91841A

IRLBA3803/P

HEXFET® Power MOSFET

- Logic-Level Gate Drive
- Advanced Process Technology
- 175°C Operating Temperature
- Fast Switching
- Fully Avalanche Rated

Description

Fifth Generation HEXFETs from International Rectifier utilize advanced processing techniques to achieve extremely low on-resistance per silicon area. This benefit, combined with the fast switching speed and ruggedized device design that HEXFET Power MOSFETs are well known for, provides the designer with an extremely efficient and reliable device for use in a wide variety of applications.

The Super-220 is a package that has been designed to have the same mechanical outline and pinout as the industry standard TO-220 but can house a considerably larger silicon die. It has increased current handling capability over both the TO-220 and the much larger TO-247 package.

This makes it ideal to reduce component count in multiparalleled TO-220 applications, reduce system power dissipation, upgrade existing designs or have TO-247 performance in a TO-220 outline.

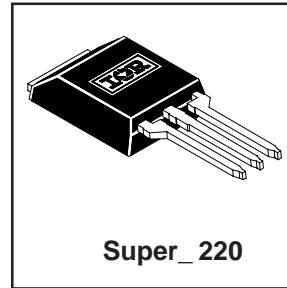
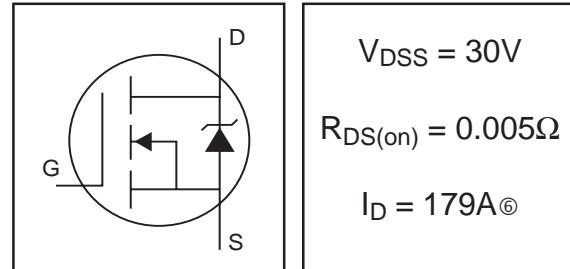
This package has also been designed to meet automotive qualification standard Q101.

Absolute Maximum Ratings

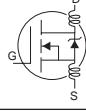
	Parameter	Max.	Units
$I_D @ T_C = 25^\circ C$	Continuous Drain Current, $V_{GS} @ 10V$	179 ⑥	
$I_D @ T_C = 100^\circ C$	Continuous Drain Current, $V_{GS} @ 10V$	126⑥	A
I_{DM}	Pulsed Drain Current ①	720	
$P_D @ T_C = 25^\circ C$	Power Dissipation	270	W
	Linear Derating Factor	1.8	W/C
V_{GS}	Gate-to-Source Voltage	± 16	V
E_{AS}	Single Pulse Avalanche Energy ②⑤	610	mJ
I_{AR}	Avalanche Current ①⑤	71	A
E_{AR}	Repetitive Avalanche Energy ①	27	mJ
dv/dt	Peak Diode Recovery dv/dt ③⑤	5.0	V/ns
T_J	Operating Junction and	-55 to + 175	$^\circ C$
T_{STG}	Storage Temperature Range		
	Soldering Temperature, for 10 seconds	300 (1.6mm from case)	
	Recommended clip force	20	N

Thermal Resistance

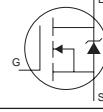
	Parameter	Typ.	Max.	Units
$R_{\theta JC}$	Junction-to-Case	—	0.55	
$R_{\theta CS}$	Case-to-Sink, Flat, Greased Surface	0.5	—	$^\circ C/W$
$R_{\theta JA}$	Junction-to-Ambient	—	58	



Electrical Characteristics @ $T_J = 25^\circ\text{C}$ (unless otherwise specified)

	Parameter	Min.	Typ.	Max.	Units	Conditions
$V_{(\text{BR})\text{DSS}}$	Drain-to-Source Breakdown Voltage	30	—	—	V	$V_{\text{GS}} = 0\text{V}$, $I_D = 250\mu\text{A}$
$\Delta V_{(\text{BR})\text{DSS}/\Delta T_J}$	Breakdown Voltage Temp. Coefficient	—	0.052	—	V°C	Reference to 25°C , $I_D = 1\text{mA}$ ⑤
$R_{\text{DS}(\text{on})}$	Static Drain-to-Source On-Resistance	—	—	0.005	Ω	$V_{\text{GS}} = 10\text{V}$, $I_D = 71\text{A}$ ④
		—	—	0.009		$V_{\text{GS}} = 4.5\text{V}$, $I_D = 59\text{A}$ ④
$V_{\text{GS}(\text{th})}$	Gate Threshold Voltage	1.0	—	—	V	$V_{\text{DS}} = V_{\text{GS}}$, $I_D = 250\mu\text{A}$
g_{fs}	Forward Transconductance	55	—	—	S	$V_{\text{DS}} = 25\text{V}$, $I_D = 71\text{A}$ ⑤
I_{DSS}	Drain-to-Source Leakage Current	—	—	25	μA	$V_{\text{DS}} = 30\text{V}$, $V_{\text{GS}} = 0\text{V}$
		—	—	250		$V_{\text{DS}} = 24\text{V}$, $V_{\text{GS}} = 0\text{V}$, $T_J = 150^\circ\text{C}$
I_{GSS}	Gate-to-Source Forward Leakage	—	—	100	nA	$V_{\text{GS}} = 16\text{V}$
	Gate-to-Source Reverse Leakage	—	—	-100		$V_{\text{GS}} = -16\text{V}$
Q_g	Total Gate Charge	—	—	140	nC	$I_D = 71\text{A}$
Q_{gs}	Gate-to-Source Charge	—	—	41		$V_{\text{DS}} = 24\text{V}$
Q_{gd}	Gate-to-Drain ("Miller") Charge	—	—	78		$V_{\text{GS}} = 4.5\text{V}$, See Fig. 6 and 13 ④⑤
$t_{\text{d}(\text{on})}$	Turn-On Delay Time	—	14	—		$V_{\text{DD}} = 15\text{V}$
t_r	Rise Time	—	230	—		$I_D = 71\text{A}$
$t_{\text{d}(\text{off})}$	Turn-Off Delay Time	—	29	—		$R_G = 1.3\Omega$
t_f	Fall Time	—	35	—		$R_D = 0.20\Omega$, See Fig. 10 ④⑤
L_D	Internal Drain Inductance	—	2.0	—	nH	Between lead, 6mm (0.25in.) from package and center of die contact
L_S	Internal Source Inductance	—	5.0	—		
C_{iss}	Input Capacitance	—	5000	—	pF	$V_{\text{GS}} = 0\text{V}$
C_{oss}	Output Capacitance	—	1800	—		$V_{\text{DS}} = 25\text{V}$
C_{rss}	Reverse Transfer Capacitance	—	880	—		$f = 1.0\text{MHz}$, See Fig. 5⑤

Source-Drain Ratings and Characteristics

	Parameter	Min.	Typ.	Max.	Units	Conditions
I_S	Continuous Source Current (Body Diode)	—	—	179⑥	A	MOSFET symbol showing the integral reverse p-n junction diode.
I_{SM}	Pulsed Source Current (Body Diode)①	—	—	720		
V_{SD}	Diode Forward Voltage	—	—	1.3	V	$T_J = 25^\circ\text{C}$, $I_S = 71\text{A}$, $V_{\text{GS}} = 0\text{V}$ ④
t_{rr}	Reverse Recovery Time	—	120	180	ns	$T_J = 25^\circ\text{C}$, $I_F = 71\text{A}$
Q_{rr}	Reverse Recovery Charge	—	450	680	nC	$dI/dt = 100\text{A}/\mu\text{s}$ ④⑤
t_{on}	Forward Turn-On Time	Intrinsic turn-on time is negligible (turn-on is dominated by L_S+L_D)				

Notes:

- ① Repetitive rating; pulse width limited by max. junction temperature. (See fig. 11)
- ② $V_{\text{DD}} = 15\text{V}$, starting $T_J = 25^\circ\text{C}$, $L = 180\mu\text{H}$, $R_G = 25\Omega$, $I_{AS} = 71\text{A}$. (See Figure 12)
- ③ $I_{SD} \leq 71\text{A}$, $dI/dt \leq 130\text{A}/\mu\text{s}$, $V_{\text{DD}} \leq V_{(\text{BR})\text{DSS}}$, $T_J \leq 175^\circ\text{C}$

④ Pulse width $\leq 300\mu\text{s}$; duty cycle $\leq 2\%$.

⑤ Uses IRL3803 data and test conditions.

⑥ Calculated continuous current based on maximum allowable junction temperature; for recommended current-handling of the package refer to Design Tip # 93-4

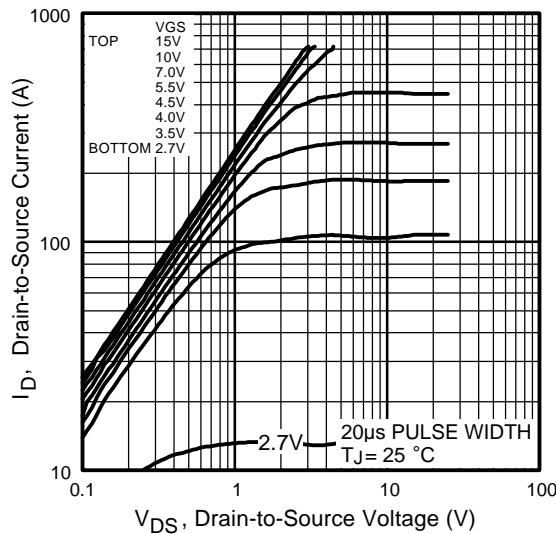


Fig 1. Typical Output Characteristics

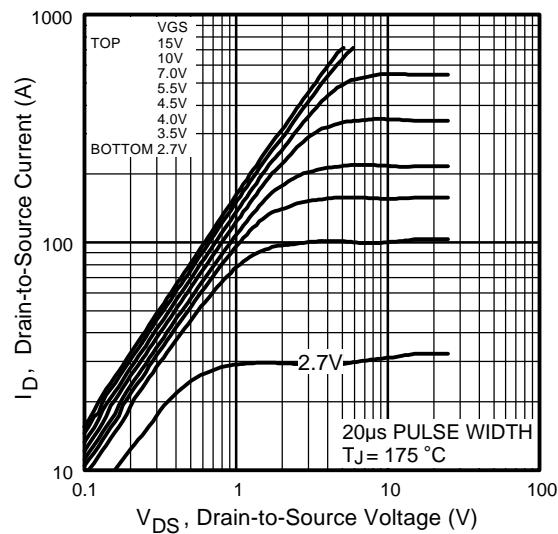


Fig 2. Typical Output Characteristics

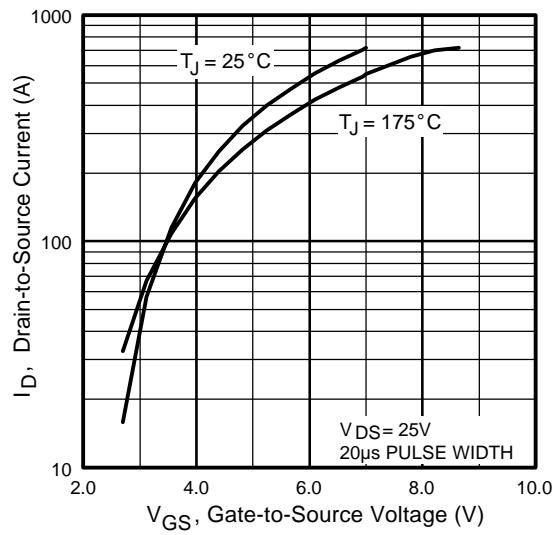


Fig 3. Typical Transfer Characteristics

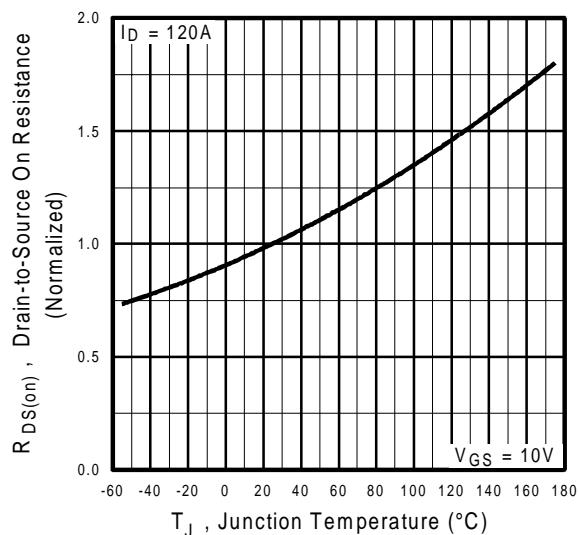


Fig 4. Normalized On-Resistance
Vs. Temperature

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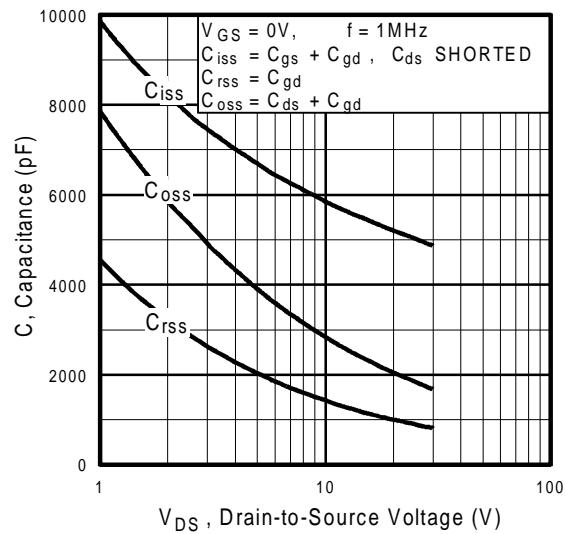


Fig 5. Typical Capacitance Vs.
Drain-to-Source Voltage

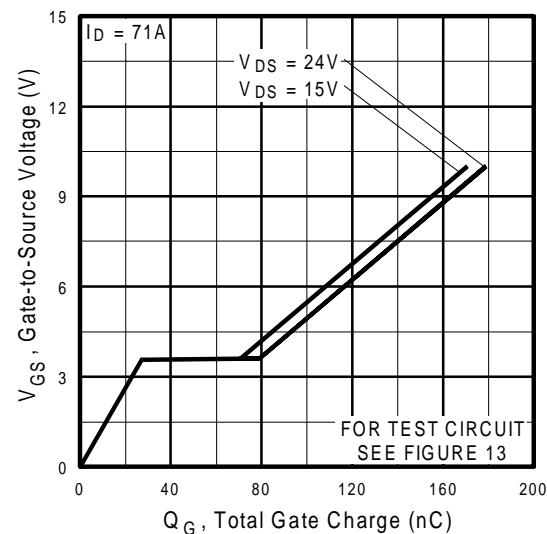


Fig 6. Typical Gate Charge Vs.
Gate-to-Source Voltage

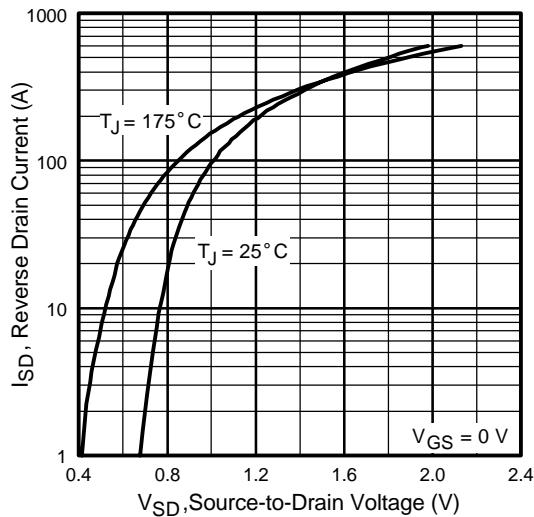


Fig 7. Typical Source-Drain Diode
Forward Voltage

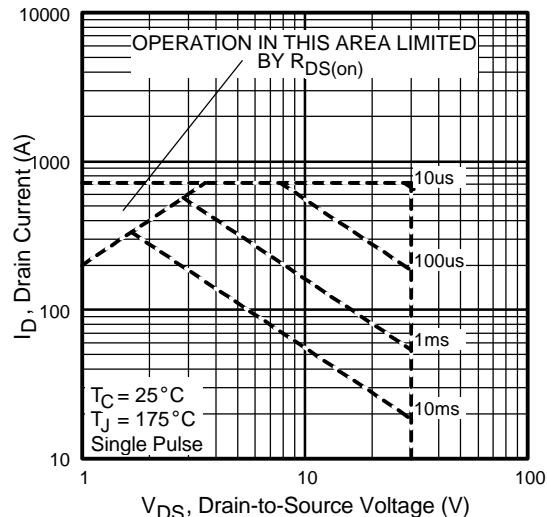


Fig 8. Maximum Safe Operating Area

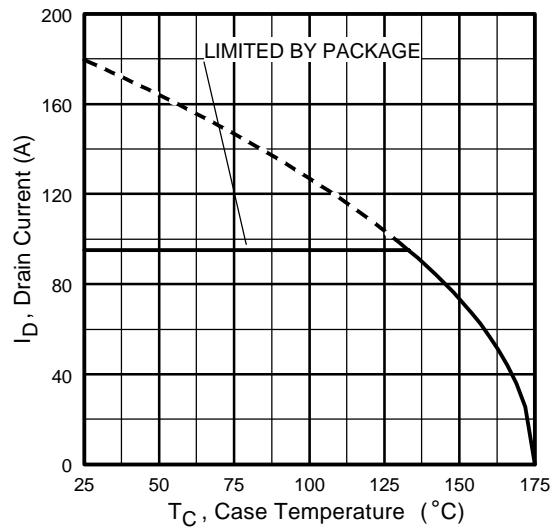


Fig 9. Maximum Drain Current Vs.
Case Temperature

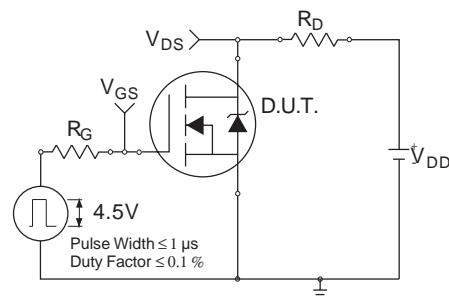


Fig 10a. Switching Time Test Circuit

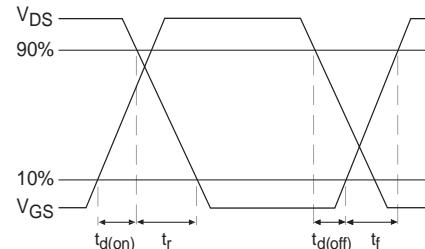


Fig 10b. Switching Time Waveforms

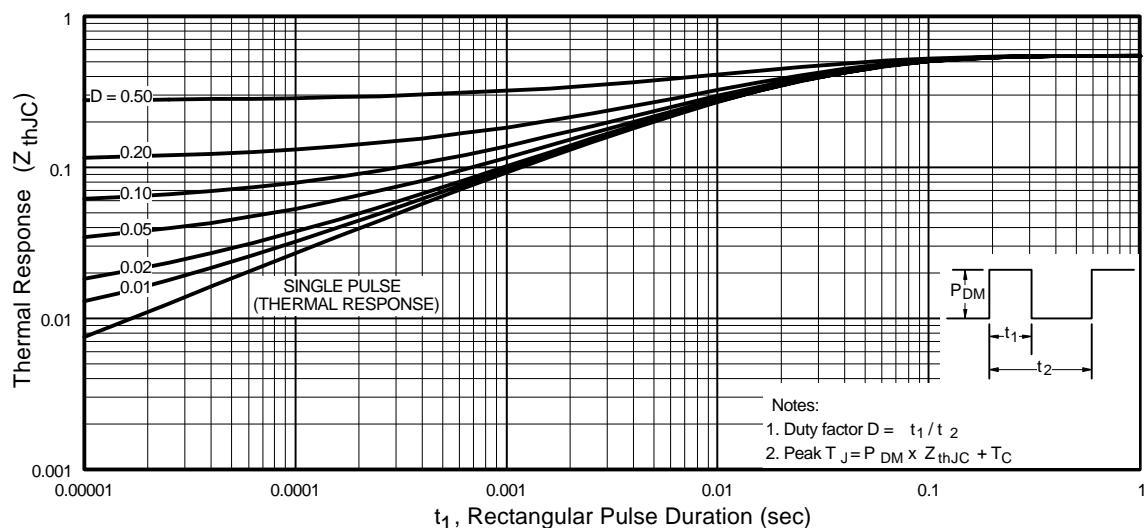


Fig 11. Maximum Effective Transient Thermal Impedance, Junction-to-Case

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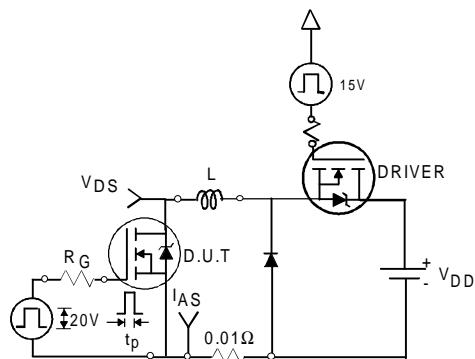


Fig 12a. Unclamped Inductive Test Circuit

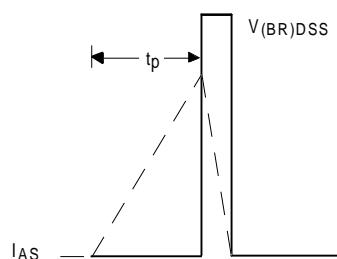


Fig 12b. Unclamped Inductive Waveforms

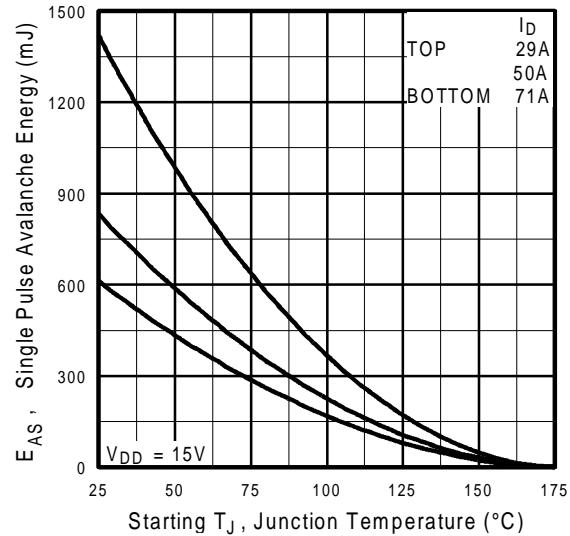


Fig 12c. Maximum Avalanche Energy
Vs. Drain Current

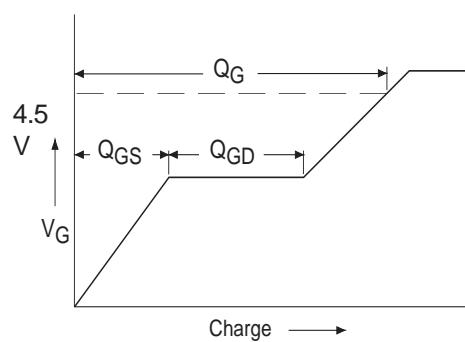


Fig 13a. Basic Gate Charge Waveform

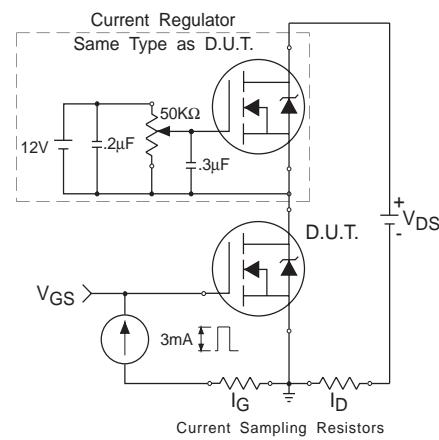
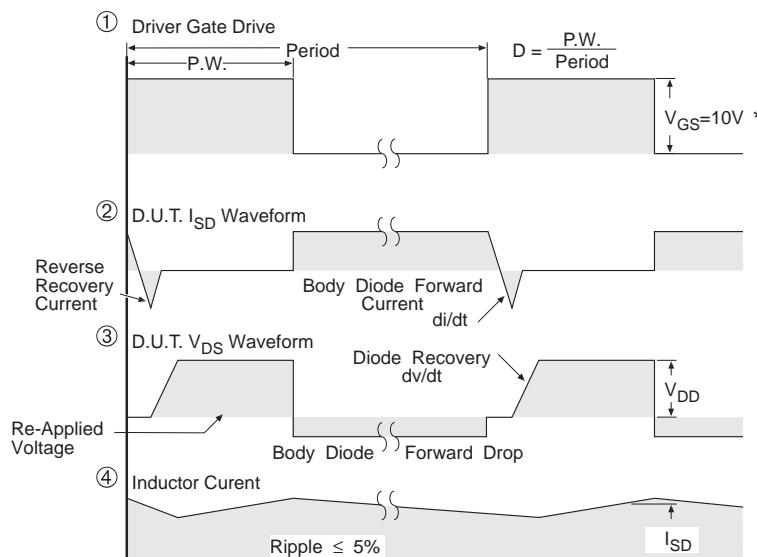
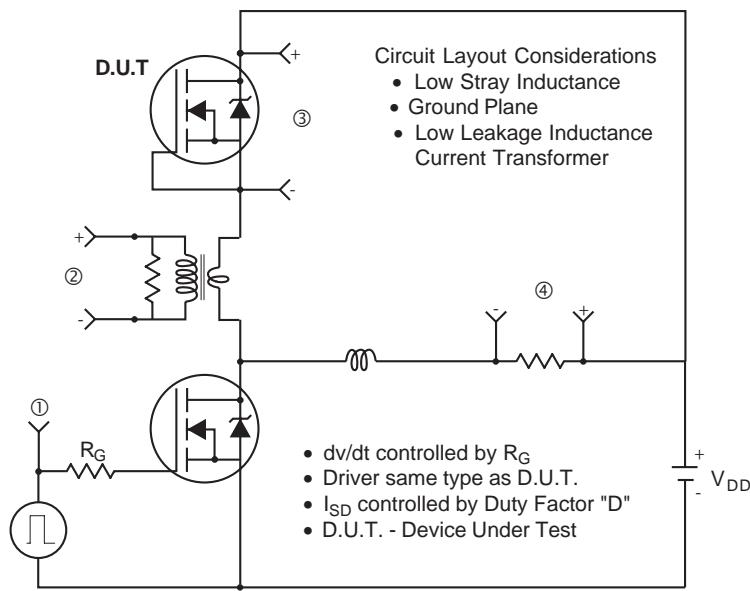


Fig 13b. Gate Charge Test Circuit

Peak Diode Recovery dv/dt Test Circuit



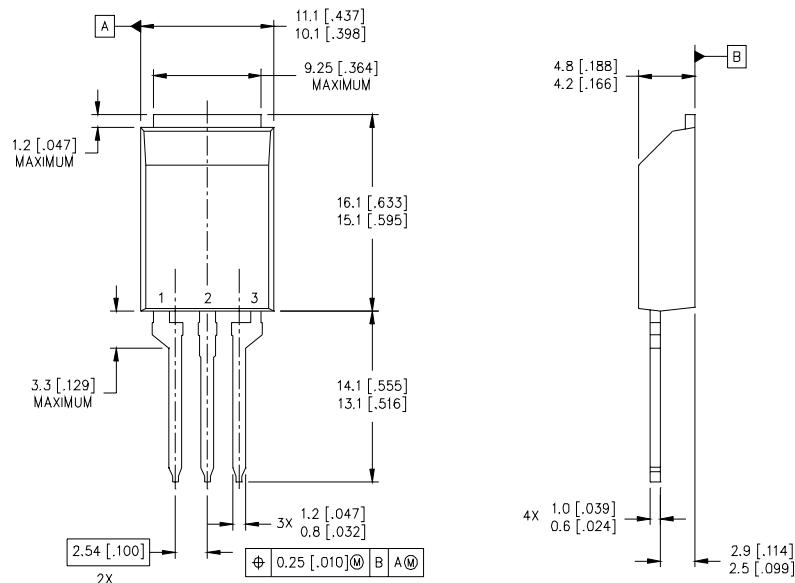
* $V_{GS} = 5V$ for Logic Level Devices

Fig 14. For N-Channel HEXFETS

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Super_220 Package Outline



NOTES:

1. DIMENSIONING & TOLERANCING PER ASME Y14.5M-1994.
2. CONTROLLING DIMENSION: MILLIMETER.
3. DIMENSIONS ARE SHOWN IN MILLIMETERS [INCHES].

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