International
IOR Rectifier

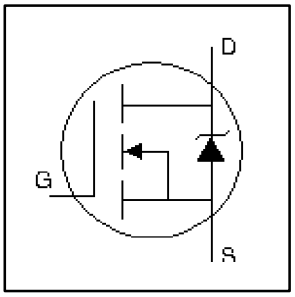
PD - 9.1275

PRELIMINARY

IRL2310

HEXFET® Power MOSFET

- Advanced Process Technology
- Ultra Low On-Resistance
- Dynamic dv/dt Rating
- Repetitive Avalanche Rated
- Logic-Level Gate Drive
- $R_{DS(on)}$ Specified at V_{GS}= 4.5V & 10V
- 175°C Operating Temperature



V_{DSS} = 100V

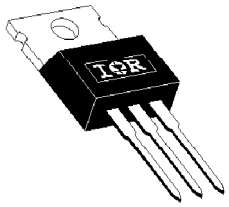
$R_{DS(on)}$ = 0.040Ω

I_D = 40A

Description

Fourth Generation HEXFETs from International Rectifier utilize advanced processing techniques to achieve the lowest possible on resistance per silicon area. This benefit, combined with the fast switching speed and ruggedized device design for which HEXFET Power MOSFETs are well known, provides the designer with an extremely efficient device for use in a wide variety of application.

The TO-220 package is universally preferred for all commercial-industrial applications at power dissipation levels to approximately 50 watts. The low thermal resistance and low package cost of the TO-220 contribute to its wide acceptance throughout the industry.



TO-220AB

Absolute Maximum Ratings

	Parameter	Max.	Units
I_D @ T_C = 25°C	Continuous Drain Current, V_{GS} @ 5.0V	40	A
I_D @ T_C = 100°C	Continuous Drain Current, V_{GS} @ 5.0V	29	
I_{DM}	Pulsed Drain Current ①	160	
P_D @T_C = 25°C	Power Dissipation	170	W
	Linear Derating Factor	1.1	W/°C
V_{GS}	Gate-to-Source Voltage	±20	V
E_{AS}	Single Pulse Avalanche Energy ②	500	mJ
I_{AR}	Avalanche Current ①	24	A
E_{AR}	Repetitive Avalanche Energy ①	17	mJ
dv/dt	Peak Diode Recovery dv/dt ③	5.5	V/ns
T_J	Operating Junction and	-55 to + 175	°C
T_{STG}	Storage Temperature Range		
	Soldering Temperature, for 10 seconds	300 (1.6mm from case)	
	Mounting torque, 6-32 or M3 screw.	10 lbf•in (1.1N•m)	

Thermal Resistance

	Parameter	Min.	Typ.	Max.	Units
$R_{\theta JC}$	Junction-to-Case	——	——	0.90	°C/W
$R_{\theta CS}$	Case-to-Sink, Flat, Greased Surface	——	0.50	——	
$R_{\theta JA}$	Junction-to-Ambient	——	——	62	

Electrical Characteristics @ T_J = 25°C (unless otherwise specified)

	Parameter	Min.	Typ.	Max.	Units	Conditions
$V_{(BR)DSS}$	Drain-to-Source Breakdown Voltage	100	—	—	V	V_{GS} = 0V, I_D = 250µA
$\Delta V_{(BR)DSS}/\Delta T_J$	Breakdown Voltage Temp. Coefficient	—	0.11	—	V/°C	Reference to 25°C, I_D = 1mA
$R_{DS(ON)}$	Static Drain-to-Source On-Resistance	—	—	0.040	Ω	V_{GS} = 10V, I_D = 24A ④
		—	—	0.050		V_{GS} = 4.5V, I_D = 20A ④
$V_{GS(th)}$	Gate Threshold Voltage	1.0	—	2.0	V	V_{DS} = V_{GS}, I_D = 250µA
g_{fs}	Forward Transconductance	18	—	—	S	V_{DS} = 50V, I_D = 24A
I_{DSS}	Drain-to-Source Leakage Current	—	—	25	µA	V_{DS} = 100V, V_{GS} = 0V
		—	—	250		V_{DS} = 80V, V_{GS} = 0V, T_J = 150°C
I_{GSS}	Gate-to-Source Forward Leakage	—	—	100	nA	V_{GS} = 20V
	Gate-to-Source Reverse Leakage	—	—	-100		V_{GS} = -20V
Q_g	Total Gate Charge	—	—	160	nC	I_D = 24A
Q_{gs}	Gate-to-Source Charge	—	—	13		V_{DS} = 80V
Q_{gd}	Gate-to-Drain ("Miller") Charge	—	—	45		V_{GS} = 10V, See Fig. 6 and 13 ④
$t_{d(on)}$	Turn-On Delay Time	—	6.6	—	ns	V_{DD} = 50V
t_r	Rise Time	—	38	—		I_D = 24A
$t_{d(off)}$	Turn-Off Delay Time	—	140	—		R_G = 5.0Ω
t_f	Fall Time	—	84	—		R_D = 2.0Ω, See Fig. 10 ④
L_D	Internal Drain Inductance	—	4.5	—	nH	Between lead, 6mm (0.25in.) from package and center of die contact
L_S	Internal Source Inductance	—	7.5	—		
C_{iss}	Input Capacitance	—	3200	—	pF	V_{GS} = 0V
C_{oss}	Output Capacitance	—	610	—		V_{DS} = 25V
C_{rss}	Reverse Transfer Capacitance	—	140	—		f = 1.0MHz, See Fig. 5

Source-Drain Ratings and Characteristics

	Parameter	Min.	Typ.	Max.	Units	Conditions
I_S	Continuous Source Current (Body Diode)	—	—	40	A	MOSFET symbol showing the integral reverse p-n junction diode.
I_{SM}	Pulsed Source Current (Body Diode) ①	—	—	160		
V_{SD}	Diode Forward Voltage	—	—	1.6	V	T_J = 25°C, I_S = 24A, V_{GS} = 0V ④
t_{rr}	Reverse Recovery Time	—	180	270	ns	T_J = 25°C, I_F = 24A
Q_{rr}	Reverse Recovery Charge	—	0.98	1.5	µC	di/dt = 100A/µs ④
t_{on}	Forward Turn-On Time	Intrinsic turn-on time is negligible (turn-on is dominated by L_S+L_D)				

Notes:

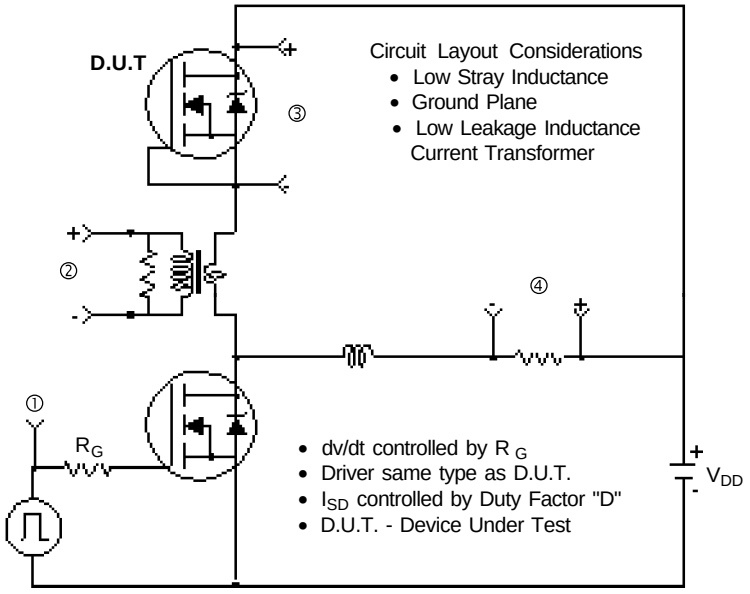
① Repetitive rating; pulse width limited by max. junction temperature. (See fig. 11)

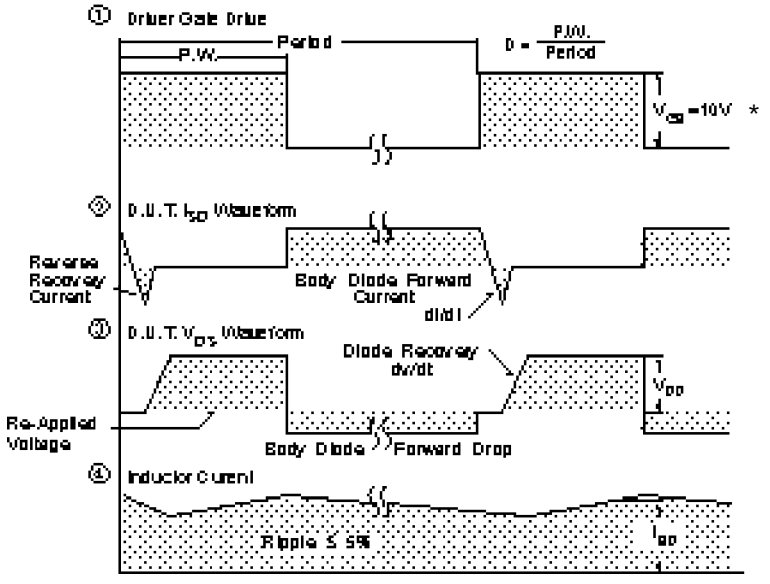
② V_{DD} = 25V, starting T_J = 25°C, L = 540 µH R_G = 25Ω, I_{AS} = 24A. (See Figure 12)

③ I_{SD} ≤ 24A, di/dt ≤ 170A/µs, V_{DD} ≤ $V_{(BR)DSS}$, T_J ≤ 175°C

④ Pulse width ≤ 300µs; duty cycle ≤ 2%.

Peak Diode Recovery dv/dt Test Circuit



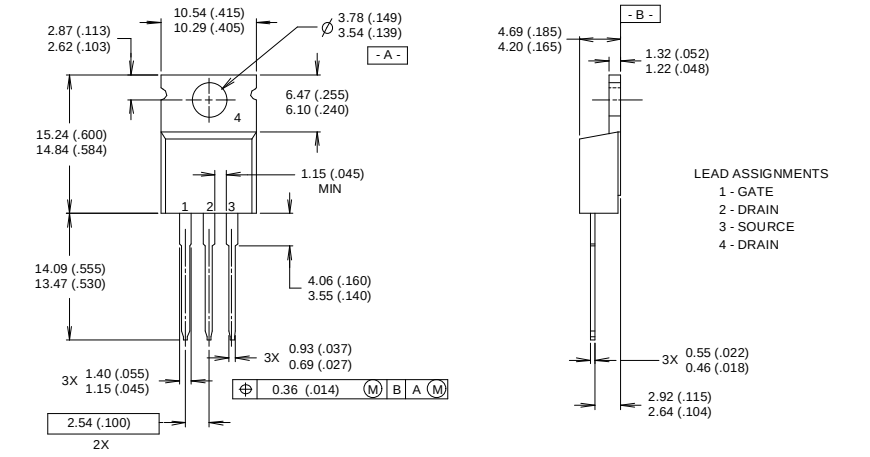


* VGS = 5V for Logic Level Devices

Fig 14. For N-Channel HEXFETS

Package Outline

TO-220AB Outline
Dimensions are shown in millimeters (inches)

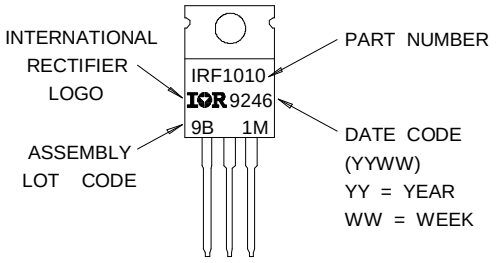


NOTES:
1 DIMENSIONING & TOLERANCING PER ANSI Y14.5M, 1982.
2 CONTROLLING DIMENSION : INCH
3 OUTLINE CONFORMS TO JEDEC OUTLINE TO-220-AB.
4 HEATSINK & LEAD MEASUREMENTS DO NOT INCLUDE BURRS.

Part Marking Information

TO-220AB

EXAMPLE : THIS IS AN IRF1010
WITH ASSEMBLY
LOT CODE 9B1M



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