Bulletin I27135 rev.C 09/97

International
IOR Rectifier

IRKU/V71, 91 SERIES

THYRISTOR/ THYRISTOR **NEW ADD-A-pak™ Power Modules**

75 A
95 A

Features

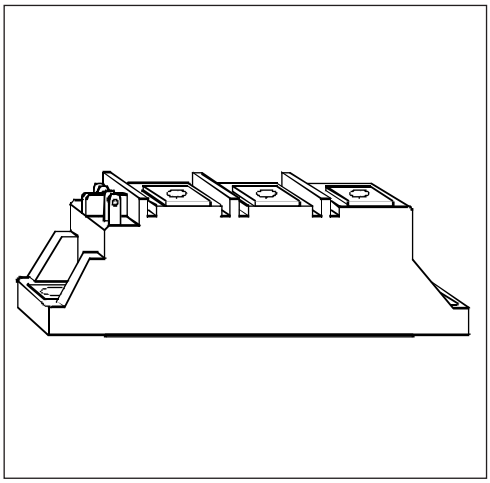
- Electrically isolated: DBC base plate
- 3500 V_{RMS} isolating voltage
- Standard JEDEC package
- Simplified mechanical designs, rapid assembly
- Auxiliary cathode terminals for wiring convenience
- High surge capability
- Wide choice of circuit configurations
- Large creepage distances
- UL E78996 approved

Description

These IRKU/V series of NEW ADD-A-paks use power thyristors in two circuit configurations. The semiconductor chips are electrically isolated from the base plate, allowing common heatsinks and compact assemblies to be built. They can be interconnected to form single phase bridges (IRKU+IRKV) or 6-pulse midpoint connection bridge. These modules are intended for general purpose high voltage applications such as high voltage regulated power supplies, battery charge and DC motor speed control circuits.

Major Ratings and Characteristics

Parameters		IRKU/V71	IRKU/V91	Units
$I_{T(AV)}$	@ 85°C	75	95	A
$I_{T(RMS)}$		115	150	A
I_{TSM}	@ 50Hz	1665	1785	A
	@ 60Hz	1740	1870	A
I^2t	@ 50Hz	13.86	15.91	KA^2s
	@ 60Hz	12.56	14.52	KA^2s
$I^2\sqrt{t}$		138.6	159.1	$KA^2\sqrt{s}$
V_{RRM} range		400 to 1600		V
T_{STG}		-40 to 125		°C
T_J		-40 to125		°C



ELECTRICAL SPECIFICATIONS

Voltage Ratings

Type number	Voltage Code -	V_{RRM}, maximum repetitive peak reverse voltage V	V_{RSM}, maximum non-repetitive peak reverse voltage V	V_{DRM}, max. repetitive peak off-state voltage, gate open circuit V	I_{RRM} I_{DRM} 125°C mA
IRKU/V71, 91	04	400	500	400	15
	08	800	900	800	
	12	1200	1300	1200	
	16	1600	1700	1600	

On-state Conduction

Parameters		IRKU/V71	IRKU/V91	Units	Conditions		
$I_{T(AV)}$	Max. average on-state current	75	95	A	180° conduction, half sine wave, T_C = 85°C		
$I_{T(RMS)}$	Max. RMS on-state current	115	150		DC		
	@T_C	80	75	°C			
I_{TSM}	Max. peak, one cycle non-repetitive on-state current	1665	1785	A	t=10ms	No voltage reapplied	Sinusoidal half wave, Initial T_J = T_J max.
		1740	1870		t=8.3ms		
		1400	1500		t=10ms	100% V_{RRM} reapplied	
		1470	1570		t=8.3ms		
		1850	2000		t=10ms	T_J = 25°C, no voltage reapplied	
		1940	2100		t=8.3ms		
I^2t	Max. I^2t for fusing	13.86	15.91	KA^2s	t=10ms	No voltage reapplied	Initial T_J = T_J max.
		12.56	14.52		t=8.3ms		
		9.80	11.25		t=10ms	100% V_{RRM} reapplied	
		8.96	10.27		t=8.3ms		
		17.11	20.00		t=10ms	T_J = 25°C, no voltage reapplied	
		15.60	18.30		t=8.3ms		
$I^2\sqrt{t}$	Max. $I^2\sqrt{t}$ for fusing (1)	138.6	159.1	$KA^2\sqrt{s}$	t=0.1 to 10ms, no voltage reapplied		
$V_{T(TO)}$	Max. value of threshold voltage (2)	0.82	0.80	V	Low level (3)		T_J = T_J max
		0.85	0.85		High level (4)		
r_t	Max. value of on-state slope resistance (2)	3.00	2.40	mΩ	Low level (3)		T_J = T_J max
		2.90	2.25		High level (4)		
V_{TM}	Max. peak on-state voltage	1.59	1.58	V	I_{TM} = π x $I_{T(AV)}$		T_J = 25°C
					I_{FM} = π x $I_{F(AV)}$		
di/dt	Max. non-repetitive rate of rise of turned on current	150		A/µs	T_J = 25°C, from 0.67 V_{DRM}, I_{TM} = π x $I_{T(AV)}$, I_g = 500mA, t_r < 0.5 µs, t_p > 6 µs		
I_H	Max. holding current	200		mA	T_J = 25°C, anode supply = 6V, resistive load, gate open circuit		
I_L	Max. latching current	400			T_J = 25°C, anode supply = 6V, resistive load		

(1) I^2t for time t_x = $I^2\sqrt{t}$ x $\sqrt{t_x}$. (2) Average power = $V_{T(TO)}$ x $I_{T(AV)}$ + r_t x $(I_{T(RMS)})^2$
(3) 16.7% x π x I_{AV} < I < π x I_{AV} (4) I > π x I_{AV}

Triggering

	Parameters	IRKU/V71	IRKU/V91	Units	Conditions	
P_{GM}	Max. peak gate power	12	12	W		
$P_{G(AV)}$	Max. average gate power	3.0	3.0			
I_{GM}	Max. peak gate current	3.0	3.0	A		
$-V_{GM}$	Max. peak negative gate voltage	10		V		
V_{GT}	Max. gate voltage required to trigger	4.0			T_J = - 40°C	Anode supply = 6V resistive load
		2.5			T_J = 25°C	
		1.7			T_J = 125°C	
I_{GT}	Max. gate current required to trigger	270		mA	T_J = - 40°C	Anode supply = 6V resistive load
		150			T_J = 25°C	
		80			T_J = 125°C	
V_{GD}	Max. gate voltage that will not trigger	0.25		V	T_J = 125°C, rated V_{DRM} applied	
I_{GD}	Max. gate current that will not trigger	6		mA	T_J = 125°C, rated V_{DRM} applied	

Blocking

	Parameters	IRKU/V71, 91	Units	Conditions
I_{RRM} I_{DRM}	Max. peak reverse and off-state leakage current at V_{RRM}, V_{DRM}	15	mA	T_J = 125 °C, gate open circuit
V_{INS}	RMS isolation voltage	2500 (1 min) 3500 (1 sec)	V	50 Hz, circuit to base, all terminals shorted
dv/dt	Max. critical rate of rise of off-state voltage (5)	500	V/µs	T_J = 125°C, linear to 0.67 V_{DRM}, gate open circuit

Thermal and Mechanical Specifications

	Parameters	IRK.71	IRK.91	Units	Conditions
T_J	Junction operating temperature range	- 40 to 125		°C	
T_{stg}	Storage temper. range	- 40 to 125			
R_{thJC}	Max. internal thermal resistance, junction to case	0.165	0.135	K/W	Per module, DC operation
R_{thCS}	Typical thermal resistance case to heatsink	0.1			Mounting surface flat, smooth and greased. Flatness < 0.03 mm; roughness < 0.02 mm
T	Mounting torque ± 10% to heatsink	5		Nm	A mounting compound is recommended and the torque should be rechecked after a period of 3 hours to allow for the spread of the compound
	busbar	3			
wt	Approximate weight	83 (3)		g (oz)	
	Case style	TO-240AA		JEDEC	

(5) Available with dv/dt = 1000V/µs, to complete code add S90 i.e. IRKU91/16S90.

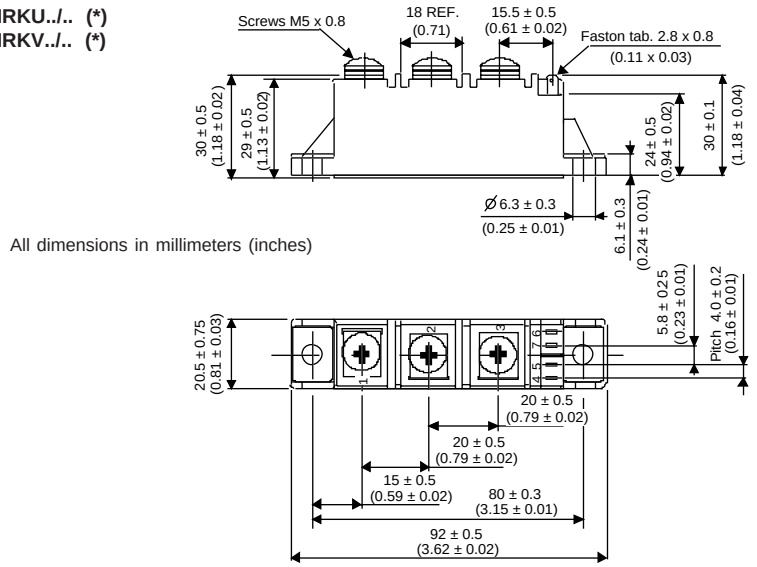
ΔR Conduction (per Junction)

(The following table shows the increment of thermal resistance R_{thJC} when devices operate at different conduction angles than DC)

Devices	Sine half wave conduction					Rect. wave conduction					Units
	180°	120°	90°	60°	30°	180°	120°	90°	60°	30°	
IRKU/V71	0.06	0.07	0.09	0.12	0.18	0.04	0.08	0.10	0.13	0.18	°C/W
IRKU/V91	0.04	0.05	0.06	0.08	0.12	0.03	0.05	0.06	0.08	0.12	

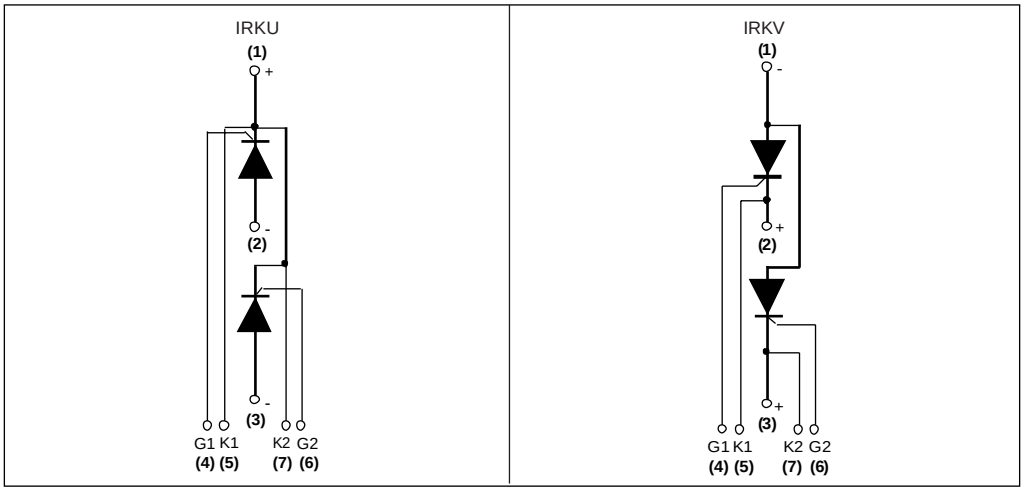
Outlines Table

IRKU../.. (*)
IRKV../.. (*)



(*) For terminals connections, see Circuit Configurations Table

Circuit Configurations Table



NOTE: To order the Optional Hardware see Bulletin I27900

Ordering Information Table

Device Code

IRK	U	91	/	16	S90
①	②	③		④	⑤

1 - Module type

2 - Circuit configuration (See Circuit Configuration Table)

3 - Current code

4 - Voltage code (See Voltage Ratings Table)

5 - dv/dt code: S90 = dv/dt 1000 V/µs

No letter = dv/dt 500 Vµs

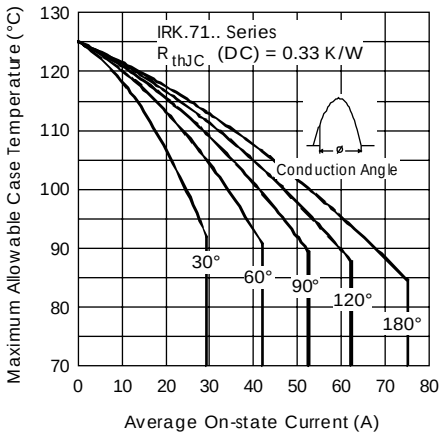


Fig. 1 - Current Ratings Characteristics

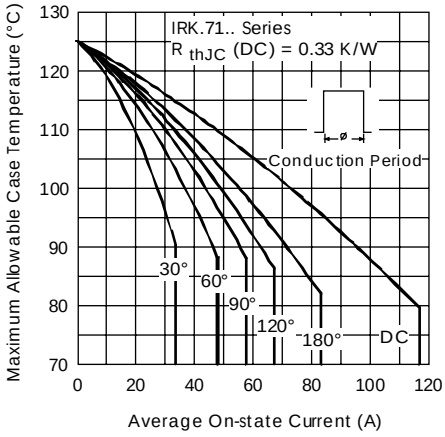


Fig. 2 - Current Ratings Characteristics

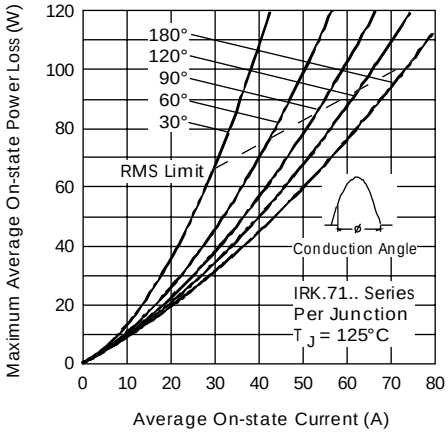


Fig. 3 - On-state Power Loss Characteristics

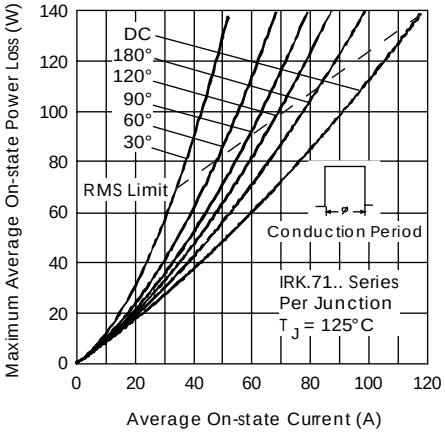


Fig. 4 - On-state Power Loss Characteristics

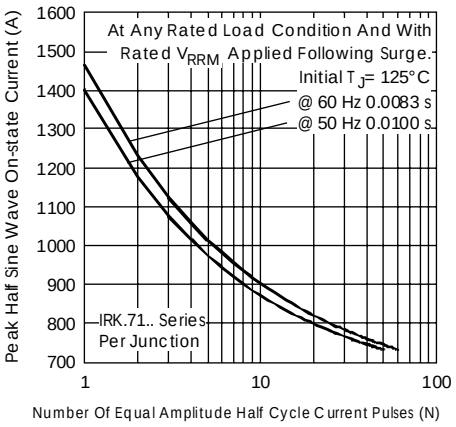


Fig. 5 - Maximum Non-Repetitive Surge Current

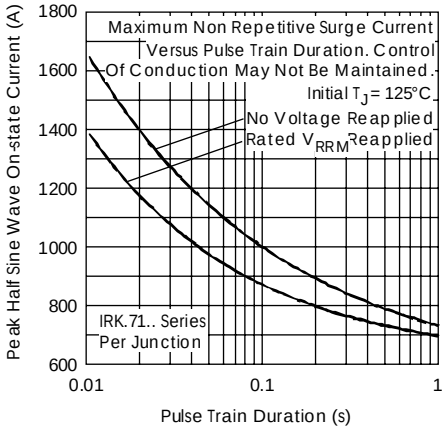


Fig. 6 - Maximum Non-Repetitive Surge Current

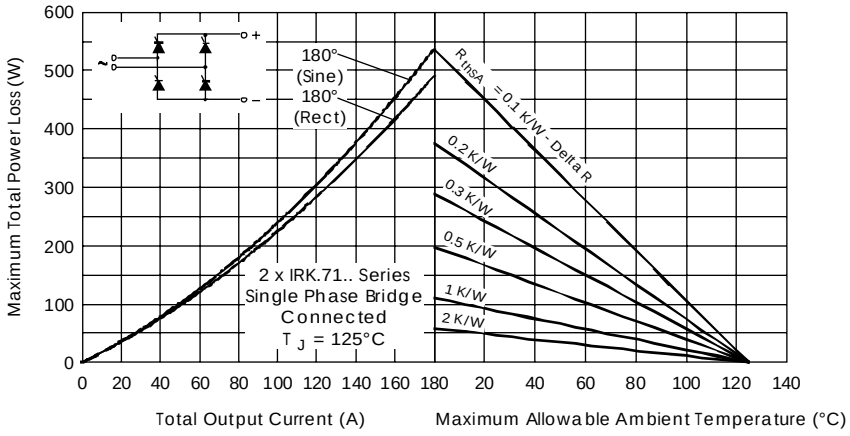


Fig. 7 - On-state Power Loss Characteristics (Single Phase Bridge IRKU+IRKV)

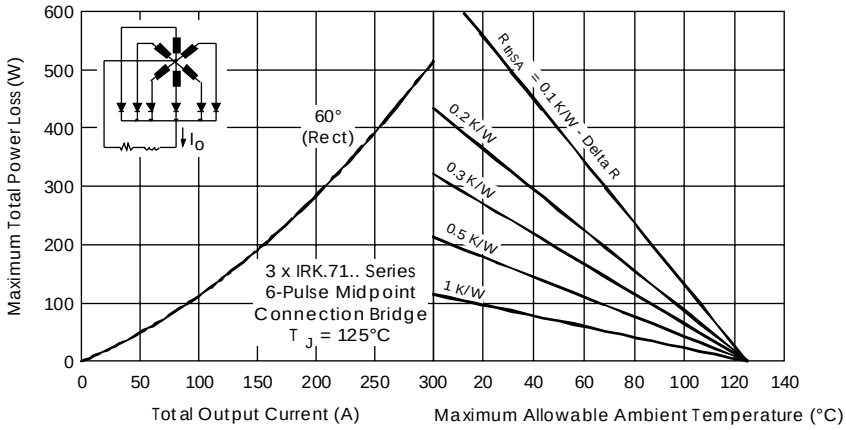


Fig. 8 - On-state Power Loss Characteristics

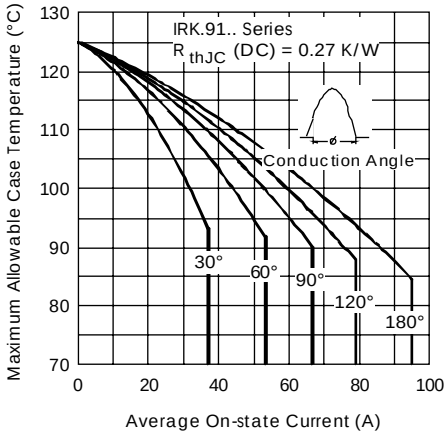


Fig. 9 - Current Ratings Characteristics

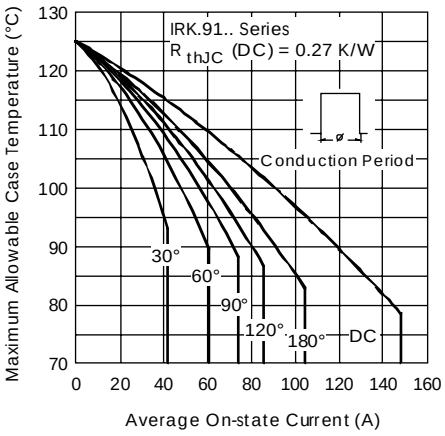


Fig. 10 - Current Ratings Characteristics

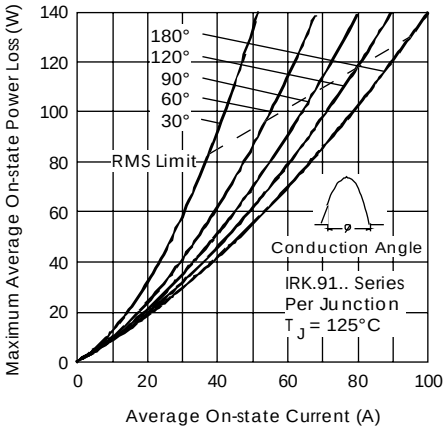


Fig. 11 - On-state Power Loss Characteristics

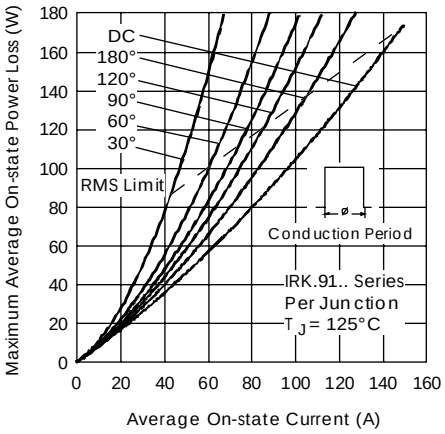


Fig. 12 - On-state Power Loss Characteristics

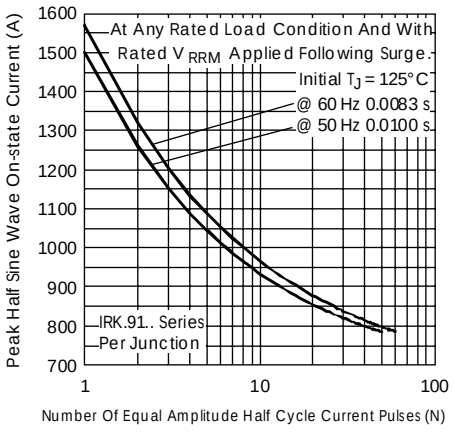


Fig. 13 - Maximum Non-Repetitive Surge Current

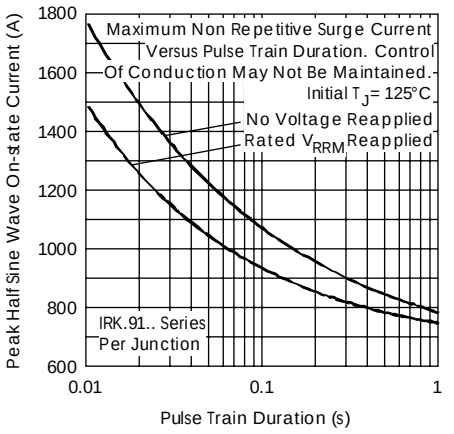


Fig. 14 - Maximum Non-Repetitive Surge Current

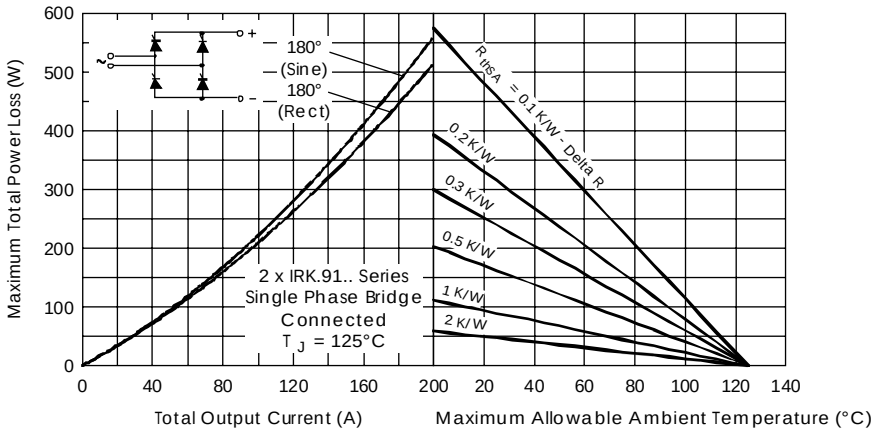


Fig. 15 - On-state Power Loss Characteristics (Single Phase Bridge IRKU+IRKV)

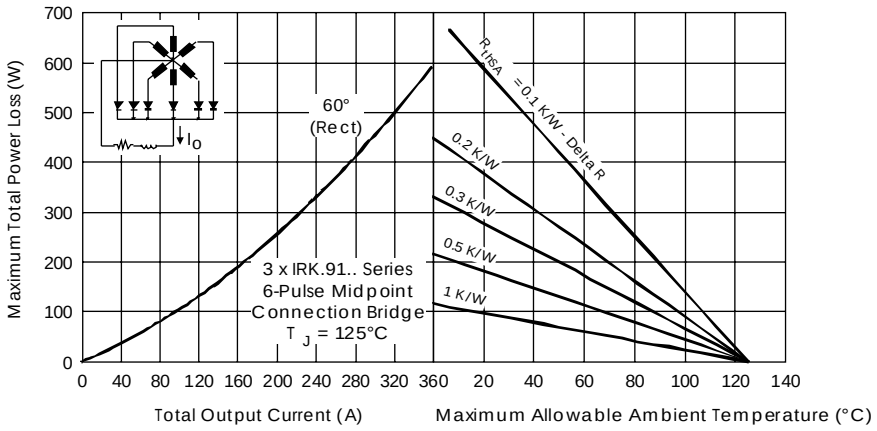


Fig. 16 - On-state Power Loss Characteristics

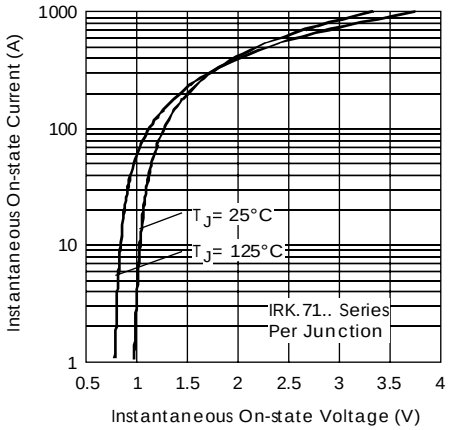


Fig. 17 - On-state Voltage Drop Characteristics

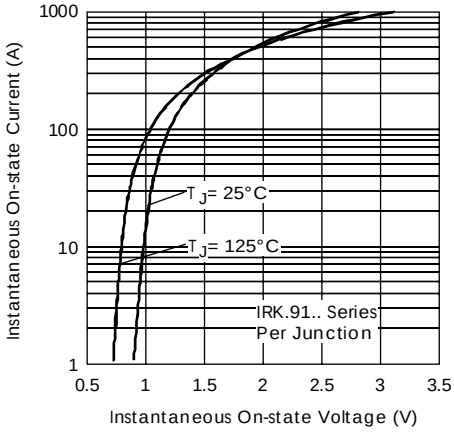


Fig. 18 - On-state Voltage Drop Characteristics

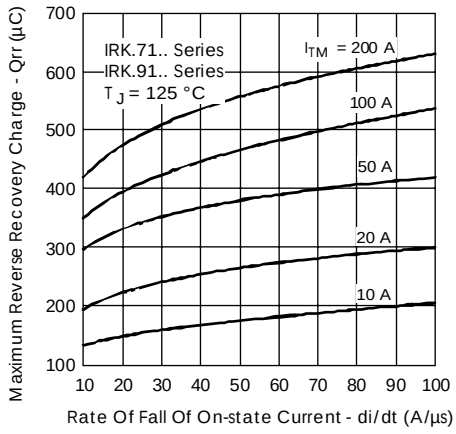


Fig. 19 - Recovery Charge Characteristics

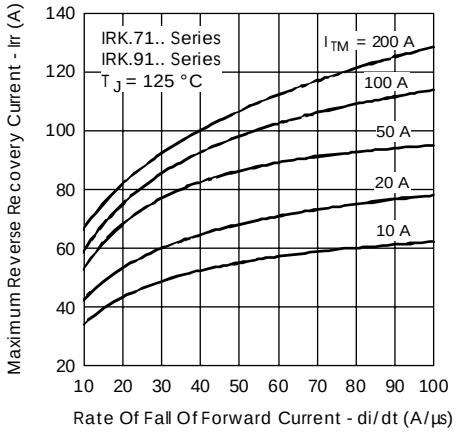


Fig. 20 - Recovery Current Characteristics

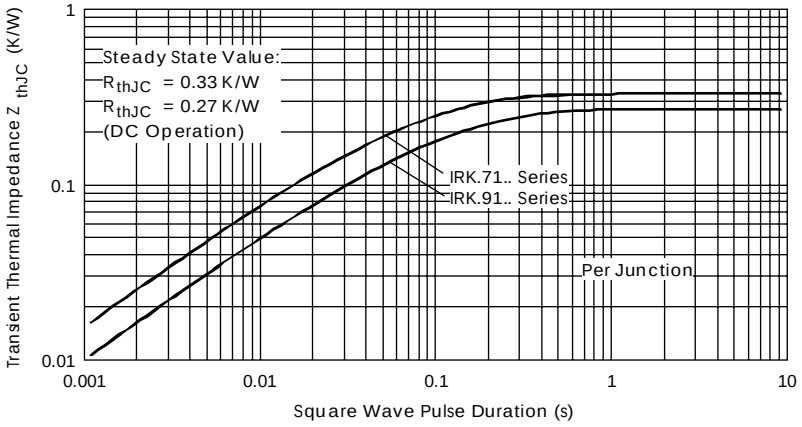


Fig. 21 - Thermal Impedance Z_{thJC} Characteristics

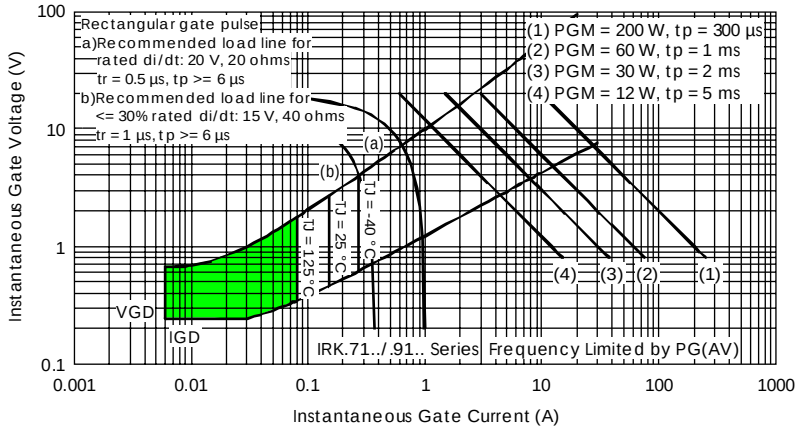


Fig. 22 - Gate Characteristics