International
IOR Rectifier

**IRISMPS2**

# REFERENCE DESIGN

International Rectifier • 233 Kansas Street El Segundo CA 90245 USA

## Technical Specifications

1. AC Input: V=90~265V, f=57~63Hz, I= 0.6Arms max

2. Inrush Current: 5A max

3. Efficiency: Typical 85% when measured at maximum load high line (82% at low line)

4. Output Characteristics

| Nominal Ouput Voltage | Load Range | | Regulation (V) |
|---|---|---|---|
| | Min | Max | |
| 12V | 0A | 2A | 11.4V ~ 12.6V |

5. Turn On Delay: <1sec @ 90V full load

6. Hold-Up Time: 80msec (230Vin Full load) / 10ms (90Vin Full load)

7. Short Circuit Protection: Yes

8: Output Rise Time: 1ms max (10-90%)

9: Over Voltage Protection: Yes

10: Switching Frequency: 50 -300kHz

## Relevant Technical Documents

AN1018a - Using the IR40xx Series SMPS ICs
AN1024a - Flyback transformer design for the IR40xx series
IRIS4011(K) - Datasheet

## Circuit Description

The IRISMPS2 refererence design is a complete tested power supply circuit. It is designed for a universal AC line input and will provide a 12V, 2A full load DC output.

The design uses a flyback converter topology, with an IRIS4011K as the main switch and control device. The initial startup current for the IRIS4011 is provided by a dropper resistor from the DC bus. Once the circuit is started the Vcc power for the IRIS4011 comes from the bias winding of the main transformer. The primary current control circuit consists of a current sensing resistor which feeds a voltage proportional to the transformer primary current into the feedback (FB) pin of the IRIS4011. The secondary voltage control loop uses a zener diode as the reference and an optocoupler to feedback the information across the transformer isolation boundary back to the control circuit of the IRIS4011.

## Test Circuit Set-up

The circuit is designed for a universal AC line input. To safely test and evaluate this circuit it ios recommended that an isolation transformer or a synthesized and isolated AC source (such as a Pacific Power Source 115-ASX) is used to power the board, with a voltage in the range of 85-265VAC, with a frequency of 50/60Hz. The AC input signal is applied to the pins at P1 and P2 marked on the board.

For the output the best load to use is an electronic load which will allow easy changes in the output load, e.g. something like a Chroma 63102. Another simple alternative is to use a High power resistor for the load.

## Circuit Operation

The front end of the circuit consists of an EMI Filter, a diode bridge rectifier, and a DC bus filter capacitor. These are all fairly common circuit components used to create a DC voltage at the top end of the transformer.

At power up the DC voltage is applied to the top of the transformer, and the top of resistor R2. R2 allows about 450uA of quiescent current to flow which charges the Vcc capacitor C6. When the voltage at the Vcc pin of the IRIS4011 reaches the positive undervoltage lockout threshold ($V_{CCUV+}$) , the IRIS4011 starts to operate and will turn on the internal FET. Now the DC bus voltage is applied across the transformer primary winding, the FET and the current sense resistors R9/R10. The current through the transformer primary, the FET and the current sense resistors will start to ramp up. the rate of the ramp is dependent on the DC bus voltage and hence the input line voltage (for example, the rate at 90VAC in is much lower than the rate at 230VAC in). The current ramps until the voltage across R9/R10 reaches the Vth1 of the IRIS4011 (0.73V typ). During this time there is no current flowing in either the bias winding or the output winding, because this is blocked by the diodes D7 and D6 respectively.

At the point when the voltage across R9/R10 reaches Vth1this activates a comparator in the IRIS4011 and the internal FET is switched off. Now the energy stored in the transformer causes the voltage at the Drain connected end of the transformer to rise, and as a result the voltage at the bias winding and the output winding changes from negative to positive. The output rectifiers now conduct and the energy is transferred to the output and the bias winding. If there is a fixed full current load on the output it will take a number of cycles for the output voltage to rise to the required level, and also it will take a few cycles for the bias winding to begin supplying power to the Vcc pin of the IRIS4011. Until this happens, C6 holds the voltage above the undervoltage lockout level (Vccuv-) to make sure the circuit does not drop out. During this time the circuit cannot create enough voltage signal through the delay circuit to activate the quasi-resonant operation, so the circuit operates with a fixed off time of 50us (this is the pulse raio control mode or PRC mode).

Once the the output capacitor C8 and the Vcc capacitor C6 are fully charged, the complete quasi-resonant signal is passed through the delay circuit D8/R6/D10 to the feedback (FB) pin. This will give a voltage above

the Vth2 threshold of the IRIS4011, and this activates the quasi-resonant operation, holding the internal FET off until all the energy is transferred from the primary side of the transformer to the secondary and bias outputs. When all the energy is transferred, the quasi-resonant signal at the FB pin will start to fall until it can no longer supply the 1.35mA required by the IRIS4011 internal latch, and the FET is turned back on. This is also the lowest point of the resonant voltage at the drain pin of the IRIS4011, so results in reduced switching losses.

If the AC input voltage changes but the load stays constant, the primary current ramp will now be steeper resulting in a shorter ON time, but still the same off time as it still takes the same amount of time to transfer the same energy to the output. The reduced ON time leads to a higher operating frequency.

If the AC input voltage remains constant, but the load is reduced, the secondary side voltage monitoring circuit (ISO1A/R5/D8) will see an increase in the voltage, as the circuit is still passing the same energy to the secondary side, but less current is being drawn. This causes the zener diode D8 to conduct, which leads to a current flow in the optocoupler ISO1A, which gets passed across the transformer boundary to the phototransistor part of the optocoupler ISO1B. This in turn creates a voltage drop across R8, generating an offset voltage at the FB pin which reduces the current required through the current sense resistors R9/R10 needed to reach a voltage of 0.73typ (Vth1 threshold) at the FB pin, and hence less energy is put into the transformer, reducing both the ON time and the OFF time.

## Circuit Waveforms

The following plots show waveforms taken from the circuit under various stated conditions

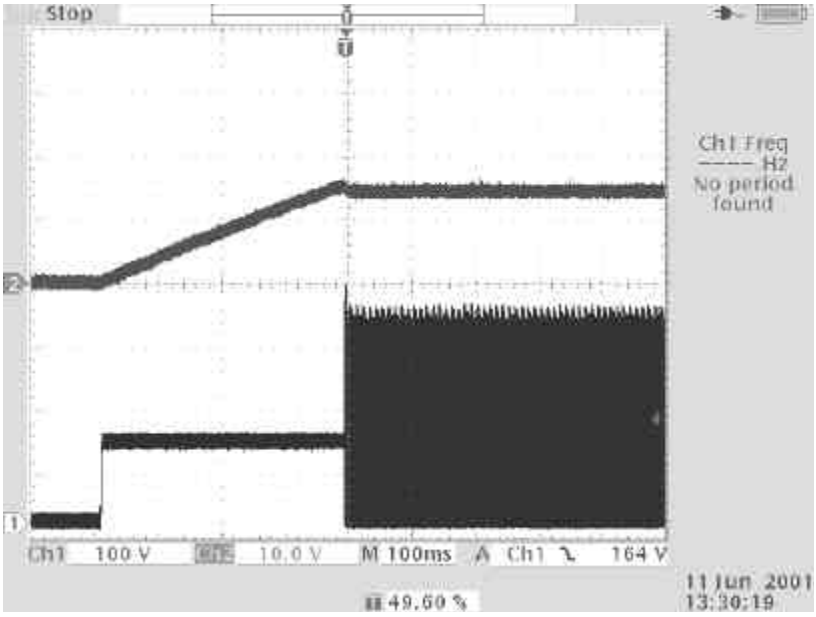



Fig 1) Drain (D) voltage of IRIS4011 (CH1) and Vcc voltage (CH2) at start-up

Fig 1) shows the drain voltage of the IRIS4011 and the Vcc voltage during start-up with full load output with a 110VAC input. Note the small dip in the Vcc voltage as the circuit starts to operate, and also the reflected voltage at the drain due from the output, raising the drain voltage above the DC bus.

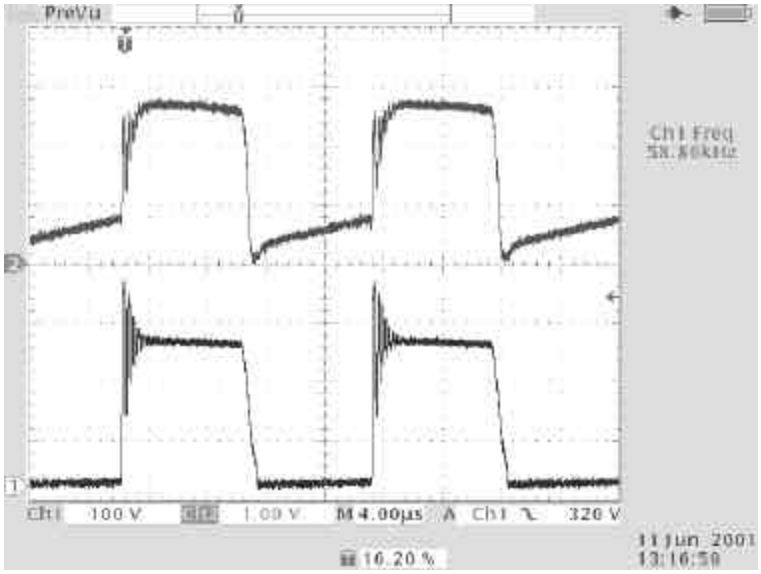



Fig 2)Drain (D) voltage of IRIS4011 (CH1) and the FB pin voltage (CH2) at 90VAC in/Full load output

Fig 2) shows the drain voltage and the feedback pin (FB) voltage. In this case the quasi-resonant signal swings all the way to zero volts at the drain before the FET is turned on, and hence underthese conditions the circuit turns the FET on with zero voltage switching, due to the quasi-resonant switching. The FB pin signal shows the current ramp when the FET is on(when the drain voltage is low), and the resonant signal being passed back during the FET off time. Note the operating frequency.

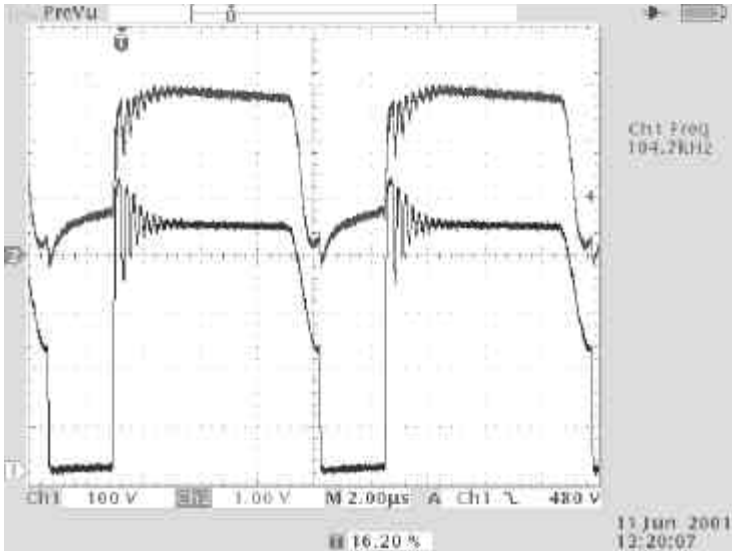



Fig 3) Drain (D) voltage of IRIS4011 (CH1) and the FB pin voltage (CH2) at 230VAC in/Full load output

Fig 3) shows the same waveforms as in fig 2) again with a full load output, but this time with a 230VAC input. Note that the operating frequency has now increased, and the effect of the quasi-resonant switching is now more pronounced. This is evident by the quarter sine wave nature of the falling edge of the drain waveform, at the bottom of which the FET is turned on, ensuring that it is turned on at the minimum possible voltage to reduce the switching losses. Note also the steeper ramp in the FB pin voltage when the FET is on which results in a shorter on time.

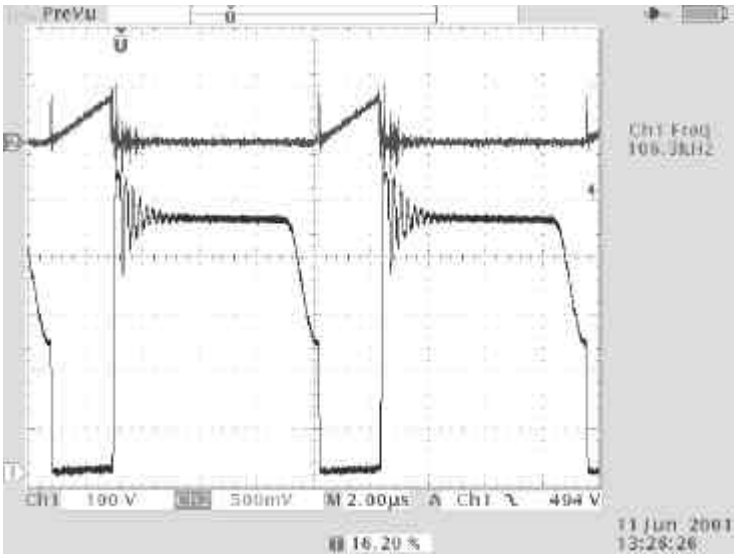



Fig 4) Drain (D) voltage of IRIS4011 (CH1) and the source(S) pin voltage (CH2) at 230VAC in/Full load output

Fig 4) shows the same conditions as for fig 3), but this time it show the Source (S) pin voltage with the drain voltage showing the effect of the primary current ramp, which is seen as a voltage generated across the current sense resistors R9/R10. Note that this waveform shows some noise on the source pin voltage which is smothed out by the RC filter comprising R8 and C11. The intial voltage spike at the start of the ramp is a result of discharging the quasi-resonant capacitor C5 and the primary winding capacitance of the transformer.

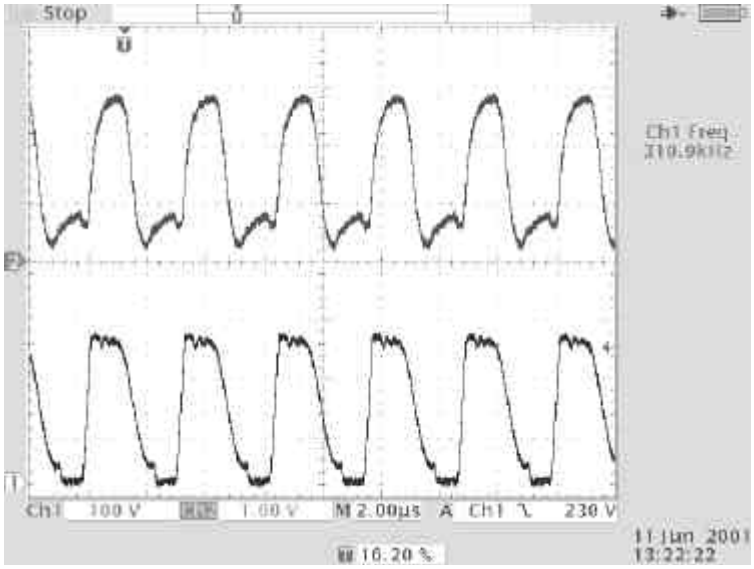



Fig 5) Drain (D) voltage of IRIS4011 (CH1) and the FB pin voltage (CH2) at 90VAC in/0.1A load output

Fig 5) again shows the drain and FB pin voltages, but this time with a 90VAC and a light load condition of 0.1A (1.2W output power). Again the quasi-resonant effect can be seen by the quarter wave signal on the drain pin and also at the FB pin. Note the very short on time, and the fact that the current ramp voltage at the FB pin does not start from zero, this is due to the offset voltage generated from the voltage feedback loop across R8.

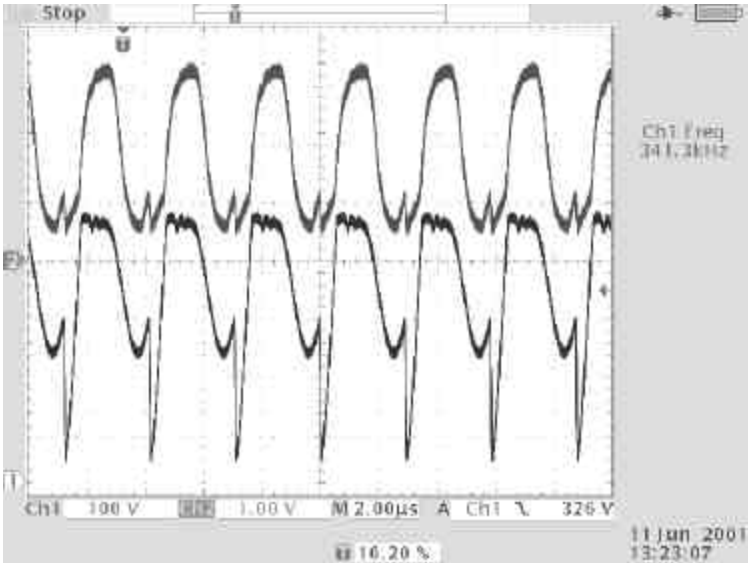
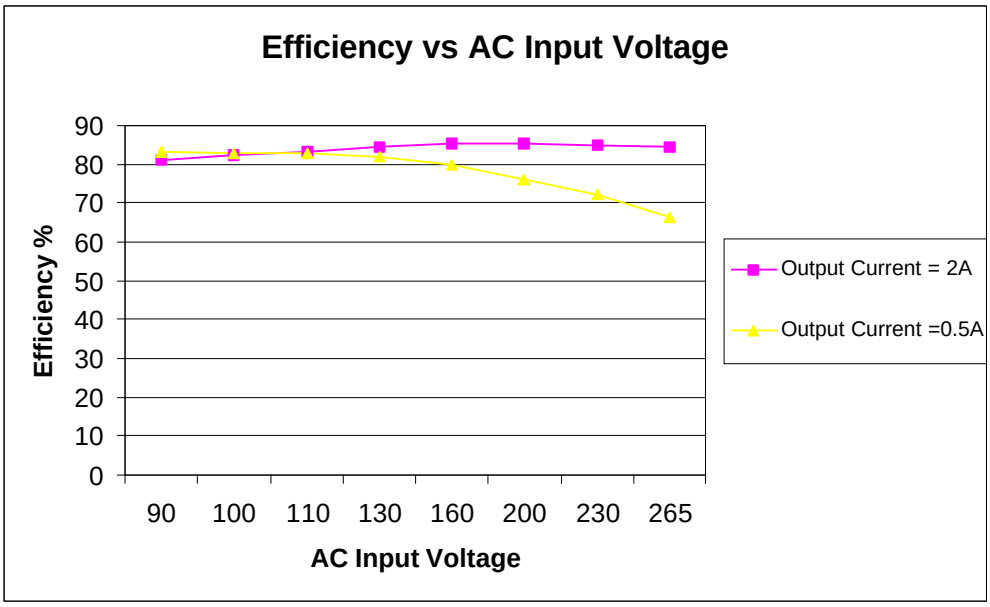
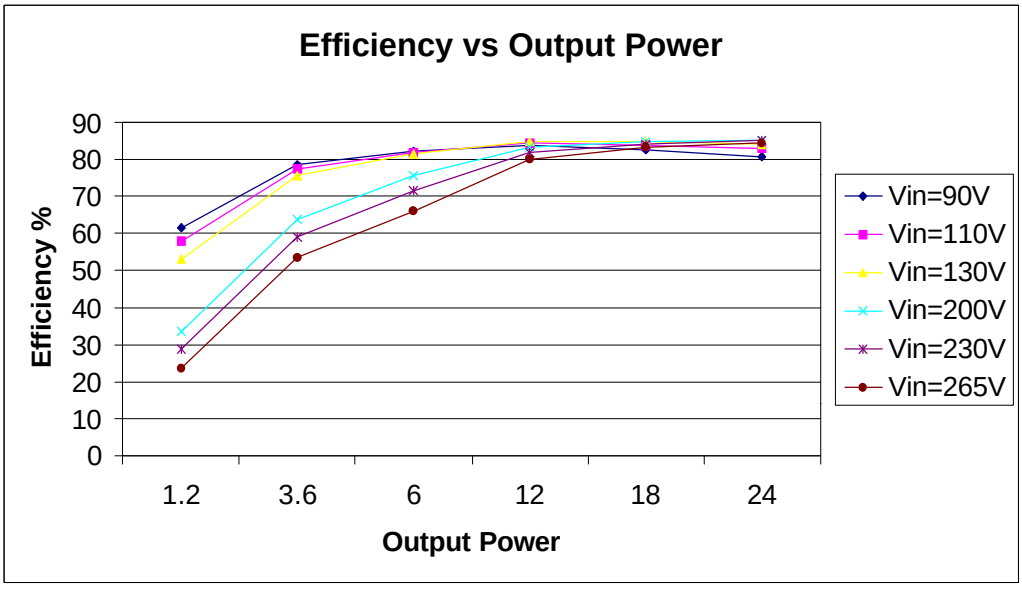



Fig 6)Drain (D) voltage of IRIS4011 (CH1) and the FB pin voltage (CH2) at 230VAC in/0.1A load output

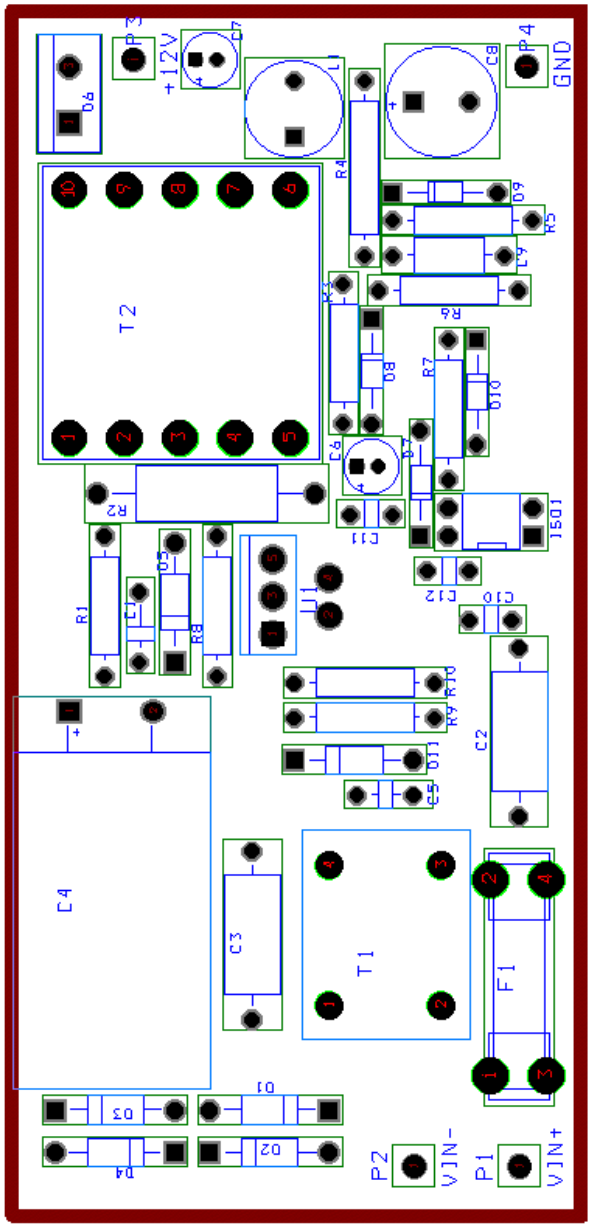
Fig 6) showsthe same details as in fig 5), but at 230VAC input, in this case you can see the on time is very short as it takes very little time to get the energy required into the transformer.

### Efficiency

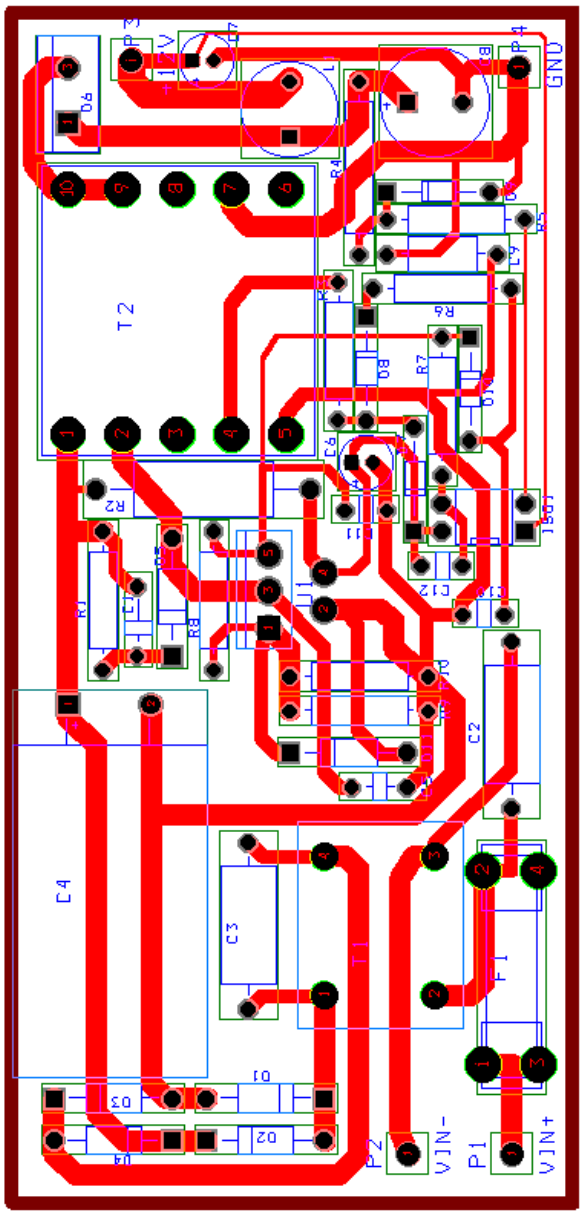


**Board Layout - Component Side**



**Board Layout - Track Side**



**WORLD HEADQUARTERS:** 233 Kansas St., El Segundo, California 90245 Tel: (310) 252-7105