International
IOR Rectifier

PD - 91781

HEXFET® TRANSISTORS

IRHQ6110
IRHQ63110

COMBINATION N AND P CHANNEL (2 EACH)
MEGA RAD HARD

100 Volt, 0.38Ω (N channel) MEGA RAD HARD HEXFET and -100 Volt, 0.88Ω (P channel) RAD HARD HEXFET

International Rectifier's MEGA RADHARD Technology HEXFETs demonstrate excellent threshold voltage stability and breakdown voltage stability at total radiation doses as high as $3x10^5$ Rads (Si). Under identical pre and post irradiation test conditions, International Rectifier's LCC packaged RAD HARD HEXFETs retain identical electrical specifications up to$1x10^5$ Rads(Si) total dose. No compensation in gate drive circuitry is required. In addition, these devices are capable of surviving transient ionization pulses as high as $1x10^{12}$ Rads (Si)/Sec, and return to the normal operation within a few microseconds. Single Event Effect (SEE) testing of International Rectifier RAD HARD HEXFETs has demonstrated immunity to SEE failure. Since the MEGA RAD process utilizes International Rectifier's patented technology, the user can expect the highest quality and reliability in the industry.

RAD HARD HEXFET transistors also feature all of the well established advantages of MOSFETs such as voltage control, very fast switching, ease of paralleling, and temperature stability of the electrical parameters. They are well suited for applications such as switching power supplies, motor controls, inverters, choppers, audio amplifiers, and high energy pulse circuits in space and weapons environments.

Product Summary

Part Number	BV_{DSS}	$R_{DS(on)}$		I_D	
		N	P	N	P
IRHQ6110	± 100V	0.38Ω	0.88Ω	3.0A	-2.2A

Features:

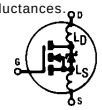
- Radiation Hardened up to $3x10^5$ Rads(Si)
- Single Event Burnout (SEB) Hardened
- Single event Gate Rupture (SEGR) Hardened
- Gamma Dot (Flash X-ray) Hardened
- Neutron Tolerant
- Identical Pre and Post Electrical Test Conditions
- Avalanche Energy Rating
- Simple Drive Requirements
- Ease of Paralleling
- Dynamic dv/dt Rating
- Hermetically Sealled
- For Automatic Insertion
- 2 N-Channel / 2 P-Channel Co-Packaged HEXFET's

Absolute Maximum Ratings

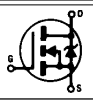
	Parameter	N-Channel	P-Channel	Units
I_D @ V_{GS} = 12V, T_C = 25°C	Continuous Drain Current	3	-2.2	A
I_D @ V_{GS} = 12V, T_C = 100°C	Continuous Drain Current	1.9	-1.4	
I_{DM}	Pulsed Drain Current ①	12	-8.8	
V_{GS}	Gate-to-Source Voltage	± 20		V
E_{AS}	Single Pulse Avalanche Energy	60②	80⑤	mJ
dv/dt	Peak Diode Recovery dv/dt	4.3③	-8.8⑥	V/ns
T_J	Operating Junction	-55 to 150		°C
T_{STG}	Storage Temperature Range			
	Lead Temperature	300 (0.063 in. (1.6mm) from case for 10s)		
	Weight	0.89 (typical)		g

10/13/98

Electrical Characteristics For Each N-Channel Chip @ Tj = 25°C (Unless Otherwise Specified)

	Parameter	Min	Typ	Max	Units	Test Conditions
BV_{DSS}	Drain-to-Source Breakdown Voltage	100	—	—	V	V_{GS} =0 V, I_D = 1.0mA
$\Delta BV_{DSS}/\Delta T_J$	Temperature Coefficient of Breakdown Voltage	—	0.122	—	V/°C	Reference to 25°C, I_D = 1.0mA
$R_{DS(on)}$	Static Drain-to-Source On-State Resistance	—	—	0.38	Ω	V_{GS} = 12V, I_D = 1.9A④
		—	—	0.39		V_{GS} = 12V, I_D = 2.9A④
$V_{GS(th)}$	Gate Threshold Voltage	2.0	—	4.0	V	V_{DS} = V_{GS}, I_D = 1.0mA
g_{fs}	Forward Transconductance	1.1	—	—	S (℧)	V_{DS} ≥ 15V, I_{DS} = 1.9A ④
I_{DSS}	Zero Gate Voltage Drain Current	—	—	25	μA	V_{DS}= 0.8 x Max Rating,V_{GS}=0V
		—	—	250		V_{DS} = 0.8 x Max Rating, V_{GS} = 0V, T_J = 125°C
I_{GSS}	Gate-to-Source Leakage Forward	—	—	100	nA	V_{GS} = 20V
I_{GSS}	Gate-to-Source Leakage Reverse	—	—	-100		V_{GS} = -20V
Q_g	Total Gate Charge	—	—	12	nC	V_{GS} = 12V, I_D =2.9A, V_{DS} = Max Rating x 0.5
Q_{gs}	Gate-to-Source Charge	—	—	3.0		
Q_{gd}	Gate-to-Drain ('Miller') Charge	—	—	5.0		
$t_{d(on)}$	Turn-On Delay Time	—	—	25	ns	V_{DD} = 50V, I_D = 2.9A, R_G = 7.5Ω
t_r	Rise Time	—	—	25		
$t_{d(off)}$	Turn-Off Delay Time	—	—	65		
t_f	Fall Time	—	—	45		
L_D	Internal Drain Inductance	—	4.0	—	nH	Measured from drain lead, 6mm (0.25 in) from package to center of die.
L_S	Internal Source Inductance	—	6.0	—		Measured from source lead, 6mm (0.25 in) from package to source bonding pad.
						Modified MOSFET symbol showing the internal inductances. 
C_{iss}	Input Capacitance	—	270	—	pF	V_{GS} = 0V, V_{DS} = 25V, f = 1.0MHz
C_{oss}	Output Capacitance	—	110	—		
C_{rss}	Reverse Transfer Capacitance	—	23	—		

Source-Drain Diode Ratings and Characteristics

	Parameter	Min	Typ	Max	Units	Test Conditions
I_S	Continuous Source Current (Body Diode)	—	—	3.0	A	Modified MOSFET symbol showing the integral reverse p-n junction rectifier. 
I_{SM}	Pulse Source Current (Body Diode) ①	—	—	12		
V_{SD}	Diode Forward Voltage	—	—	3.6	V	T_j = 25°C, I_S = 2.9A, V_{GS} = 0V ④
t_{rr}	Reverse Recovery Time	—	—	350	ns	T_j = 25°C, I_F = 2.9A, di/dt ≤ 100A/μs
Q_{RR}	Reverse Recovery Charge	—	—	800	nC	V_{DD} ≤ 50V ④
t_{on}	Forward Turn-On Time	Intrinsic turn-on time is negligible. Turn-on speed is substantially controlled by L_S + L_D.				

Electrical Characteristics For Each P-Channel Chip @ Tj = 25°C (Unless Otherwise Specified)

	Parameter	Min	Typ	Max	Units	Test Conditions
BV_{DSS}	Drain-to-Source Breakdown Voltage	-100	—	—	V	V_{GS} =0 V, I_D = -1.0mA
$\Delta BV_{DSS}/\Delta T_J$	Temperature Coefficient of Breakdown Voltage	—	-0.167	—	V/°C	Reference to 25°C, I_D = -1.0mA
$R_{DS(on)}$	Static Drain-to-Source On-State Resistance	—	—	0.88	Ω	V_{GS} = -12V, I_D = -1.3A④
		—	—	0.86		V_{GS} = -12V, I_D = -2.0A④
$V_{GS(th)}$	Gate Threshold Voltage	-2.0	—	-4.0	V	V_{DS} = V_{GS}, I_D = -1.0mA
g_{fs}	Forward Transconductance	1.1	—	—	S (℧)	V_{DS} ≥ -15V, I_{DS} = -1.3A ④
I_{DSS}	Zero Gate Voltage Drain Current	—	—	-25	μA	V_{DS}= 0.8 x Max Rating,V_{GS}=0V
		—	—	-250		V_{DS} = 0.8 x Max Rating, V_{GS} = 0V, T_J = 125°C
I_{GSS}	Gate-to-Source Leakage Forward	—	—	-100	nA	V_{GS} = -20V
I_{GSS}	Gate-to-Source Leakage Reverse	—	—	100		V_{GS} = 20V
Q_g	Total Gate Charge	—	—	11	nC	V_{GS} = -12V, I_D = -2.0A, V_{DS} = Max Rating x 0.5
Q_{gs}	Gate-to-Source Charge	—	—	3.0		
Q_{gd}	Gate-to-Drain ('Miller') Charge	—	—	4.2		
$t_{d(on)}$	Turn-On Delay Time	—	—	25	ns	V_{DD} = -50V, I_D = -2.0A, R_G = 7.5Ω
t_r	Rise Time	—	—	25		
$t_{d(off)}$	Turn-Off Delay Time	—	—	65		
t_f	Fall Time	—	—	45		
L_D	Internal Drain Inductance	—	4.0	—	nH	Measured from drain lead, 6mm (0.25 in) from package to center of die.
L_S	Internal Source Inductance	—	6.0	—		Measured from source lead, 6mm (0.25 in) from package to source bonding pad.
						Modified MOSFET symbol showing the internal inductances. 
C_{iss}	Input Capacitance	—	220	—	pF	V_{GS} = 0V, V_{DS} = -25V, f = 1.0MHz
C_{oss}	Output Capacitance	—	96	—		
C_{rss}	Reverse Transfer Capacitance	—	22	—		

Source-Drain Diode Ratings and Characteristics

	Parameter	Min	Typ	Max	Units	Test Conditions
I_S	Continuous Source Current (Body Diode)	—	—	-2.2	A	Modified MOSFET symbol showing the integral reverse p-n junction rectifier. 
I_{SM}	Pulse Source Current (Body Diode) ①	—	—	-8.8		
V_{SD}	Diode Forward Voltage	—	—	-3.6	V	T_j = 25°C, I_S = -2.0A, V_{GS} = 0V ④
t_{rr}	Reverse Recovery Time	—	—	350	ns	T_j = 25°C, I_F = -2.0A, di/dt ≤ -100A/μs, V_{DD} ≤ -50V ④
Q_{RR}	Reverse Recovery Charge	—	—	325	nC	
t_{on}	Forward Turn-On Time	Intrinsic turn-on time is negligible. Turn-on speed is substantially controlled by L_S + L_D.				

Power Ratings

	Power Ratings Test	Single FET	Two FETs	All Four FETs with Equal Power	Units
P_D @ T_C = 25°C	Max. Power Dissipation per FET	12	11	9	W
	Linear Derating Factor	0.096	0.09	0.08	W/°C
RthJC	Thermal Resistance Junction-to-case	10.4	10.9	11.8	°C/W

Radiation Performance of N-Channel Rad Hard HEXFETs

International Rectifier Radiation Hardened HEXFETs are tested to verify their hardness capability. The hardness assurance program at International Rectifier comprises 3 radiation environments.

Every manufacturing lot is tested in a low dose rate (total dose) environment per MIL-STD-750, test method 1019 condition A. International Rectifier has imposed a standard gate condition of 12 volts per note 7 and a V_{DS} bias condition equal to 80% of the device rated voltage per note 8. Pre and Post-irradiation limits of the devices irradiated to 1x 10^5 Rads (Si) are identical and presented in Table 1, column 1, IRHQ6110. Post-irradiation limits of the devices irradiated to 3x 10^5 Rads (Si) are presented in Table 1, column 2, IRHQ63110. The values in Table 1 will be met for either of the two low dose rate test circuits that are used. Both pre- and post-irradiation performance are tested and specified using the same drive circuitry and test conditions in order to provide a direct comparison. High dose rate testing may be done on a special request basis using a dose rate up to 1 x 10^{12} Rads (Si)/Sec(See Table 2).

International Rectifier radiation hardened HEXFETs are considered to be neutron-tolerant,as stated in MIL-PRF-19500 Group D.

International Rectifier radiation hardened HEXFETs have been characterized in heavy ion Single Event Effects (SEE) environments. Single Event Effects characterization is shown in Table 3.

Table 1. Low Dose Rate ⑦⑧

	Parameter	IRHQ6110 100K Rads (Si) Min	IRHQ6110 100K Rads (Si) Max	IRHQ63110 300K Rads (Si) Min	IRHQ63110 300K Rads (Si) Max	Units	Test Conditions ⑩
BV_{DSS}	Drain-to-Source Breakdown Voltage	100	—	100	—	V	V_{GS} = 0V, I_D = 1.0mA
$V_{GS(th)}$	Gate Threshold Voltage ④	2.0	4.0	1.25	4.5		V_{GS} = V_{DS}, I_D = 1.0mA
I_{GSS}	Gate-to-Source Leakage Forward	—	100	—	100	nA	V_{GS} = 20V
I_{GSS}	Gate-to-Source Leakage Reverse	—	-100	—	-100		V_{GS} = -20 V
I_{DSS}	Zero Gate Voltage Drain Current	—	25	—	25	µA	V_{DS}=0.8 x Max Rating, V_{GS} =0V
$R_{DS(on)1}$	Static Drain-to-Source ④ On-State Resistance One	—	0.38	—	0.38	Ω	V_{GS} = 12V, I_D = 1.9A
V_{SD}	Diode Forward Voltage ④	—	3.6	—	3.6	V	T_C = 25°C, I_S = 2.9A,V_{GS} = 0V

Table 2. High Dose Rate ⑨

	Parameter	10^{11} Rads (Si)/sec Min	Typ	Max	10^{12} Rads (Si)/sec Min	Typ	Max	Units	Test Conditions
V_{DSS}	Drain-to-Source Voltage	—	—	80	—	—	80	V	Applied drain-to-source voltage during gamma-dot
I_{PP}		—	25	—	—	25	—	A	Peak radiation induced photo-current
di/dt		—	—	800	—	—	160	A/µsec	Rate of rise of photo-current
L_1		0.1	—	—	0.5	—	—	µH	Circuit inductance required to limit di/dt

Table 3. Single Event Effects

Ion	LET (Si) (MeV/mg/cm²)	Fluence (ions/cm²)	Range (µm)	V_{DS}Bias (V)	V_{GS} Bias (V)
Cu	28	3x 10^5	~43	100	-5

Radiation Performance of P-Channel Rad Hard HEXFETs

International Rectifier Radiation Hardened HEXFETs are tested to verify their hardness capability. The hardness assurance program at International Rectifier comprises 3 radiation environments.

Every manufacturing lot is tested in a low dose rate (total dose) environment per MIL-STD-750, test method 1019 condition A. International Rectifier has imposed a standard gate condition of -12 volts per note 7 and a V_{DS} bias condition equal to 80% of the device rated voltage per note 8. Pre and Post-irradiation limits of the devices irradiated to 1x 10^5 Rads (Si) are identical and presented in Table 4, column 1, IRHQ6110. Post-irradiation limits of the devices irradiated to 3x 10^5 Rads (Si) are presented in Table 4, column 2, IRHQ63110. The values in Table 4 will be met for either of the two low dose rate test circuits that are used. Both pre- and post-irradiation performance are tested and specified using the same drive circuitry and test conditions in order to provide a direct comparison. High dose rate testing may be done on a special request basis using a dose rate up to 1 x 10^{12} Rads (Si)/Sec(See Table 5).

International Rectifier radiation hardened HEXFETs are considered to be neutron-tolerant,as stated in MIL-PRF-19500 Group D. It should be noted that at a radiation level of 3x10^5K Rads(Si) the only parametric limit change is $V_{GS(th)}$ Maximum.

International Rectifier radiation hardened HEXFETs have been characterized in heavy ion Single Event Effects (SEE) environments. Single Event Effects characterization is shown in Table 6.

Table 4. Low Dose Rate ⑦⑧

		IRHQ6110		IRHQ63110			
	Parameter	100K Rads (Si)		300K Rads (Si)		**Units**	**Test Conditions** ⑩
		Min	**Max**	**Min**	**Max**		
BV_{DSS}	Drain-to-Source Breakdown Voltage	-100	—	-100	—	V	V_{GS} = 0V, I_D = -1.0mA
$V_{GS(th)}$	Gate Threshold Voltage ④	-2.0	-4.0	-2.0	-5.0		V_{GS} = V_{DS}, I_D = -1.0mA
I_{GSS}	Gate-to-Source Leakage Forward	—	-100	—	-100	nA	V_{GS} = -20V
I_{GSS}	Gate-to-Source Leakage Reverse	—	100	—	100		V_{GS} = 20 V
I_{DSS}	Zero Gate Voltage Drain Current	—	-25	—	-25	µA	V_{DS}=0.8 x Max Rating, V_{GS} =0V
$R_{DS(on)1}$	Static Drain-to-Source ④ On-State Resistance One	—	0.88	—	0.88	Ω	V_{GS} = 12V, I_D = -1.3A
V_{SD}	Diode Forward Voltage ④	—	-3.6	—	-3.6	V	T_C = 25°C, I_S = -2.0A,V_{GS} = 0V

Table 5. High Dose Rate ⑨

		10^{11} Rads (Si)/sec			10^{12} Rads (Si)/sec				
	Parameter	**Min**	**Typ**	**Max**	**Min**	**Typ**	**Max**	**Units**	**Test Conditions**
V_{DSS}	Drain-to-Source Voltage	—	—	-80	—	—	-80	V	Applied drain-to-source voltage during gamma-dot
I_{PP}		—	-25	—	—	-25	—	A	Peak radiation induced photo-current
di/dt		—	—	-800	—	—	-160	A/µsec	Rate of rise of photo-current
L_1		0.1	—	—	0.5	—	—	µH	Circuit inductance required to limit di/dt

Table 6. Single Event Effects

Ion	**LET (Si)** (MeV/mg/cm^2)	**Fluence** (ions/cm^2)	**Range** (µm)	**V_{DS}Bias** (V)	**V_{GS} Bias** (V)
Cu	28	3x 10^5	~43	-100	5

N-Channel
O2, Q4

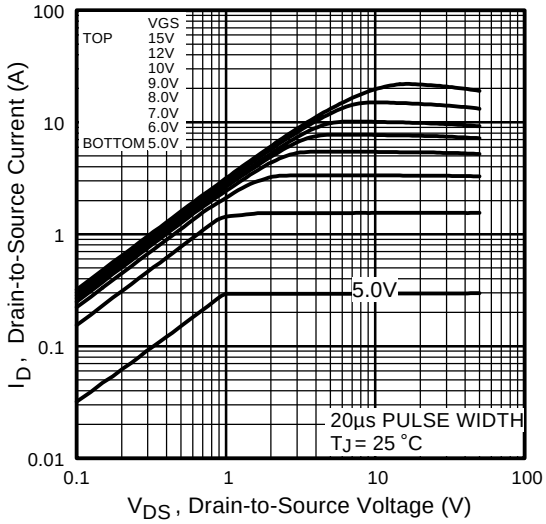


Fig 1. Typical Output Characteristics

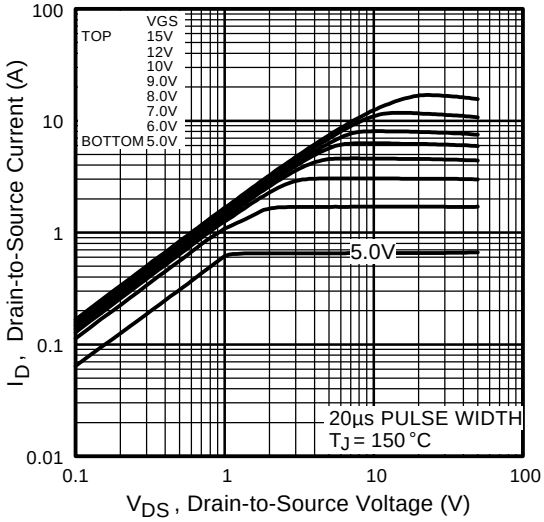


Fig 2. Typical Output Characteristics

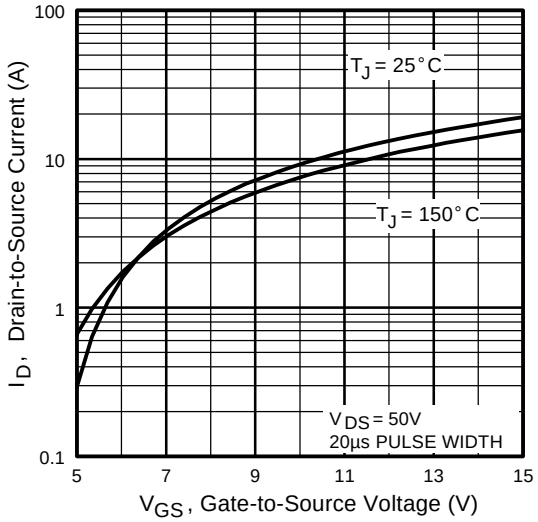


Fig 3. Typical Transfer Characteristics

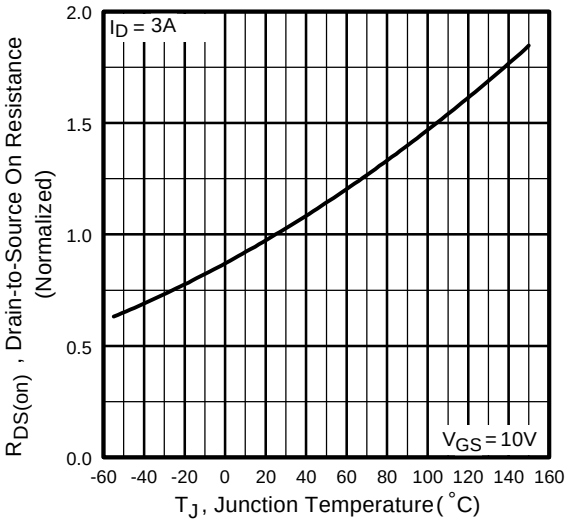


Fig 4. Normalized On-Resistance Vs. Temperature

N-Channel
Q2, Q4

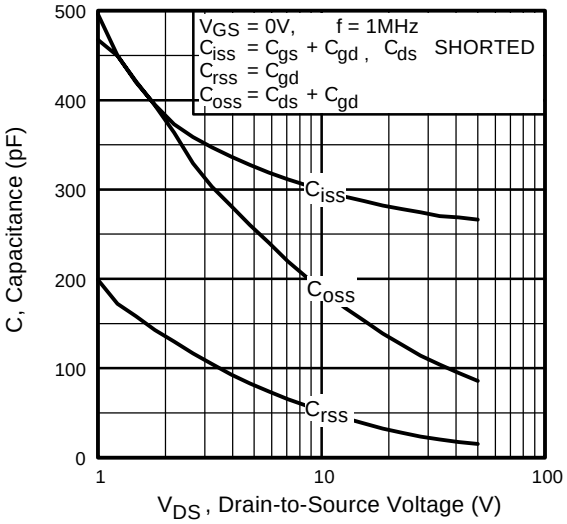


Fig 5. Typical Capacitance Vs. Drain-to-Source Voltage

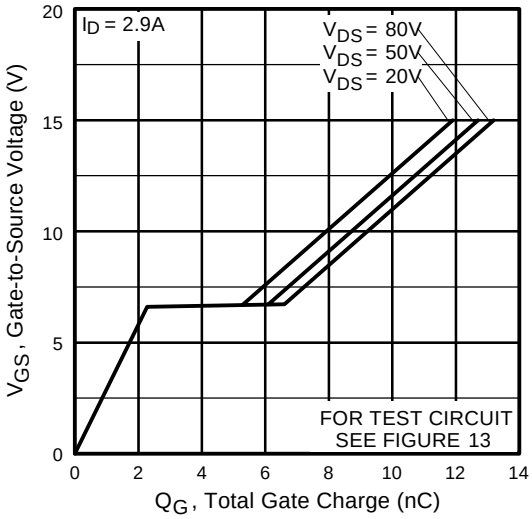


Fig 6. Typical Gate Charge Vs. Gate-to-Source Voltage

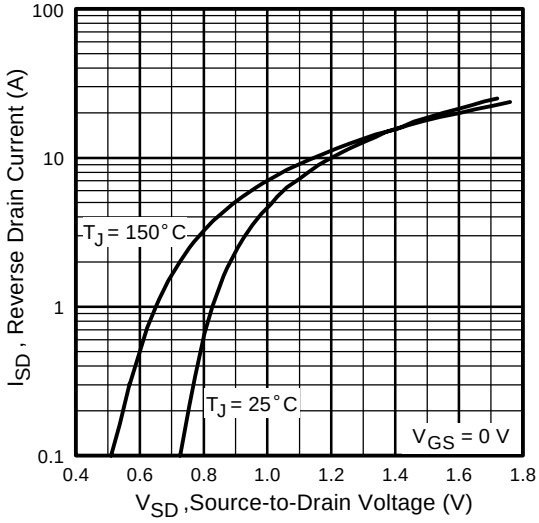


Fig 7. Typical Source-Drain Diode Forward Voltage

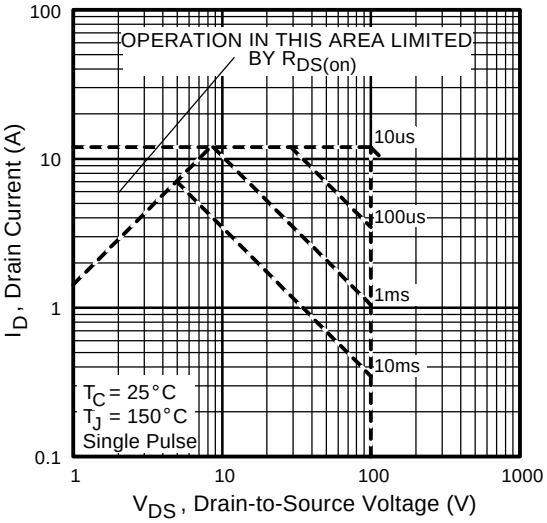


Fig 8. Maximum Safe Operating Area

N-Channel
Q2, Q4

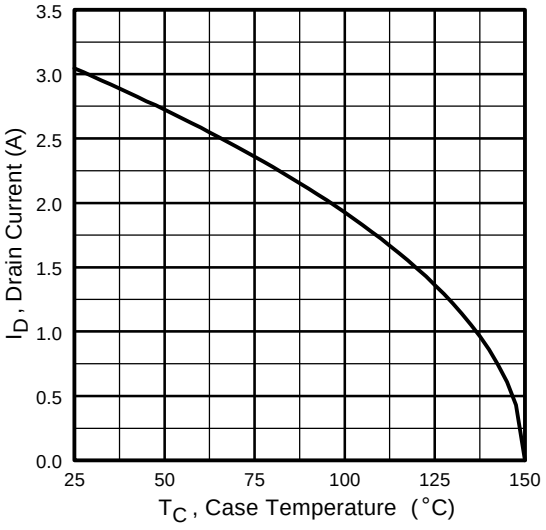


Fig 9. Maximum Drain Current Vs. Case Temperature

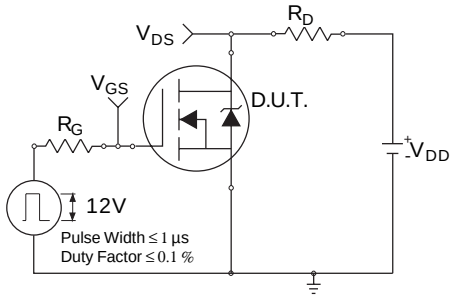


Fig 10a. Switching Time Test Circuit

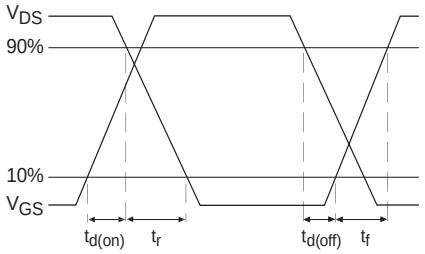


Fig 10b. Switching Time Waveforms

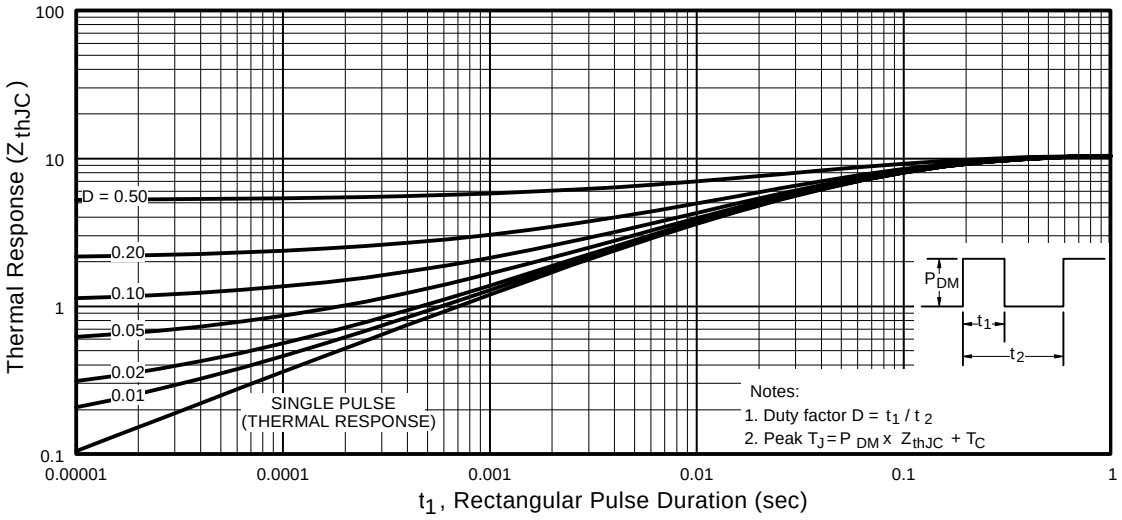


Fig 11. Maximum Effective Transient Thermal Impedance, Junction-to-Case

N-Channel
Q2, Q4

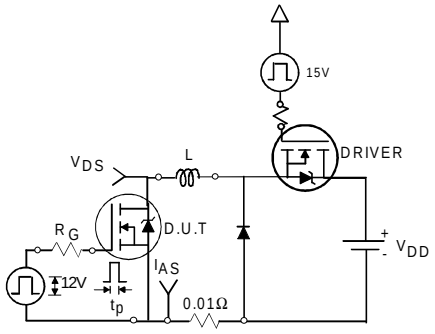


Fig 12a. Unclamped Inductive Test Circuit

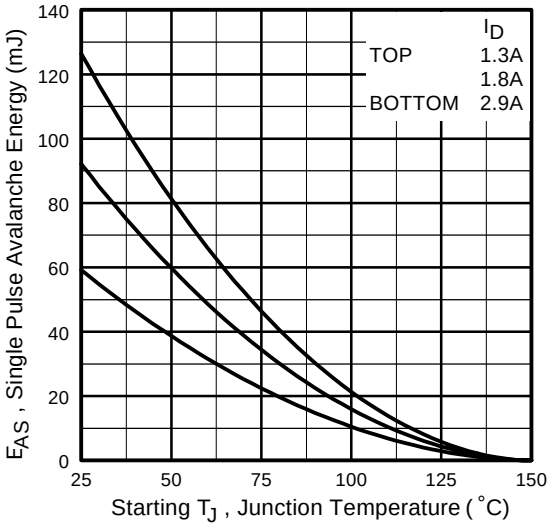


Fig 12c. Maximum Avalanche Energy Vs. Drain Current

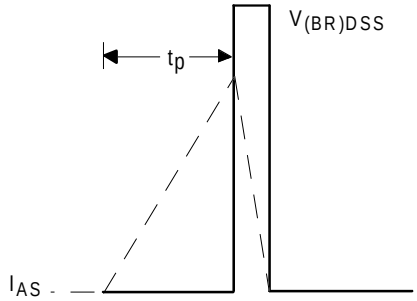


Fig 12b. Unclamped Inductive Waveforms

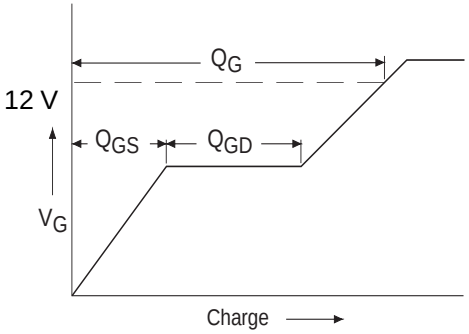


Fig 13a. Basic Gate Charge Waveform

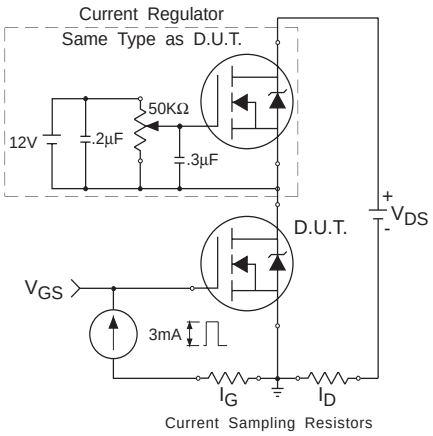


Fig 13b. Gate Charge Test Circuit

P-Channel
Q1, Q3

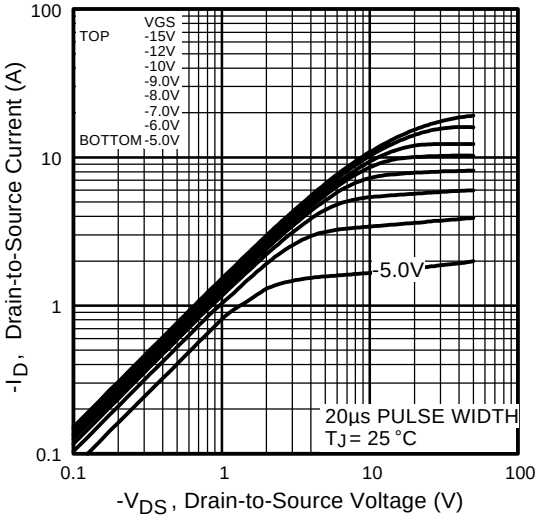


Fig 14. Typical Output Characteristics

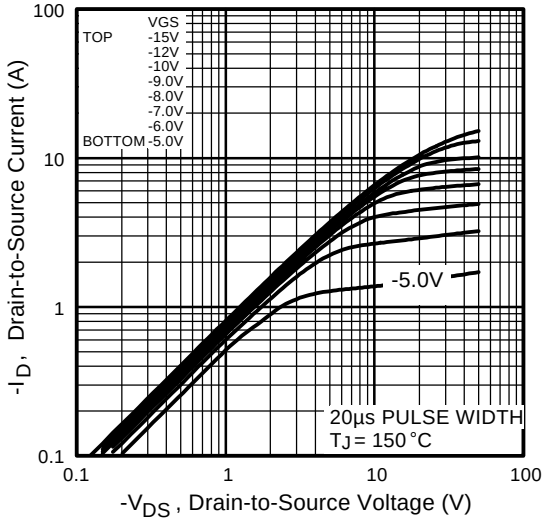


Fig 15. Typical Output Characteristics

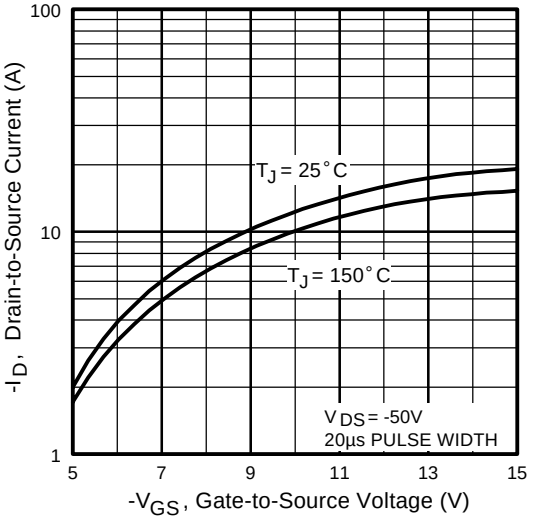


Fig 16. Typical Transfer Characteristics

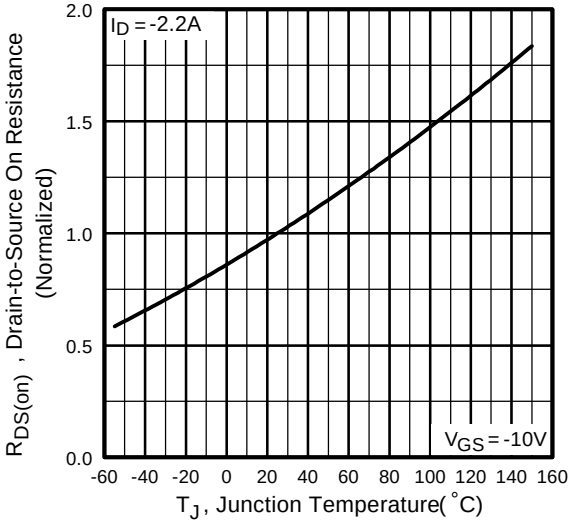


Fig 17. Normalized On-Resistance Vs. Temperature

P-Channel
Q1, Q3

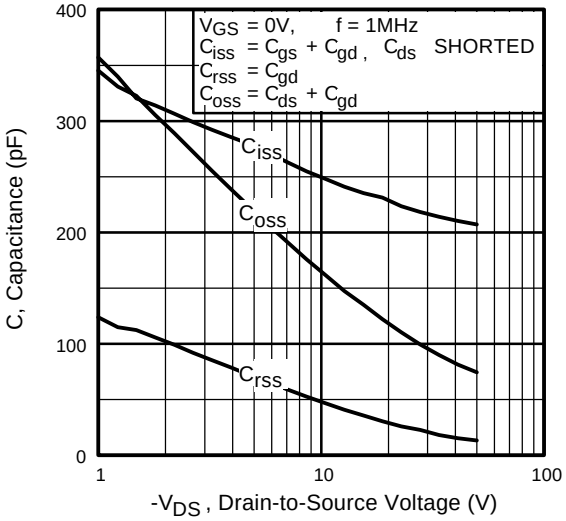


Fig 18. Typical Capacitance Vs. Drain-to-Source Voltage

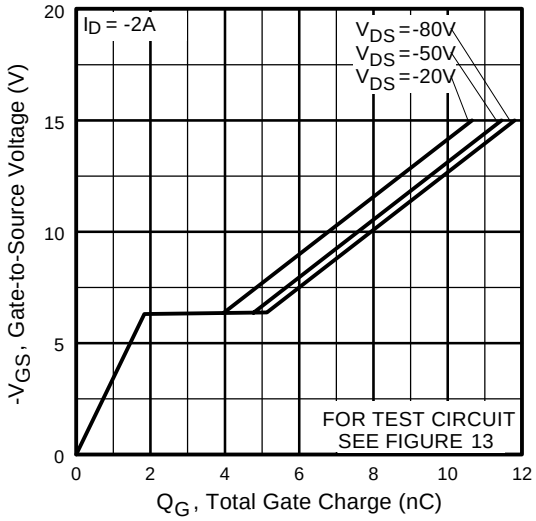


Fig 19. Typical Gate Charge Vs. Gate-to-Source Voltage

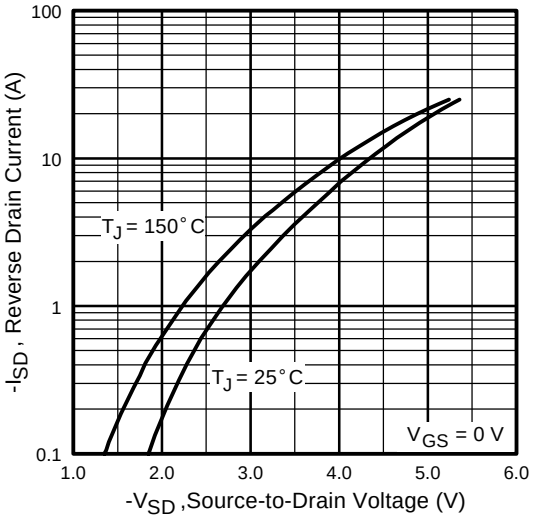


Fig 20. Typical Source-Drain Diode Forward Voltage

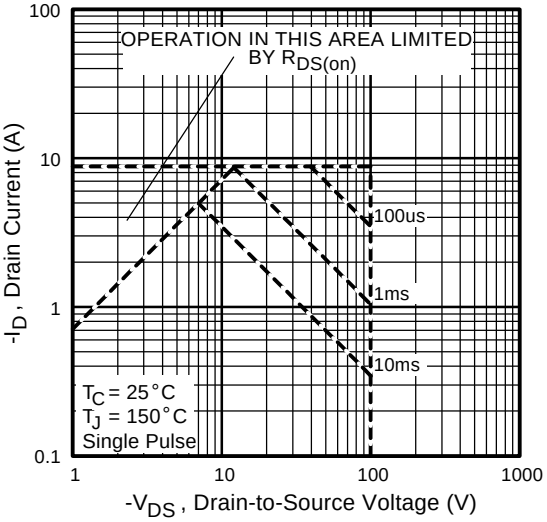


Fig 21. Maximum Safe Operating Area

P-Channel
Q1, Q3

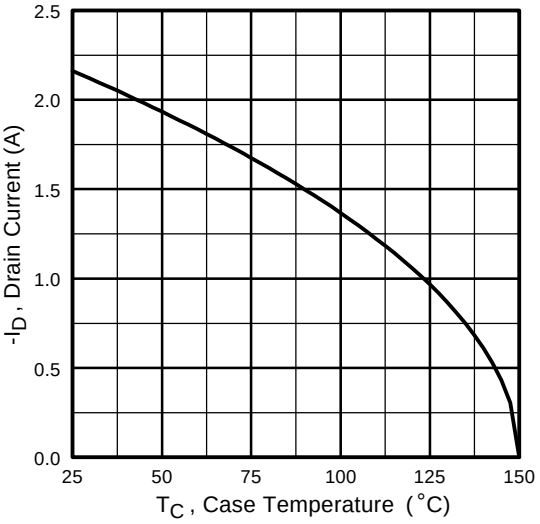


Fig 22. Maximum Drain Current Vs. Case Temperature

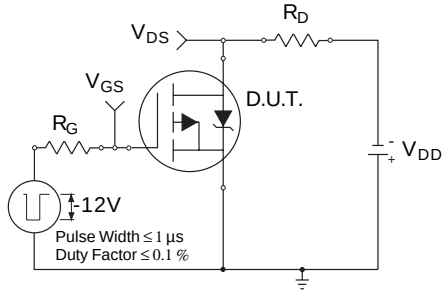


Fig 23a. Switching Time Test Circuit

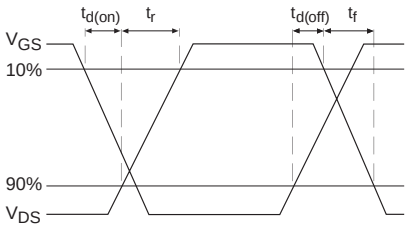


Fig 23b. Switching Time Waveforms

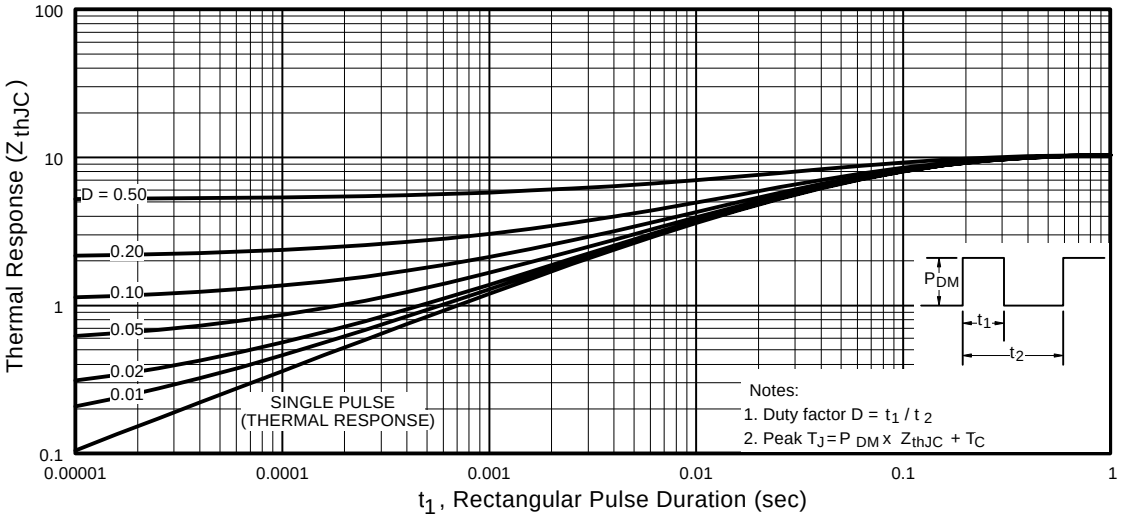


Fig 24. Maximum Effective Transient Thermal Impedance, Junction-to-Case

P-Channel
Q1, Q3

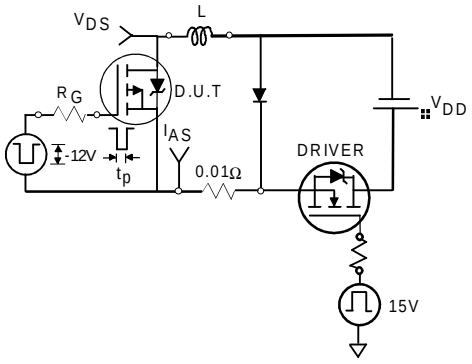


Fig 25a. Unclamped Inductive Test Circuit

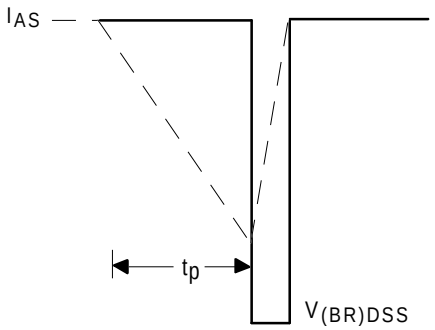


Fig 25b. Unclamped Inductive Waveforms

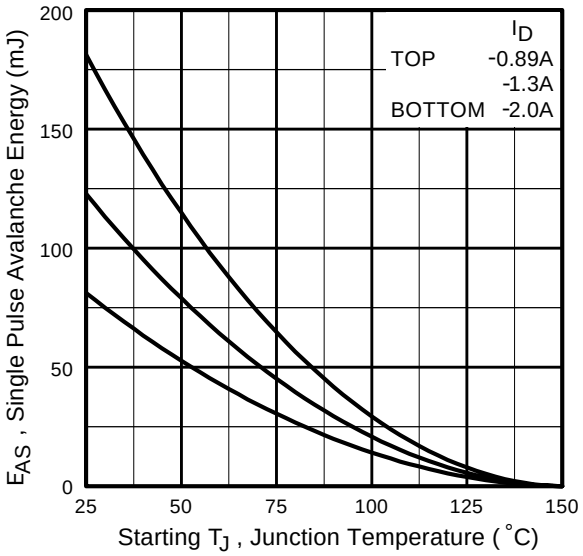


Fig 25c. Maximum Avalanche Energy Vs. Drain Current

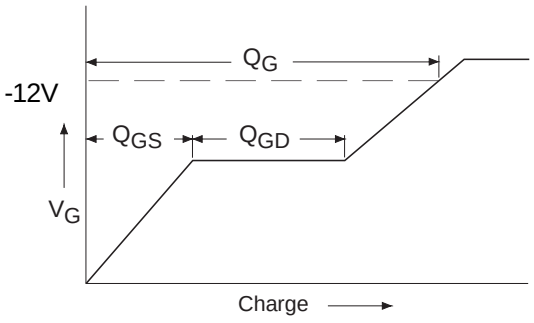


Fig 26a. Basic Gate Charge Waveform

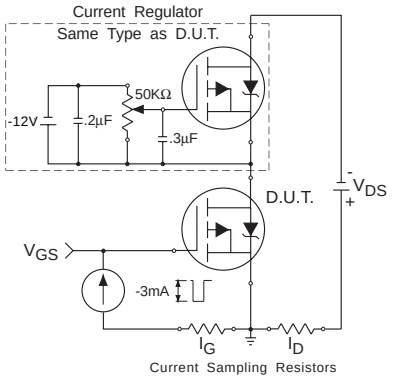


Fig 26b. Gate Charge Test Circuit

Notes:

① Repetitive Rating; Pulse width limited by maximum junction temperature. Refer to current HEXFET reliability report.

② Starting T_J = 25°C, V_{DD} = 50V
E_{AS} = [0.5 * L * (I_L^2)]
Peak I_L = 2.9A, 25 ≤ R_G ≤ 200Ω

③ I_{SD} ≤ 2.9A, di/dt ≤ 31A/µs,
V_{DD} ≤ BV_{DSS}, T_J ≤ 150°C
Suggested RG = 7.5Ω

④ Pulse width ≤ 300 µs; Duty Cycle ≤ 2%

⑤ Starting T_J = 25°C, V_{DD} = -50V
E_{AS} = [0.5 * L * (I_L^2)]
Peak I_L = -2.0A, 25 ≤ R_G ≤ 200Ω

⑥ I_{SD} ≤ -2.0A, di/dt ≤ -23A/µs,
V_{DD} ≤ BV_{DSS}, T_J ≤ 150°C
Suggested RG = 7.5Ω

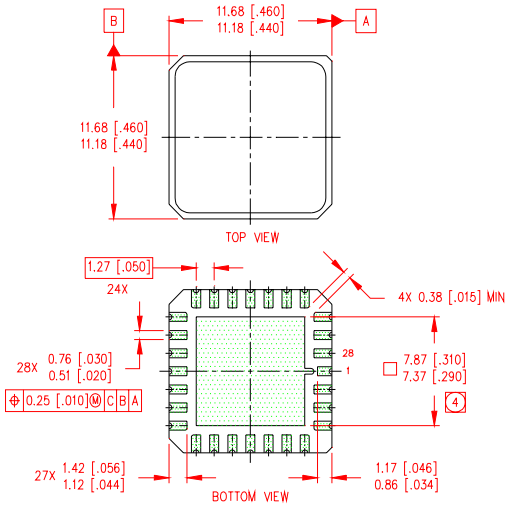
⑦ **Total Dose Irradiation with V_{GS} Bias.** 12 volt V_{GS} applied and V_{DS} = 0 during irradiation per MIL-STD-750, method 1019, condition A.

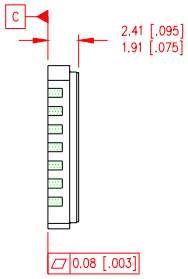
⑧ **Total Dose Irradiation with V_{DS} Bias.** V_{DS} = 0.8 rated BV_{DSS} (pre-irradiation) applied and V_{GS} = 0 during irradiation per MIL-STD -750, method 1019, condition A.

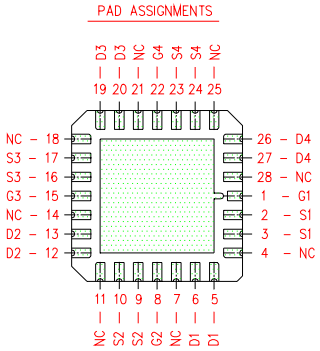
⑨ This test is performed using a flash x-ray source operated in the e-beam mode (energy ~2.5 MeV), 30 nsec pulse.

⑩ All Pre-Irradiation and Post-Irradiation test conditions are **identical** to facilitate direct comparison for circuit applications.

Case Outline and Dimensions — 28 Pin - LCC







LEGEND

G = GATE S = SOURCE
D = DRAIN NC = NO CONNECTION

NOTES:
1. DIMENSIONING & TOLERANCING PER ASME Y14.5M–1994.
2. CONTROLLING DIMENSION: INCH
3. DIMENSIONS ARE SHOWN IN MILLIMETERS [INCHES].
④ DIMENSION INDICATES SIZE OF HEATSINK METALLIZATION.

International
IOR Rectifier

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IR ITALY: Via Liguria 49, 10071 Borgaro, Torino Tel: ++ 39 11 451 0111
IR FAR EAST: K&H Bldg., 2F, 30-4 Nishi-Ikebukuro 3-Chome, Toshima-Ku, Tokyo Japan 171 Tel: 81 3 3983 0086
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