International
IOR Rectifier

REPETITIVE AVALANCHE AND dv/dt RATED
HEXFET® TRANSISTOR

IRHNA7460SE

N-CHANNEL
SINGLE EVENT EFFECT (SEE) RAD HARD

500Volt, 0.32Ω, (SEE) RAD HARD HEXFET

International Rectifier's (SEE) RAD HARD technology HEXFETs demonstrate immunity to SEE failure. These devices are also capable of surviving transient ionization pulses as high as 1 x 10^{12} Rads (Si)/Sec, and return to normal operation within a few microseconds. Since the SEE process utilizes International Rectifier's patented HEXFET technology, the user can expect the highest quality and reliability in the industry.

RAD HARD HEXFET transistors also feature all of the well-established advantages of MOSFETs, such as voltage control, very fast switching, ease of paralleling and temperature stability of the electrical parameters. They are well-suited for applications such as switching power supplies, motor controls, inverters, choppers, audio amplifiers and high-energy pulse circuits in space and weapons environments.

Product Summary

Part Number	BV_{DSS}	$R_{DS(on)}$	I_D
IRHNA7460SE	500V	0.32Ω	20A

Features:

- Radiation Hardened up to 1 x 10^5 Rads (Si)
- Single Event Burnout (SEB) Hardened
- Single Event Gate Rupture (SEGR) Hardened
- Gamma Dot (Flash X-Ray) Hardened
- Neutron Tolerant
- Identical Pre- and Post-Electrical Test Conditions
- Repetitive Avalanche Rating
- Dynamic dv/dt Rating
- Simple Drive Requirements
- Ease of Paralleling
- Hermetically Sealed
- Surface Mount
- Light Weight

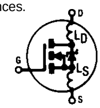
Absolute Maximum Ratings

Pre-Irradiation

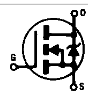
	Parameter	IRHNA7460SE	Units
I_D @ V_{GS} = 12V, T_C = 25°C	Continuous Drain Current	20	A
I_D @ V_{GS} = 12V, T_C = 100°C	Continuous Drain Current	12	
I_{DM}	Pulsed Drain Current ①	80	
P_D @ T_C = 25°C	Max. Power Dissipation	300	W
	Linear Derating Factor	2.4	W/K ⑤
V_{GS}	Gate-to-Source Voltage	±20	V
E_{AS}	Single Pulse Avalanche Energy ②	500	mJ
I_{AR}	Avalanche Current ①	20	A
E_{AR}	Repetitive Avalanche Energy ①	30	mJ
dv/dt	Peak Diode Recovery dv/dt ③	3.8	V/ns
T_J T_{STG}	Operating Junction Storage Temperature Range	-55 to 150	°C
	Package Mounting Surface Temperature	300 (for 5 sec.)	
	Weight	3.3 (typical)	g

7/2/98

Electrical Characteristics @ Tj = 25°C (Unless Otherwise Specified)

	Parameter	Min	Typ	Max	Units	Test Conditions
BV_{DSS}	Drain-to-Source Breakdown Voltage	500	—	—	V	V_{GS} = 0V, I_D = 1.0mA
$\Delta BV_{DSS}/\Delta T_J$	Temperature Coefficient of Breakdown Voltage	—	0.66	—	V/°C	Reference to 25°C, I_D = 1.0mA
$R_{DS(on)}$	Static Drain-to-Source On-State Resistance	—	—	0.32	Ω	V_{GS} = 12V, I_D = 12A ④
		—	—	0.36		V_{GS} = 12V, I_D = 20A
$V_{GS(th)}$	Gate Threshold Voltage	2.5	—	4.5	V	V_{DS} = V_{GS}, I_D = 1.0mA
g_{fs}	Forward Transconductance	6.0	—	—	S (℧)	V_{DS} > 15V, I_{DS} = 12A ④
I_{DSS}	Zero Gate Voltage Drain Current	—	—	50	µA	V_{DS}= 0.8 x Max Rating, V_{GS}=0V
		—	—	250		V_{DS} = 0.8 x Max Rating V_{GS} = 0V, T_J = 125°C
I_{GSS}	Gate-to-Source Leakage Forward	—	—	100	nA	V_{GS} = 20V
I_{GSS}	Gate-to-Source Leakage Reverse	—	—	-100		V_{GS} = -20V
Q_g	Total Gate Charge	—	—	220	nC	V_{GS} = 12V, I_D = 20A V_{DS} = Max Rating x 0.5
Q_{gs}	Gate-to-Source Charge	—	—	50		
Q_{gd}	Gate-to-Drain ('Miller') Charge	—	—	110		
$t_{d(on)}$	Turn-On Delay Time	—	—	35	ns	V_{DD} = 250V, I_D = 20A, R_G = 2.35Ω
t_r	Rise Time	—	—	100		
$t_{d(off)}$	Turn-Off Delay Time	—	—	100		
t_f	Fall Time	—	—	100		
L_D	Internal Drain Inductance	—	0.8	—	nH	Measured from drain lead, 6mm (0.25 in) from package to center of die. Modified MOSFET symbol showing the internal inductances. 
L_S	Internal Source Inductance	—	2.8	—		Measured from source lead, 6mm (0.25 in) from package to source bonding pad.
C_{iss}	Input Capacitance	—	3500	—	pF	V_{GS} = 0V, V_{DS} = 25V f = 1.0MHz
C_{oss}	Output Capacitance	—	730	—		
C_{rss}	Reverse Transfer Capacitance	—	260	—		

Source-Drain Diode Ratings and Characteristics

	Parameter	Min	Typ	Max	Units	Test Conditions
I_S	Continuous Source Current (Body Diode)	—	—	20	A	Modified MOSFET symbol showing the integral reverse p-n junction rectifier. 
I_{SM}	Pulse Source Current (Body Diode) ①	—	—	80		
V_{SD}	Diode Forward Voltage	—	—	1.8	V	T_j = 25°C, I_S = 20A, V_{GS} = 0V ④
t_{rr}	Reverse Recovery Time	—	—	800	ns	T_j = 25°C, I_F = 20A, di/dt ≤ 100A/µs V_{DD} ≤ 50V ④
Q_{RR}	Reverse Recovery Charge	—	—	16	µC	
t_{on}	Forward Turn-On Time	Intrinsic turn-on time is negligible. Turn-on speed is substantially controlled by L_S + L_D.				

Thermal Resistance

	Parameter	Min	Typ	Max	Units	Test Conditions
R_{thJC}	Junction-to-Case	—	—	0.42	K/W ⑤	
$R_{thJ-PCB}$	Junction-to-PC board	—	1.6	—		soldered to a 2" square copper-clad board

Radiation Performance of Rad Hard HEXFETs

International Rectifier Radiation Hardened HEXFETs are tested to verify their hardness capability. The hardness assurance program at International Rectifier comprises three radiation environments.

Every manufacturing lot is tested in a low dose rate (total dose) environment per MIL-STD-750, test method 1019 condition A. International Rectifier has imposed a standard gate condition of 12 volts per note 6 and a V_{DS} bias condition equal to 80% of the device rated voltage per note 7. Post-irradiation limits of the devices irradiated to 1 x 10^5 Rads (Si) are presented in Table 1, column 1, IRHNA7460SE. The values in Table 1 will be met for either of the two low dose rate test circuits that are used. Both pre- and post-irradiation performance are tested and specified using the same drive circuitry and test conditions in order to provide a direct comparison. It should be noted that at a radiation level of 1 x 10^5 Rads (Si) the only parametric limit change is V_{GSTh} minimum.

High dose rate testing may be done on a special request basis using a dose rate up to 1 x 10^{12} Rads (Si)/Sec (See Table 2).

International Rectifier radiation hardened HEXFETs have been characterized in heavy ion Single Event Effects (SEE) environments. Single Event Effects characterization is shown in Table 3.

Table 1. Low Dose Rate ⑥ ⑦

	Parameter	IRHNA7460SE 100K Rads (Si)		Units	Test Conditions ⑨
		Min	Max		
BV_{DSS}	Drain-to-Source Breakdown Voltage	500	—	V	V_{GS} = 0V, I_D = 1.0mA
$V_{GS(th)}$	Gate Threshold Voltage ④	2.0	4.5		V_{GS} = V_{DS}, I_D = 1.0mA
I_{GSS}	Gate-to-Source Leakage Forward	—	100	nA	V_{GS} = 20V
I_{GSS}	Gate-to-Source Leakage Reverse	—	-100		V_{GS} = -20V
I_{DSS}	Zero Gate Voltage Drain Current	—	50	µA	V_{DS}=0.8 x Max Rating, V_{GS}=0V
$R_{DS(on)1}$	Static Drain-to-Source ④ On-State Resistance One	—	0.32	Ω	V_{GS} = 12V, I_D = 12A
V_{SD}	Diode Forward Voltage ④	—	1.8	V	T_C = 25°C, I_S =20A, V_{GS} = 0V

Table 2. High Dose Rate ⑧

	Parameter	10^{11} Rads (Si)/sec			10^{12} Rads (Si)/sec			Units	Test Conditions
		Min	Typ	Max	Min	Typ	Max		
V_{DSS}	Drain-to-Source Voltage	—	—	400	—	—	400	V	Applied drain-to-source voltage during gamma-dot
I_{PP}		—	7.0	—	—	7.0	—	A	Peak radiation induced photo-current
di/dt		—	16	—	—	2.3	—	A/µsec	Rate of rise of photo-current
L_1		—	27	—	—	133	—	µH	Circuit inductance required to limit di/dt

Table 3. Single Event Effects

Ion	LET (Si) (MeV/mg/cm²)	Fluence (ions/cm²)	Range (µm)	V_{DS} Bias (V)	V_{GS} Bias (V)
Cu	28	3x 10^5	~43	375	-5

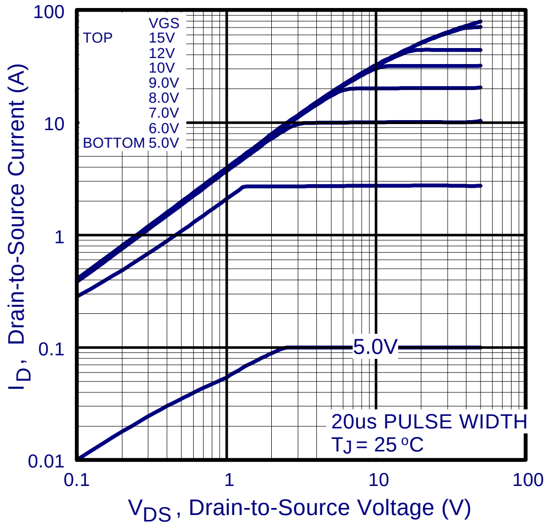


Fig 1. Typical Output Characteristics

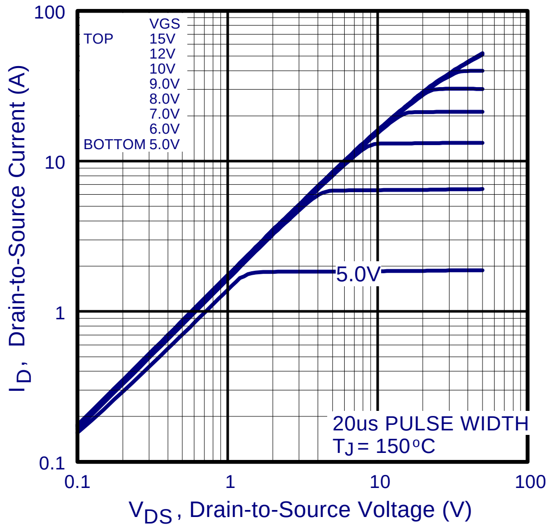


Fig 2. Typical Output Characteristics

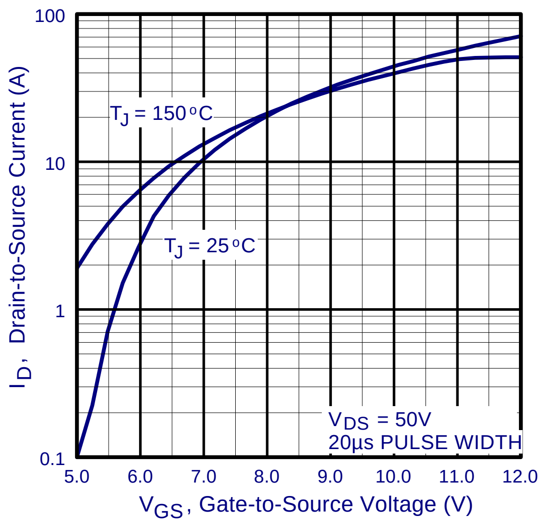


Fig 3. Typical Transfer Characteristics

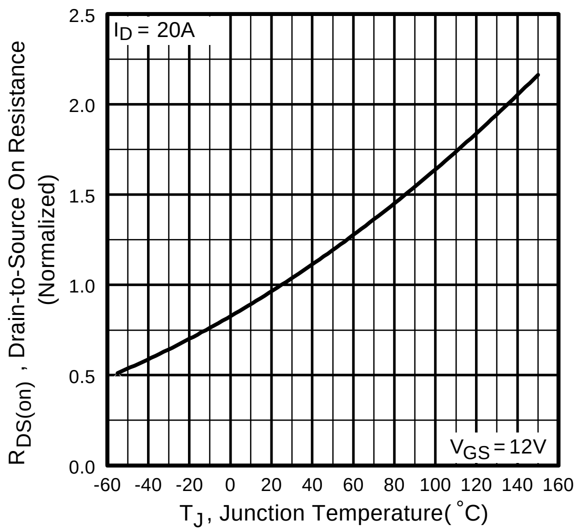


Fig 4. Normalized On-Resistance Vs. Temperature

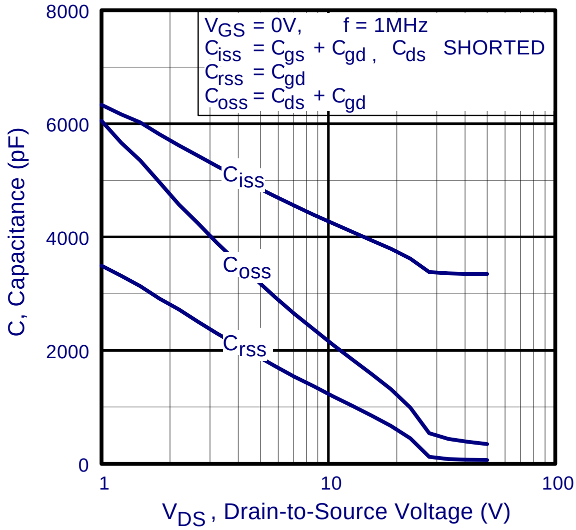


Fig 5. Typical Capacitance Vs. Drain-to-Source Voltage

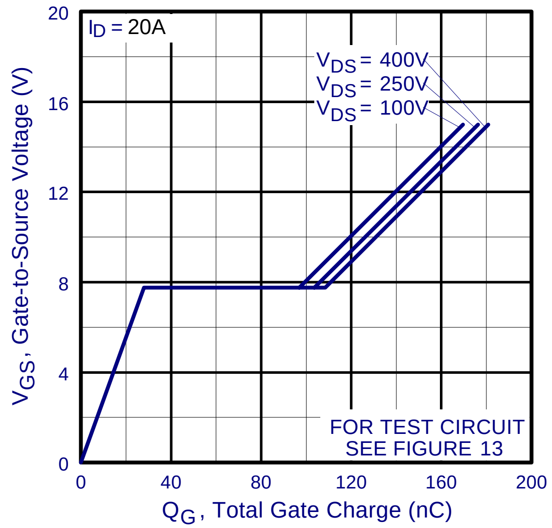


Fig 6. Typical Gate Charge Vs. Gate-to-Source Voltage

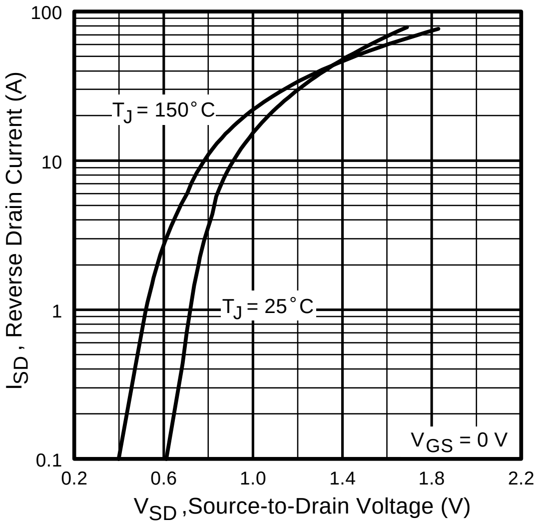


Fig 7. Typical Source-Drain Diode Forward Voltage

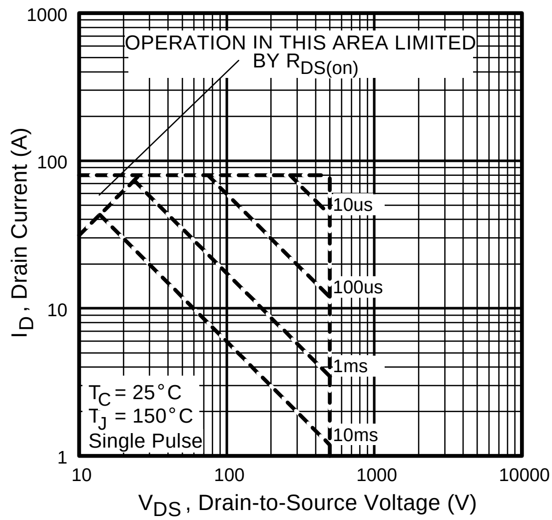


Fig 8. Maximum Safe Operating Area

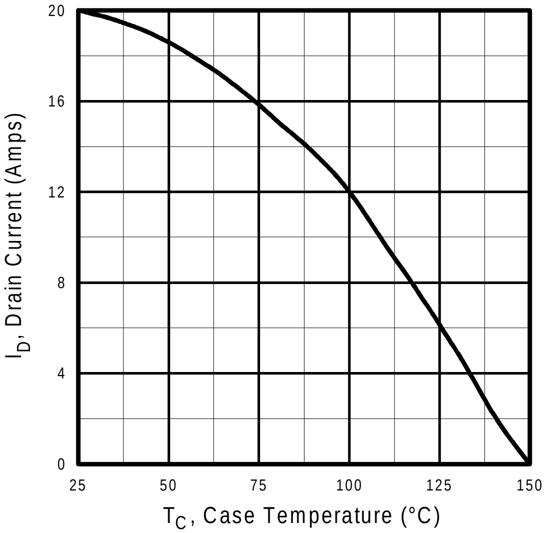


Fig 9. Maximum Drain Current Vs. Case Temperature

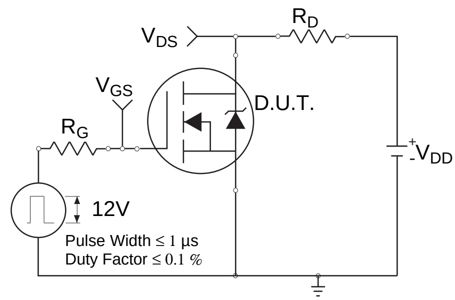


Fig 10a. Switching Time Test Circuit

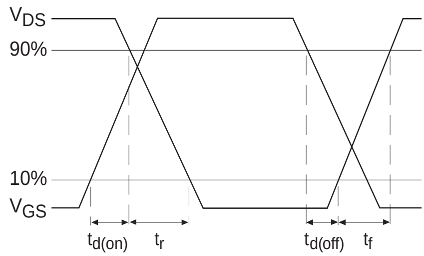


Fig 10b. Switching Time Waveforms

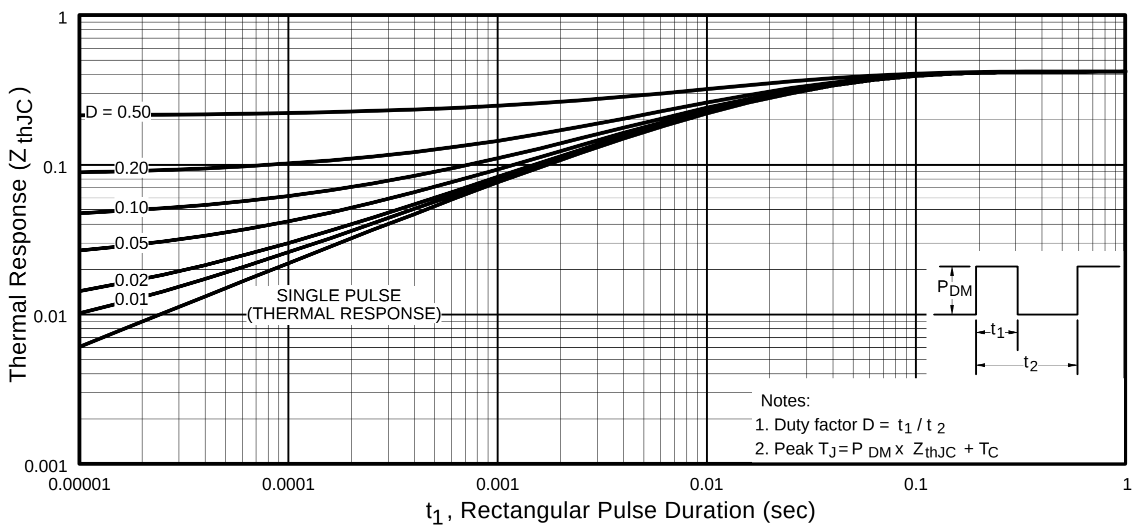


Fig 11. Maximum Effective Transient Thermal Impedance, Junction-to-Case

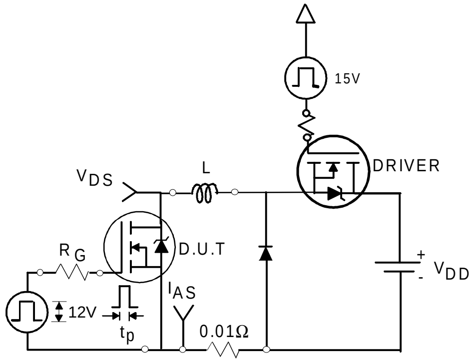


Fig 12a. Unclamped Inductive Test Circuit

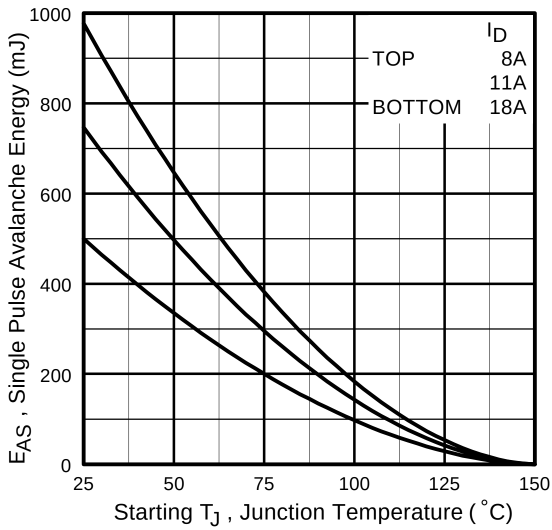


Fig 12c. Maximum Avalanche Energy Vs. Drain Current

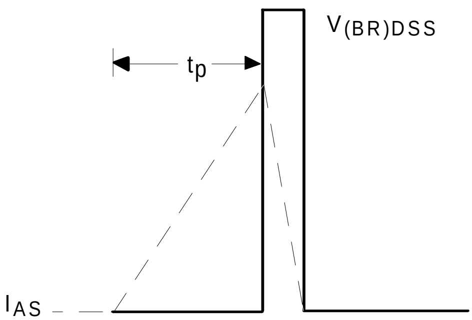


Fig 12b. Unclamped Inductive Waveforms

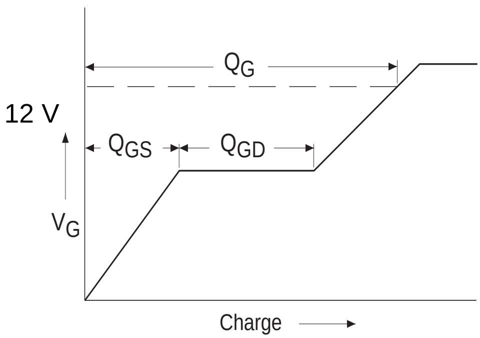


Fig 13a. Basic Gate Charge Waveform

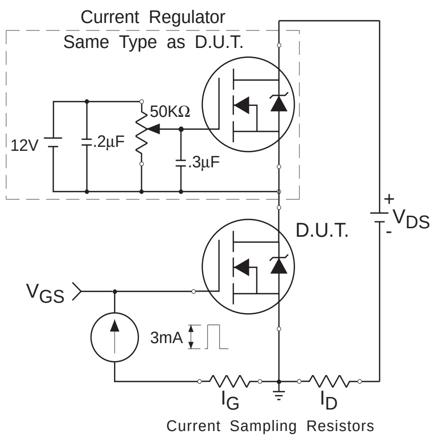


Fig 13b. Gate Charge Test Circuit

① Repetitive Rating; Pulse width limited by maximum junction temperature. Refer to current HEXFET reliability report.

② @ V_{DD} = 50V, starting T_J = 25°C, $E_{AS} = [0.5 * L * (I_L^2)]$ Peak I_L = 20A, V_{GS} = 12V, 25 ≤ R_G ≤ 200Ω

③ I_{SD} ≤ 20A, di/dt ≤ 120A/µs, V_{DD} ≤ BV_{DSS}, T_J ≤ 150°C Suggested RG = 2.35Ω

④ Pulse width ≤ 300 µs; Duty Cycle ≤ 2%

⑤ K/W = °C/W W/K = W/°C

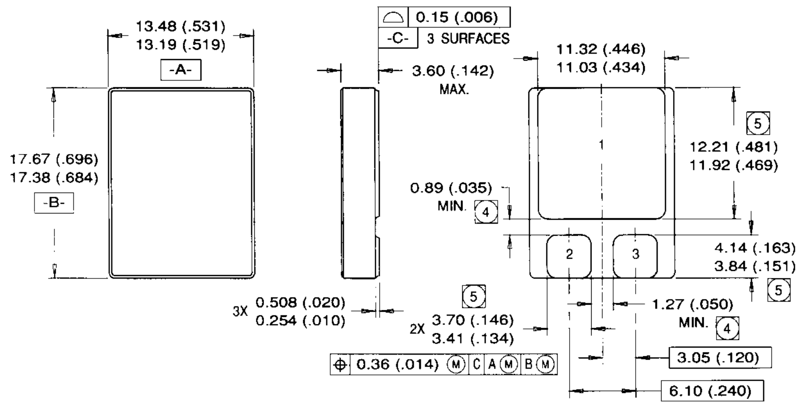
⑥ **Total Dose Irradiation with V_{GS} Bias.** 12 volt V_{GS} applied and V_{DS} = 0 during irradiation per MIL-STD-750, method 1019, condition A.

⑦ **Total Dose Irradiation with V_{DS} Bias.** V_{DS} = 0.8 rated BV_{DSS} (pre-irradiation) applied and V_{GS} = 0 during irradiation per MIL-STD-750, method 1019, condition A.

⑧ This test is performed using a flash x-ray source operated in the e-beam mode (energy ~2.5 MeV), 30 nsec pulse.

⑨ All Pre-Irradiation and Post-Irradiation test conditions are **identical** to facilitate direct comparison for circuit applications.

Case Outline and Dimensions — SMD-2



NOTES:

1. DIMENSIONING & TOLERANCING PER ANSI Y14.5M-1982
2. CONTROLLING DIMENSION: INCH.
3. DIMENSIONS ARE SHOWN IN MILLIMETERS (INCHES).

④ DIMENSION INCLUDES METALLIZATION FLASH.

⑤ DIMENSION DOES NOT INCLUDE METALLIZATION FLASH.

LEAD ASSIGNMENTS

1 = DRAIN
2 = GATE
3 = SOURCE

SMD-2

International
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