International
IOR Rectifier

PD - 90713B

REPETITIVE AVALANCHE AND dv/dt RATED
HEXFET® TRANSISTOR

IRHE7230
IRHE8230
N CHANNEL
MEGA RAD HARD

200Volt, 0.35Ω, MEGA RAD HARD HEXFET

International Rectifier's RAD HARD technology HEXFETs demonstrate excellent threshold voltage stability and breakdown voltage stability at total radiaition doses as high as 1x10^6 Rads(Si). Under **identical** pre- and post-irradiation test conditions, International Rectifier's RAD HARD HEXFETs retain **identical** electrical specifications up to 1 x 10^5 Rads (Si) total dose. No compensation in gate drive circuitry is required. These devices are also capable of surviving transient ionization pulses as high as 1 x 10^{12} Rads (Si)/Sec, and return to normal operation within a few microseconds. Since the RAD HARD process utilizes International Rectifier's patented HEXFET technology, the user can expect the highest quality and reliability in the industry.

RAD HARD HEXFET transistors also feature all of the well-established advantages of MOSFETs, such as voltage control, very fast switching, ease of paralleling and temperature stability of the electrical parameters. They are well-suited for applications such as switching power supplies, motor controls, inverters, choppers, audio amplifiers and high-energy pulse circuits in space and weapons environments.

Product Summary

Part Number	BV_{DSS}	$R_{DS(on)}$	I_D
IRHE7230	200V	0.35Ω	5.5A
IRHE8230	200V	0.35Ω	5.5A

Features:

- Radiation Hardened up to 1 x 10^6 Rads (Si)
- Single Event Burnout (SEB) Hardened
- Single Event Gate Rupture (SEGR) Hardened
- Gamma Dot (Flash X-Ray) Hardened
- Neutron Tolerant
- Identical Pre- and Post-Electrical Test Conditions
- Repetitive Avalanche Rating
- Dynamic dv/dt Rating
- Simple Drive Requirements
- Ease of Paralleling
- Hermetically Sealed
- Surface Mount
- Lightweight

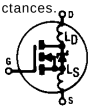
Absolute Maximum Ratings ①

Pre-Irradiation

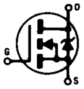
	Parameter	IRHE7230, IRHE8230	Units
I_D @ V_{GS} = 12V, T_C = 25°C	Continuous Drain Current	5.5	A
I_D @ V_{GS} = 12V, T_C = 100°C	Continuous Drain Current	3.5	
I_{DM}	Pulsed Drain Current ②	22	
P_D @ T_C = 25°C	Max. Power Dissipation	25	W
	Linear Derating Factor	0.2	W/°C
V_{GS}	Gate-to-Source Voltage	±20	V
E_{AS}	Single Pulse Avalanche Energy ③	240	mJ
dv/dt	Peak Diode Recovery dv/dt ④	5.0	V/ns
T_J T_{STG}	Operating Junction Storage Temperature Range	-55 to 150	°C
	Lead Temperature	300 (0.063 in. (1.6mm) from case for 10s)	
	Weight	0.42 (typical)	g

10/13/98

Electrical Characteristics @ Tj = 25°C (Unless Otherwise Specified) ①

	Parameter	Min	Typ	Max	Units	Test Conditions
BV_{DSS}	Drain-to-Source Breakdown Voltage	200	—	—	V	V_{GS} = 0V, I_D = 1.0mA
$\Delta BV_{DSS}/\Delta T_J$	Temperature Coefficient of Breakdown Voltage	—	0.25	—	V/°C	Reference to 25°C, I_D = 1.0mA
$R_{DS(on)}$	Static Drain-to-Source On-State Resistance	—	—	0.35	Ω	V_{GS} = 12V, I_D = 3.5A ⑤
		—	—	0.36		V_{GS} = 12V, I_D = 5.5A ⑤
$V_{GS(th)}$	Gate Threshold Voltage	2.0	—	4.0	V	V_{DS} = V_{GS}, I_D = 1.0mA
g_{fs}	Forward Transconductance	2.5	—	—	S (℧)	V_{DS} > 15V, I_{DS} = 3.5A ⑤
I_{DSS}	Zero Gate Voltage Drain Current	—	—	25	µA	V_{DS}= 0.8 x Max Rating,V_{GS}=0V
		—	—	250		V_{DS} = 0.8 x Max Rating V_{GS} = 0V, T_J = 125°C
I_{GSS}	Gate-to-Source Leakage Forward	—	—	100	nA	V_{GS} = 20V
I_{GSS}	Gate-to-Source Leakage Reverse	—	—	-100		V_{GS} = -20V
Q_g	Total Gate Charge	—	—	50	nC	V_{GS} =12V, I_D = 5.5A V_{DS} = Max Rating x 0.5
Q_{gs}	Gate-to-Source Charge	—	—	10		
Q_{gd}	Gate-to-Drain ('Miller') Charge	—	—	25		
$t_{d(on)}$	Turn-On Delay Time	—	—	25	ns	V_{DD} = 100V, I_D = 5.5A, R_G = 7.5Ω
t_r	Rise Time	—	—	40		
$t_{d(off)}$	Turn-Off Delay Time	—	—	60		
t_f	Fall Time	—	—	45		
L_D	Internal Drain Inductance	—	1.8	—	nH	Measured from drain lead, 6mm (0.25 in) from package to center of die. Modified MOSFET symbol showing the internal inductances. 
L_S	Internal Source Inductance	—	4.3	—		Measured from source lead, 6mm (0.25 in) from package to source bonding pad.
C_{iss}	Input Capacitance	—	1100		pF	V_{GS} = 0V, V_{DS} = 25V f = 1.0MHz
C_{oss}	Output Capacitance	—	250	—		
C_{rss}	Reverse Transfer Capacitance	—	55	—		

Source-Drain Diode Ratings and Characteristics ①

	Parameter	Min	Typ	Max	Units	Test Conditions
I_S	Continuous Source Current (Body Diode)	—	—	5.5	A	Modified MOSFET symbol showing the integral reverse p-n junction rectifier. 
I_{SM}	Pulse Source Current (Body Diode) ②	—	—	22		
V_{SD}	Diode Forward Voltage	—	—	1.4	V	T_j = 25°C, I_S = 5.5A, V_{GS} = 0V ⑤
t_{rr}	Reverse Recovery Time	—	—	400	ns	T_j = 25°C, I_F = 5.5A, di/dt ≤ 100A/µs V_{DD} ≤ 50V ⑤
Q_{RR}	Reverse Recovery Charge	—	—	3.0	µC	
t_{on}	Forward Turn-On Time	Intrinsic turn-on time is negligible. Turn-on speed is substantially controlled by L_S + L_D.				

Thermal Resistance

	Parameter	Min	Typ	Max	Units	Test Conditions
R_{thJC}	Junction-to-Case	—	—	5.0	°C/W	
$R_{th\text{-}PCB}$	Junction-to-Ambient	—	19	—		Solder to a copper clad PC Board

Radiation Performance of Rad Hard HEXFETs

International Rectifier Radiation Hardened HEXFETs are tested to verify their hardness capability. The hardness assurance program at International Rectifier comprises three radiation environments.

Every manufacturing lot is tested in a low dose rate (total dose) environment per MIL-STD-750, test method 1019 condition A. International Rectifier has imposed a standard gate condition of 12 volts per note 6 and a V_{DS} bias condition equal to 80% of the device rated voltage per note 7. Pre- and post- irradiation limits of the devices irradiated to 1 x 10^5 Rads (Si) are identical and are presented in Table 1, column 1, IRHE7230. Post-irradiation limits of the devices irradiated to 1 x 10^6 Rads (Si) are presented in Table 1, column 2, IRHE8230. The values in Table 1 will be met for either of the two low dose rate test circuits that are used. Both pre- and post-irradiation performance are tested and specified using the same drive circuitry and test conditions in order to provide a direct comparison.

High dose rate testing may be done on a special request basis using a dose rate up to 1 x 10^{12} Rads (Si)/Sec (See Table 2).

International Rectifier radiation hardened HEXFETs have been characterized in heavy ion Single Event Effects (SEE) environments. Single Event Effects characterization is shown in Table 3.

Table 1. Low Dose Rate ⑥ ⑦

	Parameter	IRHE7230 100K Rads (Si)		IRHE8230 1000K Rads (Si)		Units	Test Conditions ⑨
		Min	Max	Min	Max		
BV_{DSS}	Drain-to-Source Breakdown Voltage	200	—	200	—	V	V_{GS} = 0V, I_D = 1.0mA
$V_{GS(th)}$	Gate Threshold Voltage ⑤	2.0	4.0	1.25	4.5		V_{GS} = V_{DS}, I_D = 1.0mA
I_{GSS}	Gate-to-Source Leakage Forward	—	100	—	100	nA	V_{GS} = 20V
I_{GSS}	Gate-to-Source Leakage Reverse	—	-100	—	-100		V_{GS} = -20 V
I_{DSS}	Zero Gate Voltage Drain Current	—	25	—	50	µA	V_{DS}=0.8 x Max Rating, V_{GS} =0V
$R_{DS(on)1}$	Static Drain-to-Source ⑤ On-State Resistance One	—	1.225	—	1.68	Ω	V_{GS} = 12V, I_D = 3.5A
V_{SD}	Diode Forward Voltage ⑤	—	1.4	—	1.4	V	T_C = 25°C, I_S =5.5A, V_{GS} = 0V

Table 2. High Dose Rate ⑧

	Parameter	10^{11} Rads (Si)/sec			10^{12} Rads (Si)/sec			Units	Test Conditions
		Min	Typ	Max	Min	Typ	Max		
V_{DSS}	Drain-to-Source Voltage	—	—	160	—	—	160	V	Applied drain-to-source voltage during gamma-dot
I_{PP}		—	20	—	—	20	—	A	Peak radiation induced photo-current
di/dt		—	—	160	—	—	8.0	A/µsec	Rate of rise of photo-current
L_1		1.0	—	—	20	—	—	µH	Circuit inductance required to limit di/dt

Table 3. Single Event Effects

Ion	LET (Si) (MeV/mg/cm^2)	Fluence (ions/cm^2)	Range (µm)	V_{DS} Bias (V)	V_{GS} Bias (V)
Cu	28	3x 10^5	~43	180	-5

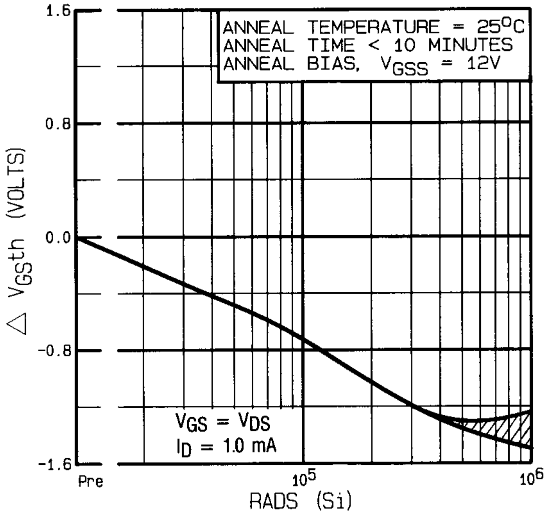


Fig 1. Typical Response of Gate Threshhold Voltage Vs. Total Dose Exposure

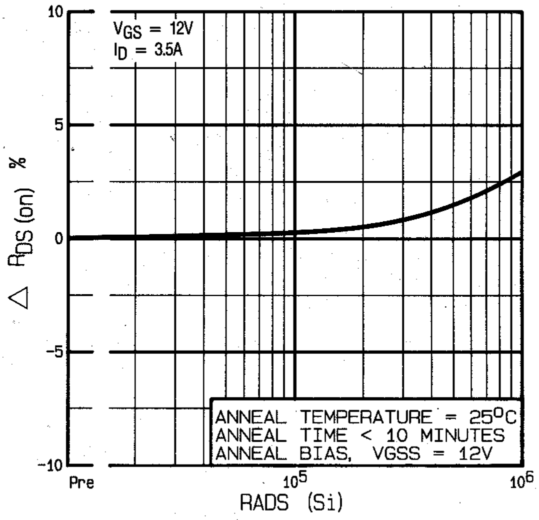


Fig 2. Typical Response of On-State Resistance Vs. Total Dose Exposure

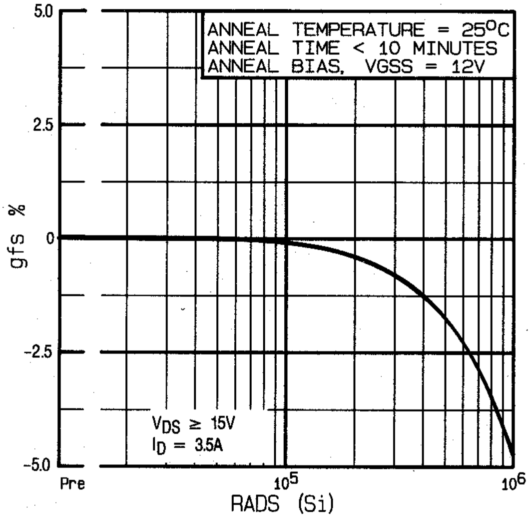


Fig 3. Typical Response of Transconductance Vs. Total Dose Exposure

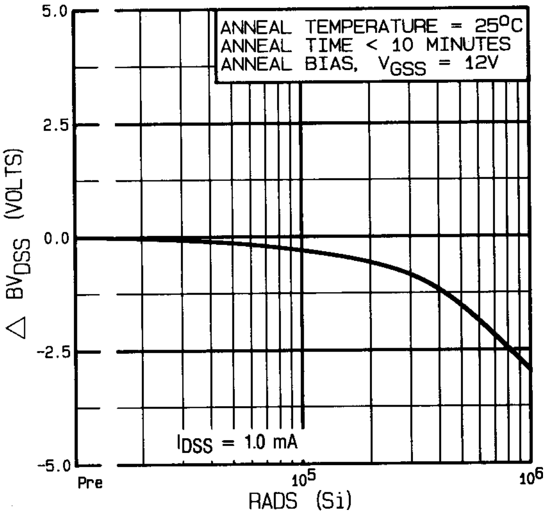


Fig 4. Typical Response of Drain to Source Breakdown Vs. Total Dose Exposure

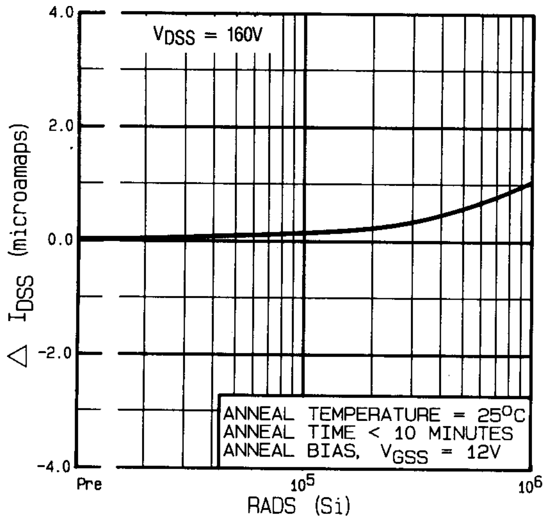


Fig 5. Typical Zero Gate Voltage Drain Current Vs. Total Dose Exposure

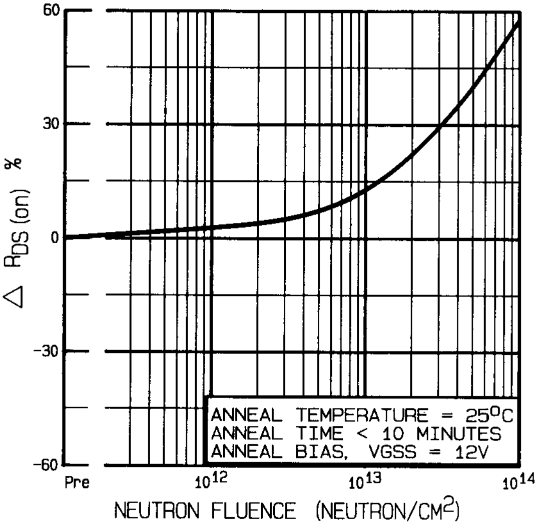


Fig 6. Typical On-State Resistance Vs. Neutron Fluence Level

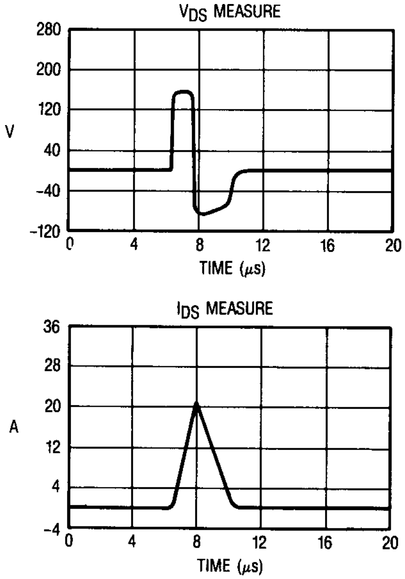


Fig 7. Typical Transient Response of Rad Hard HEXFET During 1x10^{12} Rad (Si)/Sec Exposure

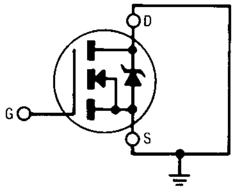


Fig 8a. Gate Stress of V_{GSS} Equals 12 Volts During Radiation

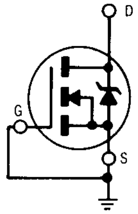


Fig 8b. V_{DSS} Stress Equals 80% of B_{VDSS} During Radiation

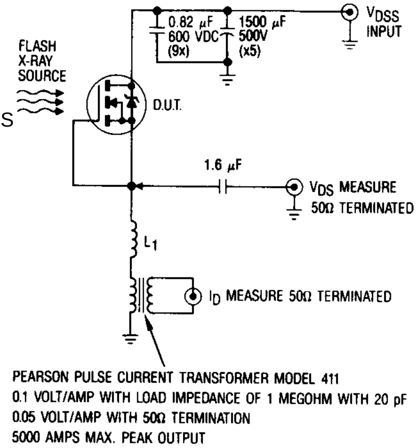


Fig 9. High Dose Rate (Gamma Dot) Test Circuit

Note: Bias Conditions during radiation: V_{GS} = 12 Vdc, V_{DS} = 0 Vdc

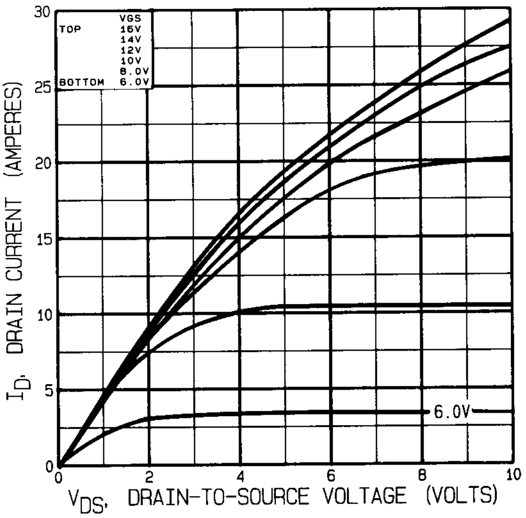


Fig 10. Typical Output Characteristics Pre-Irradiation

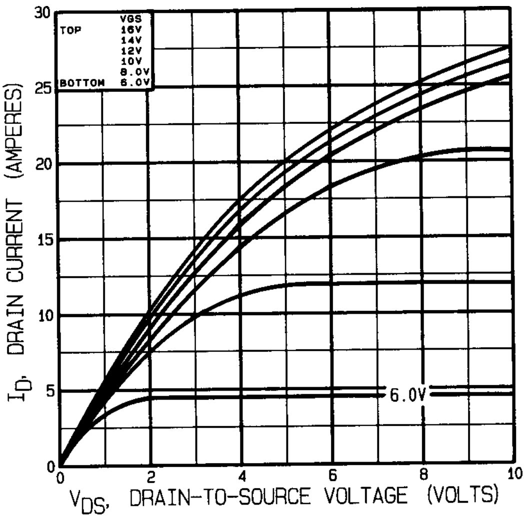


Fig 11. Typical Output Characteristics Post-Irradiation 100K Rads (Si)

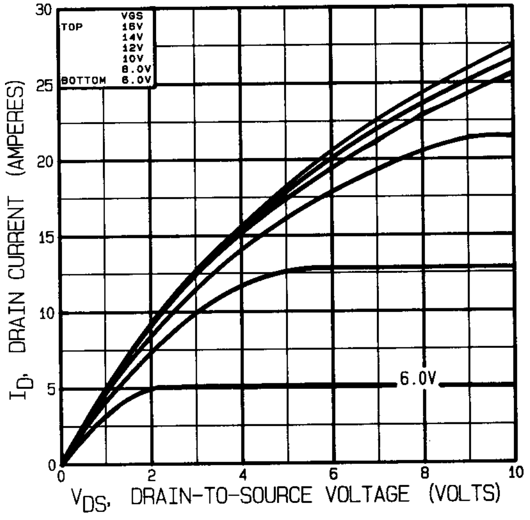


Fig 12. Typical Output Characteristics Post-Irradiation 300K Rads (Si)

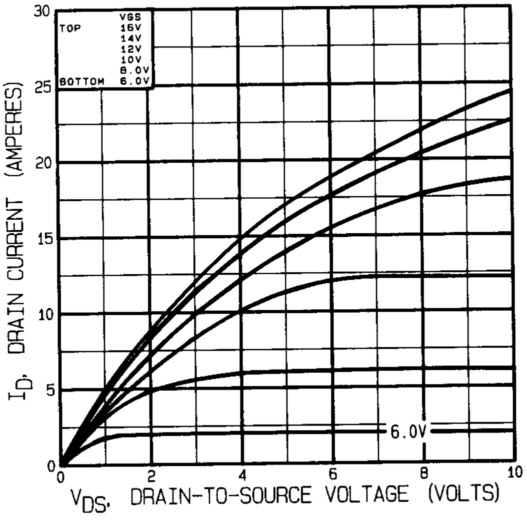


Fig 13. Typical Output Characteristics Post-Irradiation 1 Mega Rads (Si)

Note: Bias Conditions during radiation: V_{GS} = 0 Vdc, V_{DS} = 160 Vdc

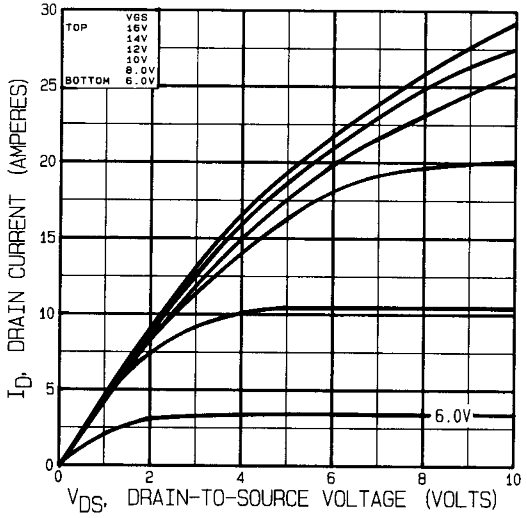


Fig 14. Typical Output Characteristics Pre-Irradiation

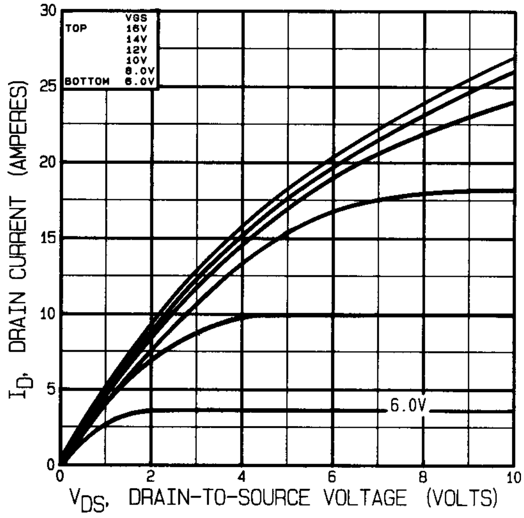


Fig 15. Typical Output Characteristics Post-Irradiation 100K Rads (Si)

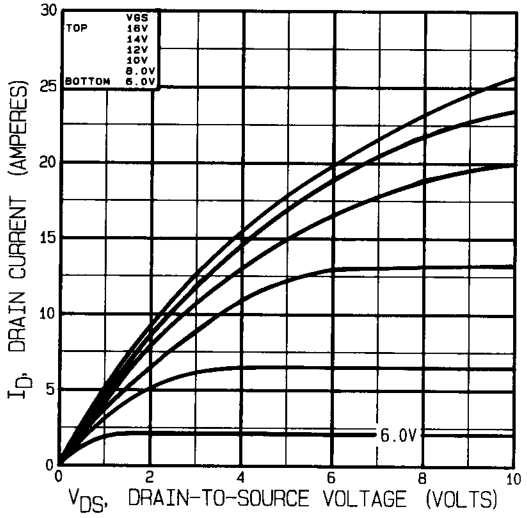


Fig 16. Typical Output Characteristics Post-Irradiation 300K Rads (Si)

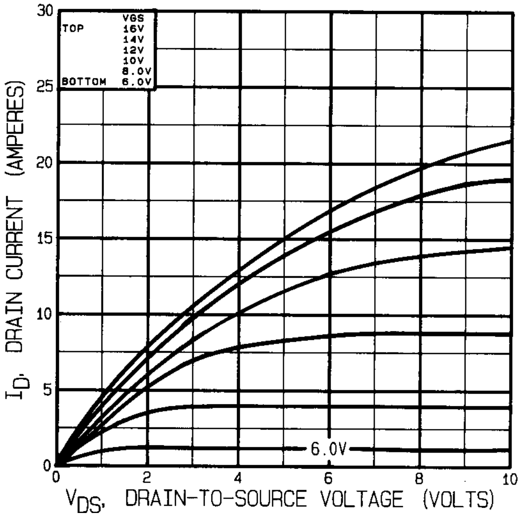


Fig 17. Typical Output Characteristics Post-Irradiation 1 Mega Rads (Si)

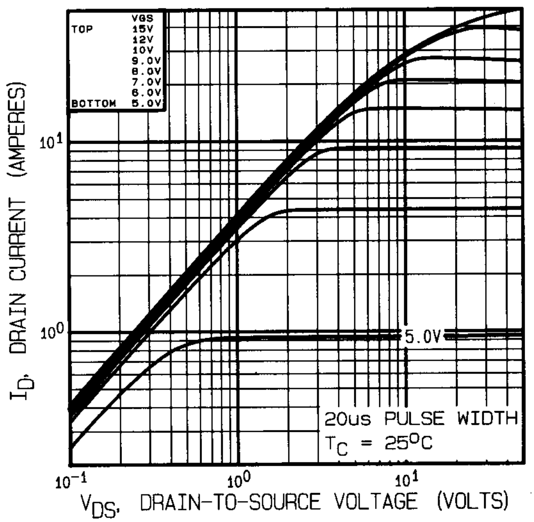


Fig 18. Typical Output Characteristics

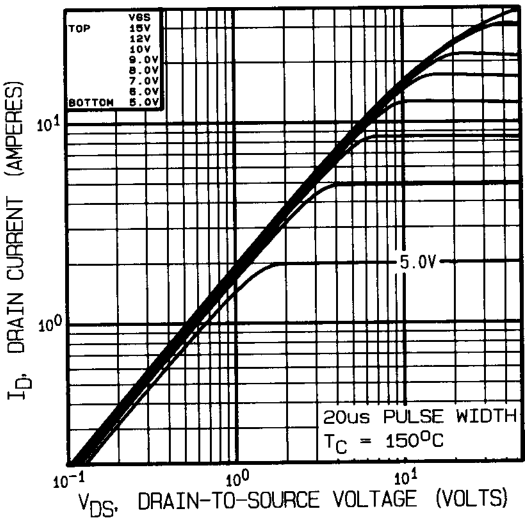


Fig 19. Typical Output Characteristics

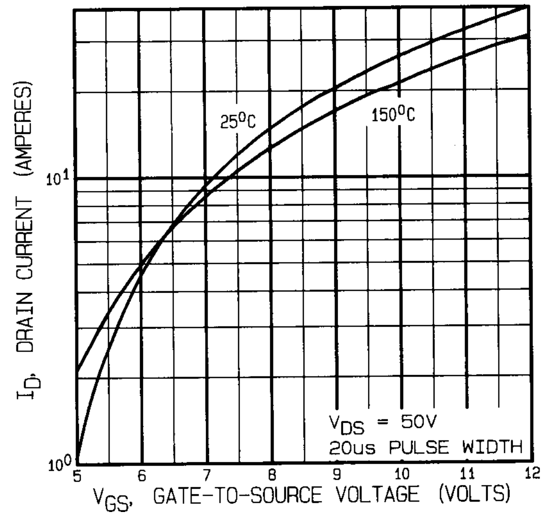


Fig 20. Typical Transfer Characteristics

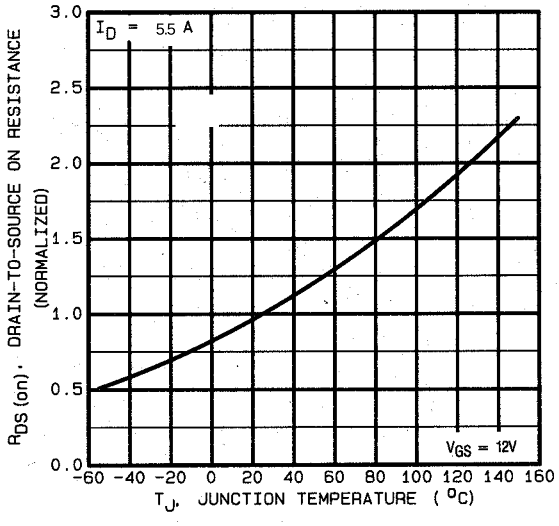


Fig 21. Normalized On-Resistance Vs. Temperature

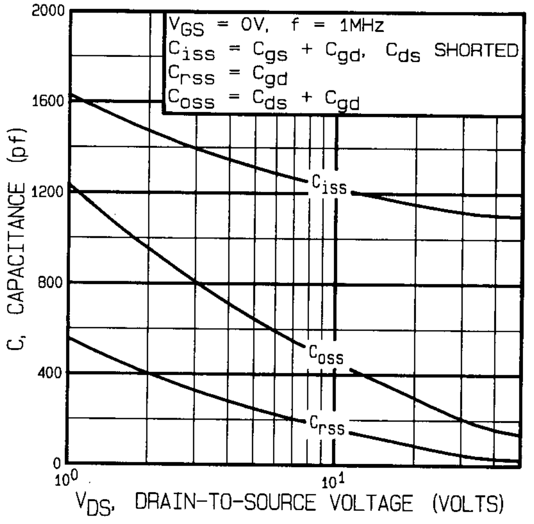


Fig 22. Typical Capacitance Vs. Drain-to-Source Voltage

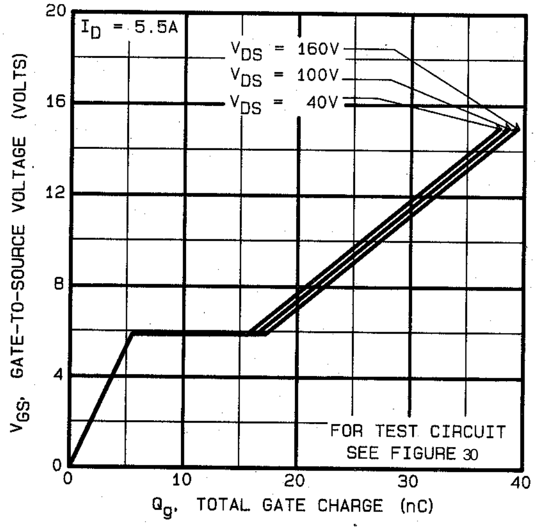


Fig 23. Typical Gate Charge Vs. Gate-to-Source Voltage

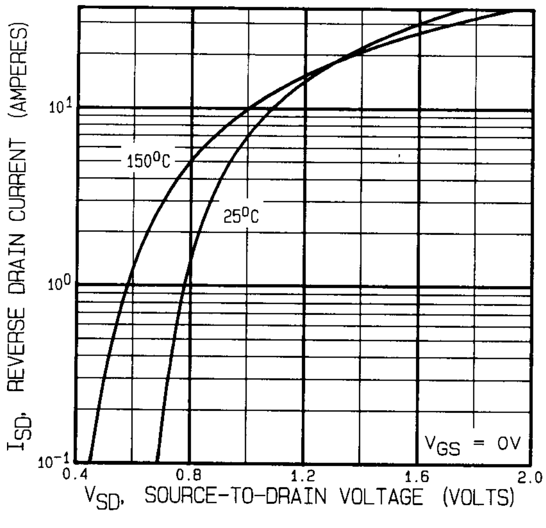


Fig 24. Typical Source-Drain Diode Forward Voltage

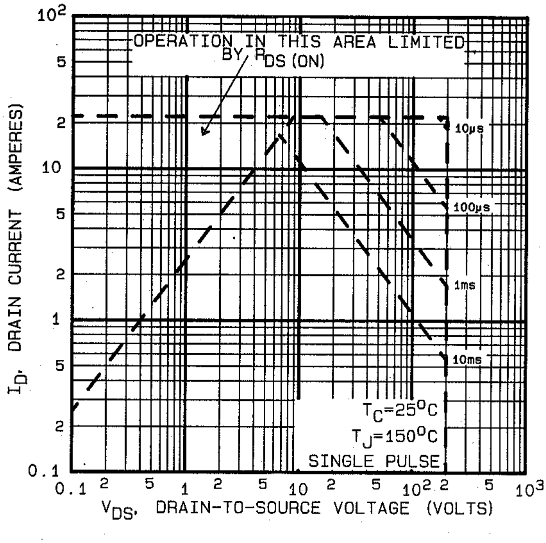


Fig 25. Maximum Safe Operating Area

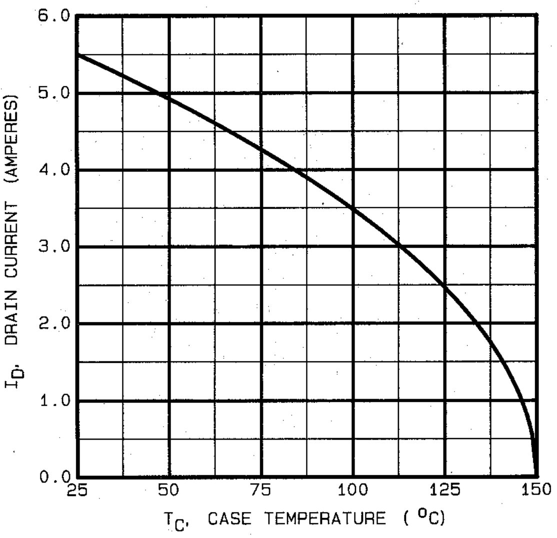


Fig 26. Maximum Drain Current Vs. Case Temperature

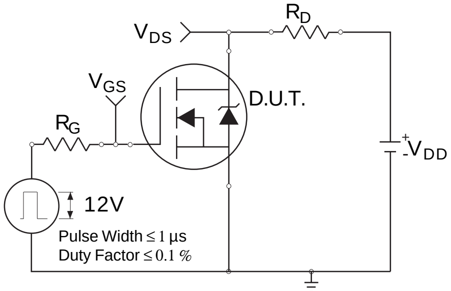


Fig 27a. Switching Time Test Circuit

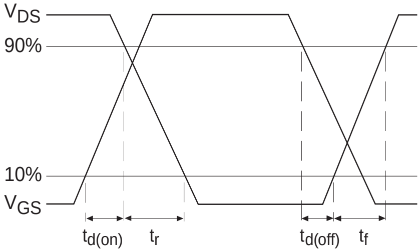


Fig 27b. Switching Time Waveforms

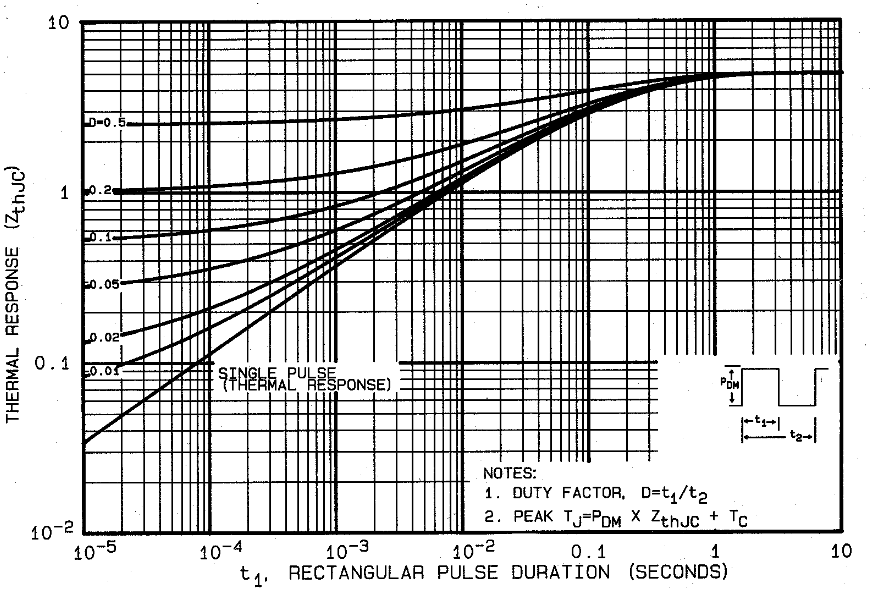


Fig 28. Maximum Effective Transient Thermal Impedance, Junction-to-Case

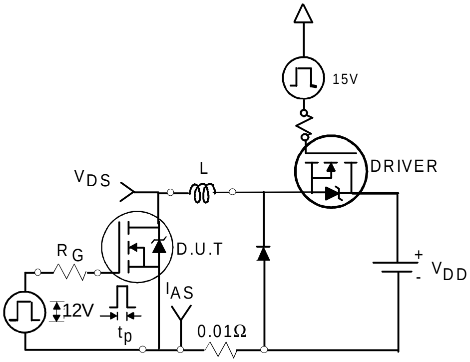


Fig 29a. Unclamped Inductive Test Circuit

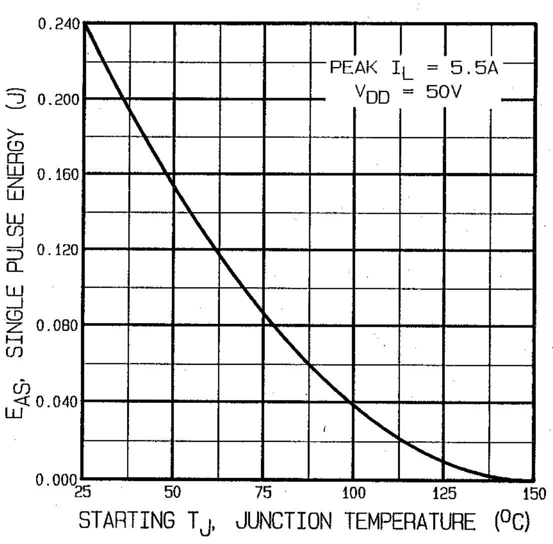


Fig 29c. Maximum Avalanche Energy Vs. Drain Current

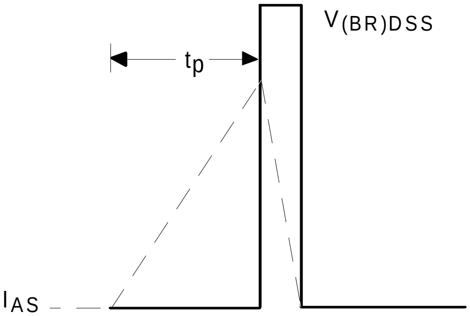


Fig 29b. Unclamped Inductive Waveforms

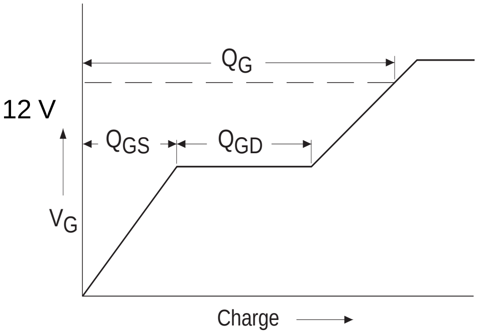


Fig30a. Basic Gate Charge Waveform

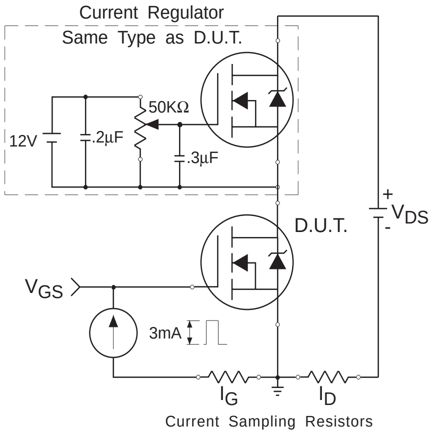


Fig 30b. Gate Charge Test Circuit

① See Figures 18 through 30 for pre-radiation curves

② Repetitive Rating; Pulse width limited by maximum junction temperature.
Refer to current HEXFET reliability report.

③ V_{DD} = 25V, Starting T_J = 25°C,
Peak I_L = 5.5A, L≥11mH, R_G=25Ω

④ $I_{SD} \leq$ 5.5A, di/dt ≤ 120A/µs,
$V_{DD} \leq BV_{DSS}$, $T_J \leq$ 150°C
Suggested RG =7.5Ω

⑤ Pulse width ≤ 300 µs; Duty Cycle ≤ 2%

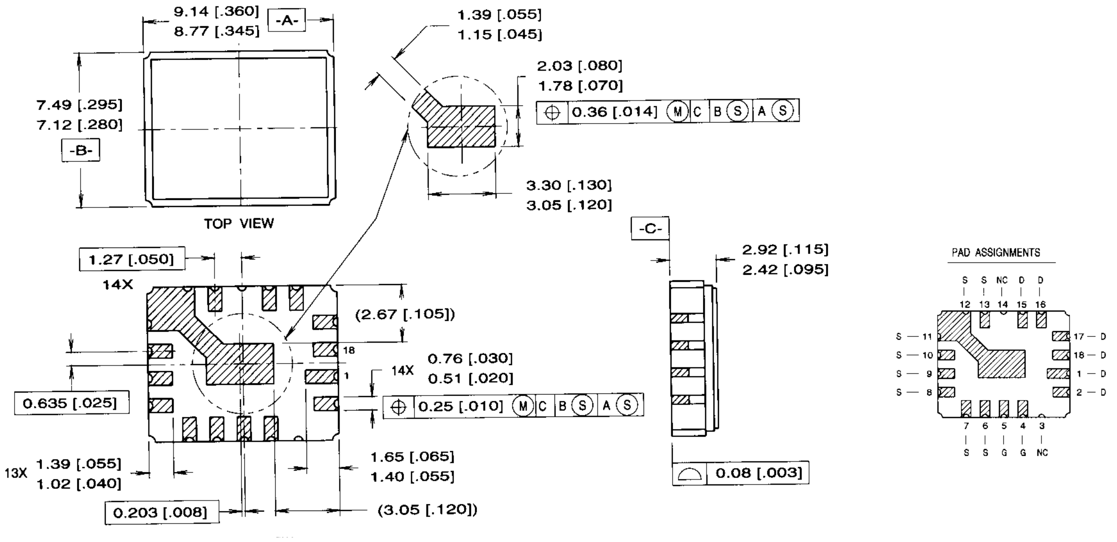
⑥ **Total Dose Irradiation with V_{GS} Bias.**
12 volt V_{GS} applied and V_{DS} = 0 during irradiation per MIL-STD-750, method 1019, codition A.

⑦ **Total Dose Irradiation with V_{DS} Bias.**
V_{DS} = 0.8 rated BV_{DSS} (pre-radiation) applied and V_{GS} = 0 during irradiation per MIL-STD-750, method 1019, condition A.

⑧ This test is performed using a flash x-ray source operated in the e-beam mode (energy ~2.5 MeV), 30 nsec pulse.

⑨ All Pre-Irradiation and Post-Irradiation test conditions are **identical** to facilitate direct comparison for circuit applications.

Case Outline and Dimensions — Leadless Chip Carrier (LCC) Package



G = GATE
D = DRAIN
S = SOURCE
NC = NO CONNECTION

NOTES:
1. DIMENSIONING & TOLERANCING PER ANSI Y14.5M-1982.
2. CONTROLLING DIMENSION: INCH.
3. DIMENSIONS ARE SHOWN IN MILLIMETERS [INCHES].

IR Case Style Leadless Chip Carrier (LCC)

International
IOR Rectifier

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