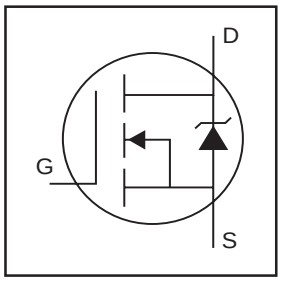
PD-91847A

International
IOR Rectifier

IRFSL11N50A

HEXFET® Power MOSFET

- Dynamic dv/dt Rating
- Repetitive Avalanche Rated
- Fast Switching
- Ease of Paraleling
- Simple Drive Requirements



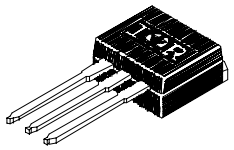
V_{DSS} = 500V

$R_{DS(on)}$ = 0.55Ω

I_D = 11A

Description

Third Generation HEXFETs from International Rectifier provide the designer with the best combination of fast switching, ruggedized device design, low on-resistance and cost-effectiveness.



TO-262

Absolute Maximum Ratings

	Parameter	Max.	Units
I_D @ T_C = 25°C	Continuous Drain Current, V_{GS} @ 10V	11	A
I_D @ T_C = 100°C	Continuous Drain Current, V_{GS} @ 10V	7.0	
I_{DM}	Pulsed Drain Current ①	44	
P_D @T_C = 25°C	Power Dissipation	190	W
	Linear Derating Factor	1.3	W/°C
V_{GS}	Gate-to-Source Voltage	± 30	V
E_{AS}	Single Pulse Avalanche Energy②	390	mJ
I_{AR}	Avalanche Current①	11	A
E_{AR}	Repetitive Avalanche Energy①	19	mJ
dv/dt	Peak Diode Recovery dv/dt ③	4.1	V/ns
T_J	Operating Junction and	-55 to + 175	°C
T_{STG}	Storage Temperature Range		
	Soldering Temperature, for 10 seconds	300 (1.6mm from case)	

Thermal Resistance

	Parameter	Typ.	Max.	Units
$R_{\theta JC}$	Junction-to-Case	——	0.75	°C
$R_{\theta JA}$	Junction-to-Ambient	——	40	

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Electrical Characteristics @ T_J = 25°C (unless otherwise specified)

	Parameter	Min.	Typ.	Max.	Units	Conditions
$V_{(BR)DSS}$	Drain-to-Source Breakdown Voltage	500	—	—	V	V_{GS} = 0V, I_D = 250µA
$\Delta V_{(BR)DSS}/\Delta T_J$	Breakdown Voltage Temp. Coefficient	—	0.57	—	V/°C	Reference to 25°C, I_D = 1mA
$R_{DS(on)}$	Static Drain-to-Source On-Resistance	—	—	0.55	Ω	V_{GS} = 10V, I_D = 6.6A ④
$V_{GS(th)}$	Gate Threshold Voltage	2.0	—	4.0	V	V_{DS} = V_{GS}, I_D = 250µA
g_{fs}	Forward Transconductance	6.0	—	—	S	V_{DS} = 50V, I_D = 6.6A
I_{DSS}	Drain-to-Source Leakage Current	—	—	25	µA	V_{DS} = 500V, V_{GS} = 0V
		—	—	250		V_{DS} = 400V, V_{GS} = 0V, T_J = 150°C
I_{GSS}	Gate-to-Source Forward Leakage	—	—	100	nA	V_{GS} = 30V
	Gate-to-Source Reverse Leakage	—	—	-100		V_{GS} = -30V
Q_g	Total Gate Charge	—	—	51	nC	I_D = 11A
Q_{gs}	Gate-to-Source Charge	—	—	12		V_{DS} = 400V
Q_{gd}	Gate-to-Drain ("Miller") Charge	—	—	23		V_{GS} = 10V, See Fig. 6 and 13 ④
$t_{d(on)}$	Turn-On Delay Time	—	14	—	ns	V_{DD} = 250V
t_r	Rise Time	—	34	—		I_D = 11A
$t_{d(off)}$	Turn-Off Delay Time	—	32	—		R_G = 9.1Ω
t_f	Fall Time	—	27	—		R_D = 22Ω,See Fig. 10 ④
L_D	Internal Drain Inductance	—	4.5	—	nH	Between lead, 6mm (0.25in.) from package and center of die contact
L_S	Internal Source Inductance	—	7.5	—		
C_{iss}	Input Capacitance	—	1426	—	pF	V_{GS} = 0V
C_{oss}	Output Capacitance	—	208	—		V_{DS} = 25V
C_{rss}	Reverse Transfer Capacitance	—	9.6	—		f = 1.0MHz, See Fig. 5
C_{oss}	Output Capacitance	—	1954	—		V_{GS} = 0V, V_{DS} = 1.0V, f = 1.0MHz
C_{oss}	Output Capacitance	—	53	—		V_{GS} = 0V, V_{DS} = 400V, f = 1.0MHz
C_{oss} eff.	Effective Output Capacitance ⑤	—	110	—		V_{GS} = 0V, V_{DS} = 0V to 400V

Source-Drain Ratings and Characteristics

	Parameter	Min.	Typ.	Max.	Units	Conditions
I_S	Continuous Source Current (Body Diode)	—	—	11	A	MOSFET symbol showing the integral reverse p-n junction diode.
I_{SM}	Pulsed Source Current (Body Diode) ①	—	—	44		
V_{SD}	Diode Forward Voltage	—	—	1.5	V	T_J = 25°C, I_S = 11A, V_{GS} = 0V ④
t_{rr}	Reverse Recovery Time	—	530	790	ns	T_J = 25°C, I_F = 11A
Q_{rr}	Reverse RecoveryCharge	—	3.4	5.1	µC	di/dt = 100A/µs ④
t_{on}	Forward Turn-On Time	Intrinsic turn-on time is negligible (turn-on is dominated by L_S+L_D)				

Notes:

① Repetitive rating; pulse width limited by max. junction temperature. (See fig. 11)

② Starting T_J = 25°C, L = 6.4mH R_G = 25Ω, I_{AS} = 11A. (See Figure 12)

③ I_{SD} ≤ 11A, di/dt ≤ 185A/µs, V_{DD} ≤ $V_{(BR)DSS}$, T_J ≤ 175°C

④ Pulse width ≤ 300µs; duty cycle ≤ 2%.

⑤ C_{oss} eff. is a fixed capacitance that gives the same charging time as C_{oss} while V_{DS} is rising from 0 to 80% V_{DSS}

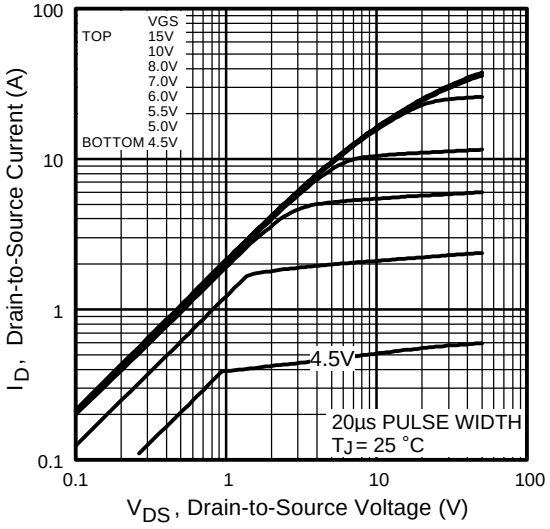


Fig 1. Typical Output Characteristics

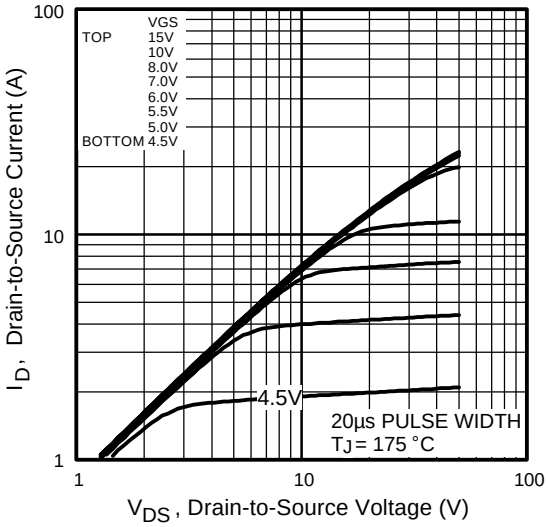


Fig 2. Typical Output Characteristics

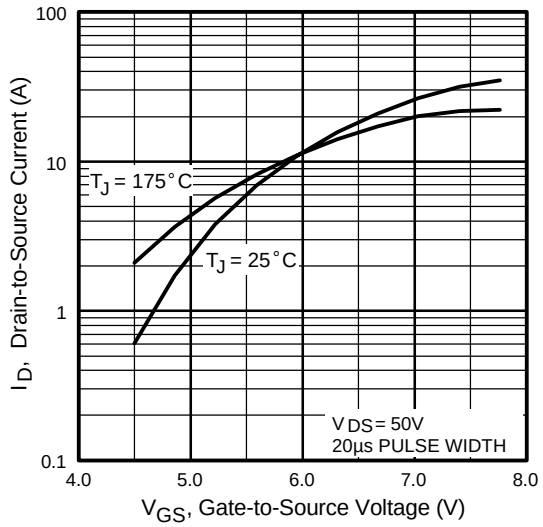


Fig 3. Typical Transfer Characteristics

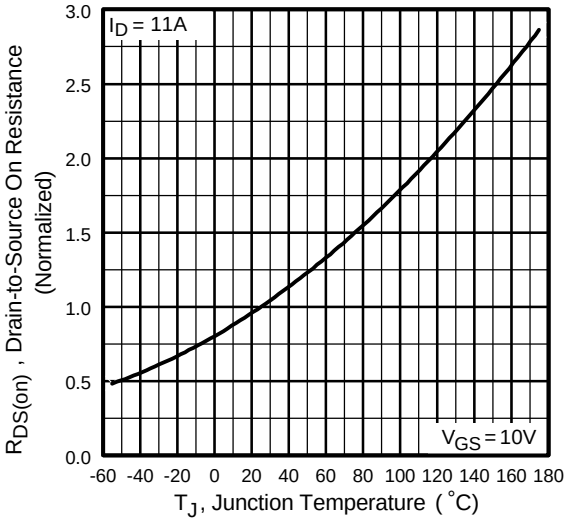


Fig 4. Normalized On-Resistance Vs. Temperature

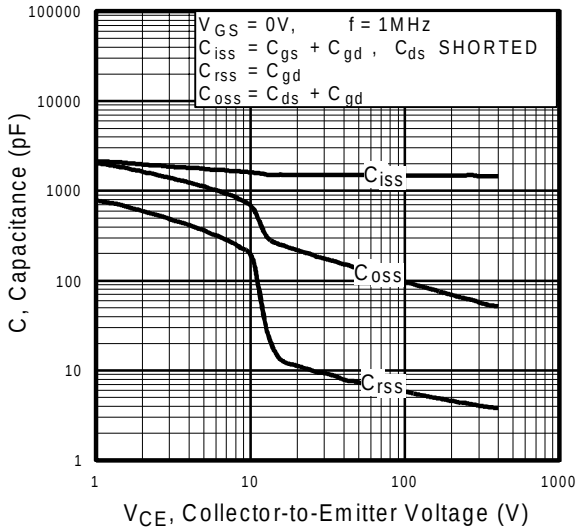


Fig 5. Typical Capacitance Vs. Drain-to-Source Voltage

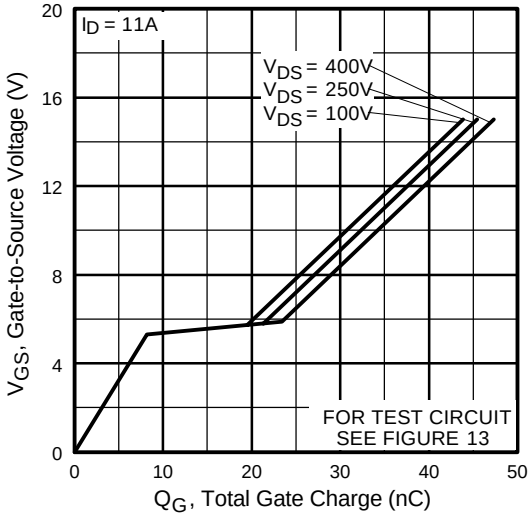


Fig 6. Typical Gate Charge Vs. Gate-to-Source Voltage

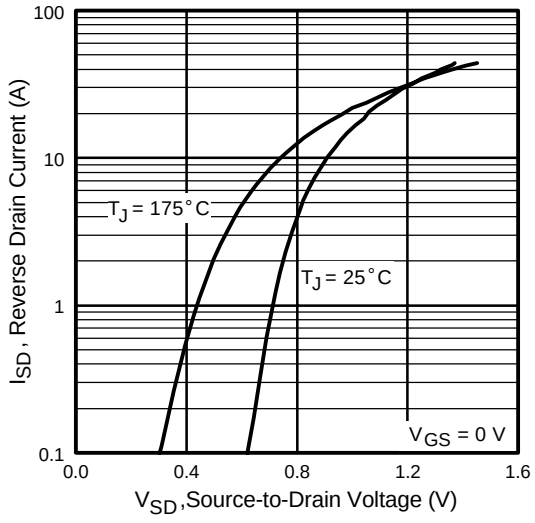


Fig 7. Typical Source-Drain Diode Forward Voltage

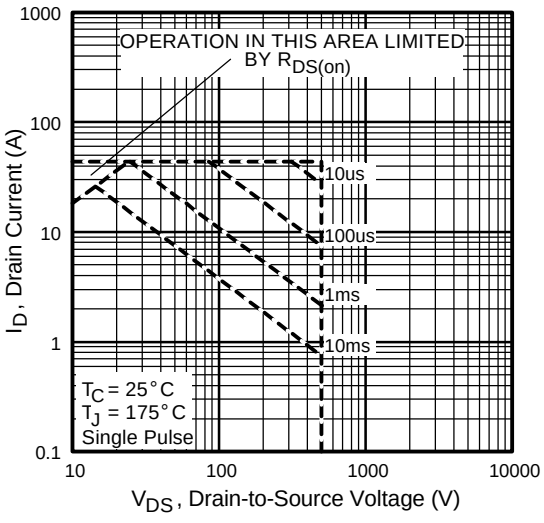


Fig 8. Maximum Safe Operating Area

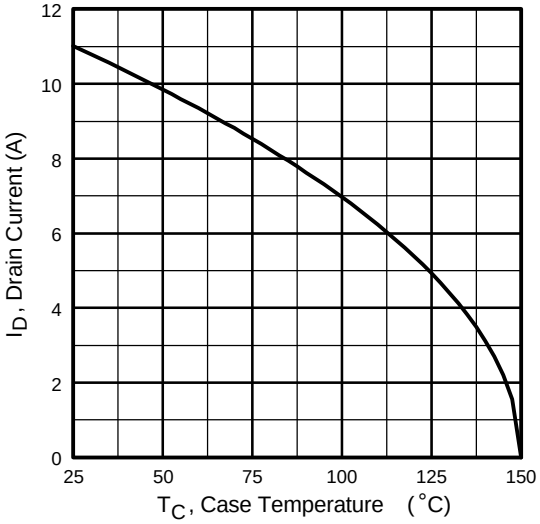


Fig 9. Maximum Drain Current Vs. Case Temperature

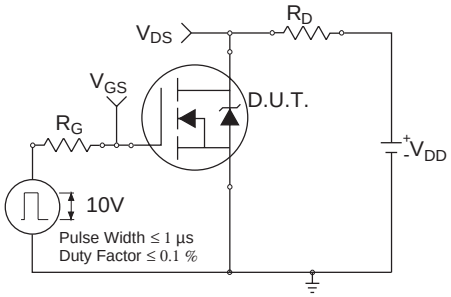


Fig 10a. Switching Time Test Circuit

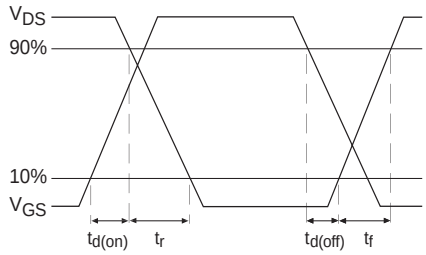


Fig 10b. Switching Time Waveforms

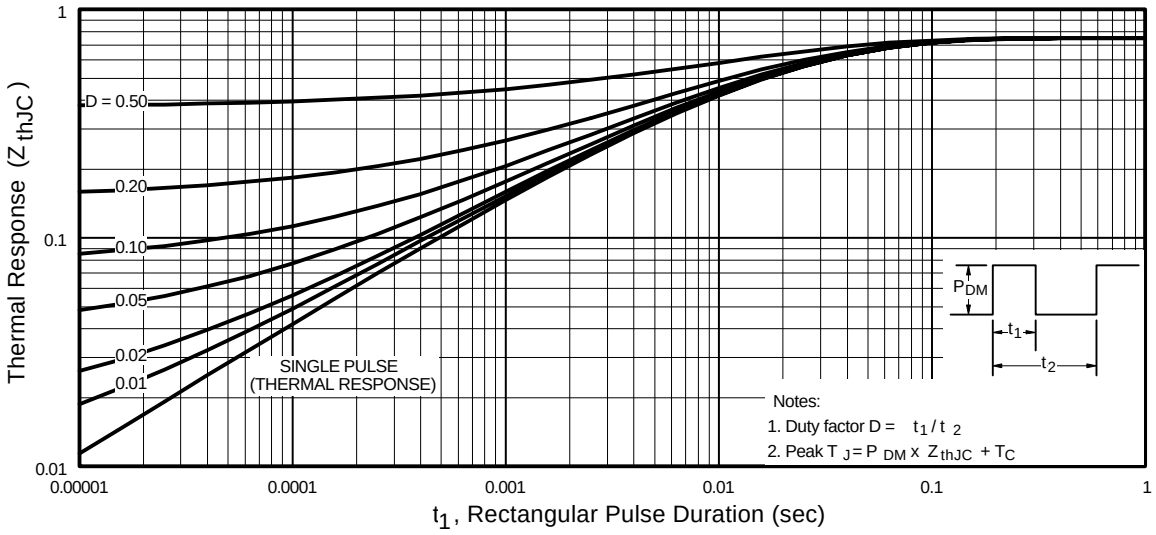


Fig 11. Maximum Effective Transient Thermal Impedance, Junction-to-Case

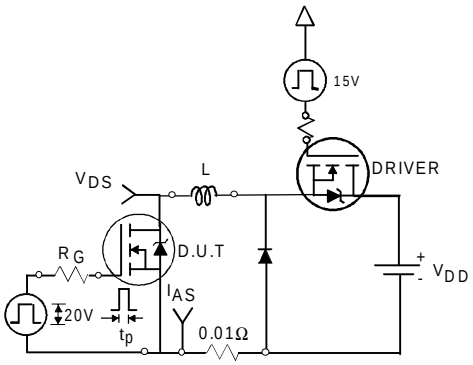


Fig 12a. Unclamped Inductive Test Circuit

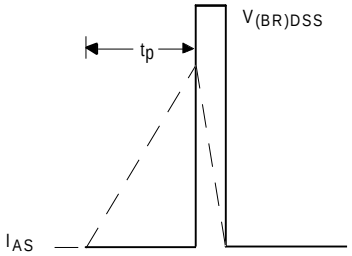


Fig 12b. Unclamped Inductive Waveforms

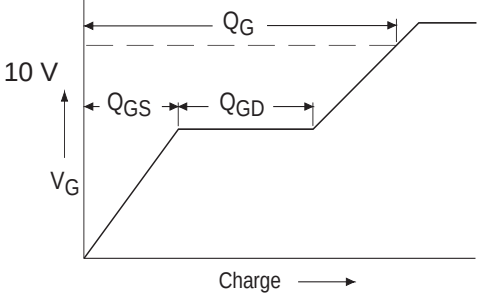


Fig 13a. Basic Gate Charge Waveform

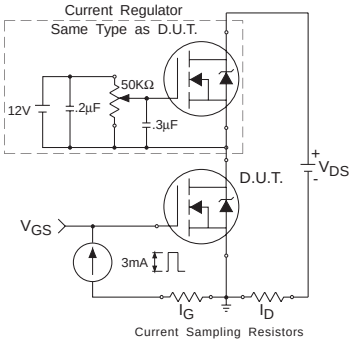


Fig 13b. Gate Charge Test Circuit

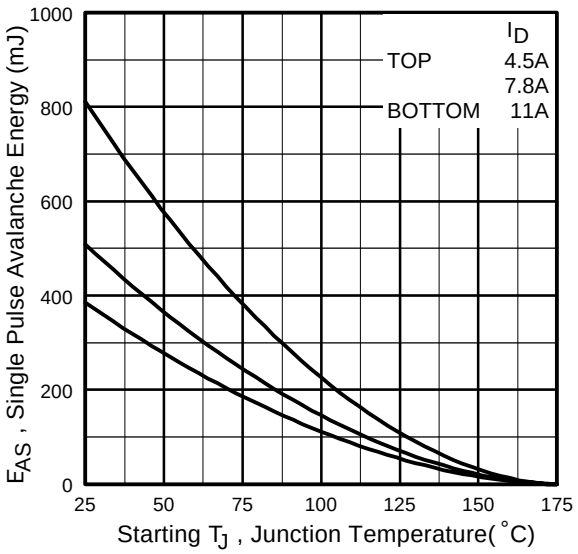


Fig 12c. Maximum Avalanche Energy Vs. Drain Current

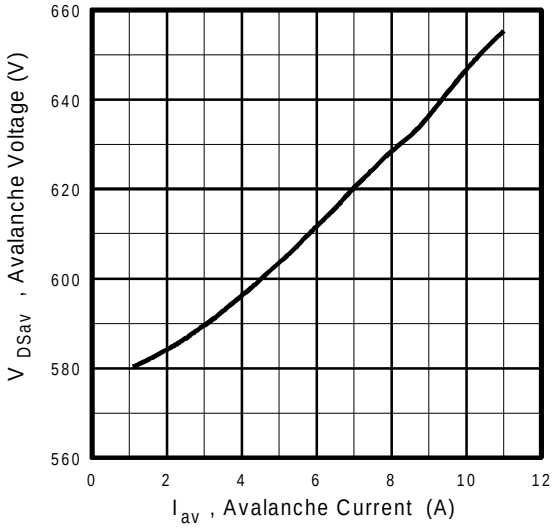
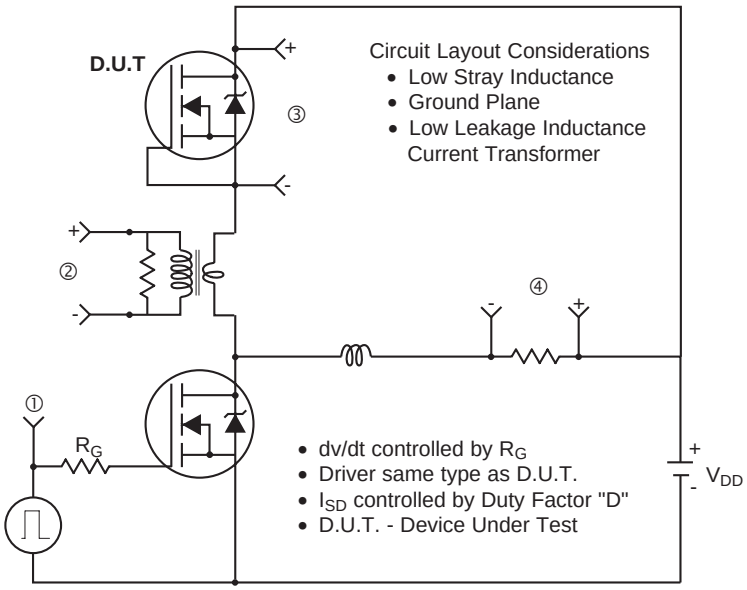
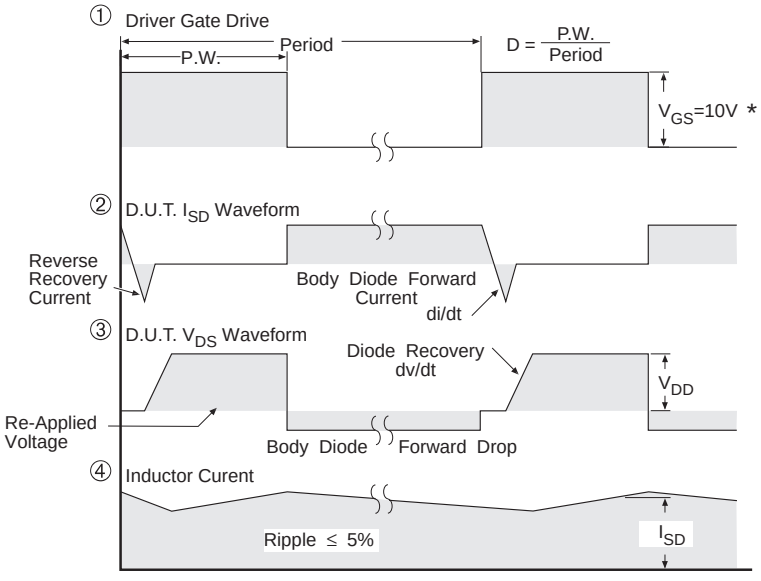


Fig 12d. Typical Drain-to-Source Voltage Vs. Avalanche Current

Peak Diode Recovery dv/dt Test Circuit



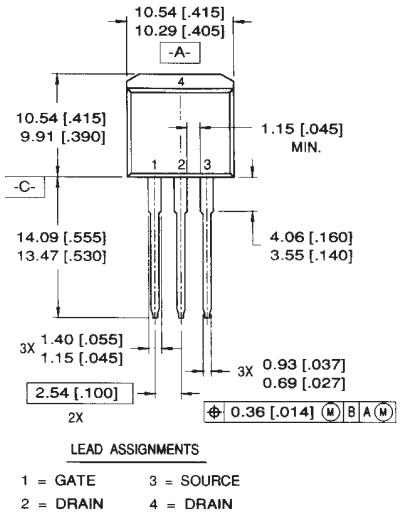


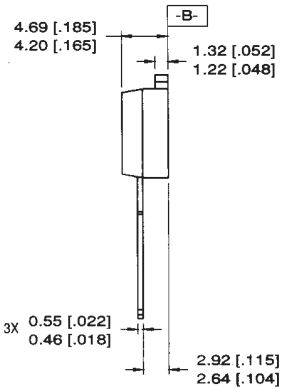
* V_{GS} = 5V for Logic Level Devices

Fig 14. For N-Channel HEXFETS

Package Outline

TO-262 Outline





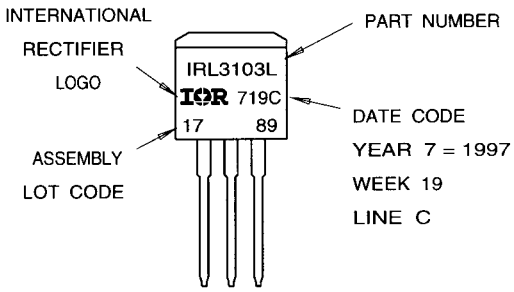
NOTES:

1. DIMENSIONING & TOLERANCING PER ANSI Y14.5M-1982
2. CONTROLLING DIMENSION: INCH.
3. DIMENSIONS ARE SHOWN IN MILLIMETERS [INCHES].
4. HEATSINK & LEAD DIMENSIONS DO NOT INCLUDE BURRS.

Part Marking Information

TO-262

EXAMPLE: THIS IS AN IRL3103L
LOT CODE 1789
ASSEMBLED ON WW 19, 1997
IN THE ASSEMBLY LINE "C"



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IR ITALY: Via Liguria 49, 10071 Borgaro, Torino Tel: ++ 39 11 451 0111
IR FAR EAST: K&H Bldg., 2F, 30-4 Nishi-Ikebukuro 3-Chome, Toshima-Ku, Tokyo Japan 171 Tel: 81 3 3983 0086
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