

INTERNATIONAL RECTIFIER



REPETITIVE AVALANCHE RATED AND dv/dt RATED

HEXFET[®] TRANSISTOR

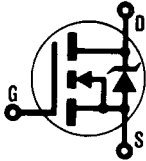
IRFM240

2N7219

JANTX2N7219

JANTXV2N7219

[REF: MIL-S-19500/596]



N-CHANNEL

200 Volt, 0.18 Ohm HEXFET

The HEXFET[®] technology is the key to International Rectifier's advanced line of power MOSFET transistors. The efficient geometry design achieves very low on-state resistance combined with high transconductance.

The HEXFET transistors also feature all of the well established advantages of MOSFETs such as voltage control, very fast switching, ease of paralleling and temperature stability of the electrical parameters.

They are well suited for applications such as switching power supplies and virtually any application where military and/or high reliability is required.

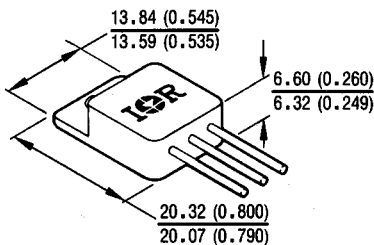
Product Summary

Part Number	BV_{DSS}	$R_{DS(on)}$	I_D
IRFM240	200V	0.18 Ω	18A

FEATURES:

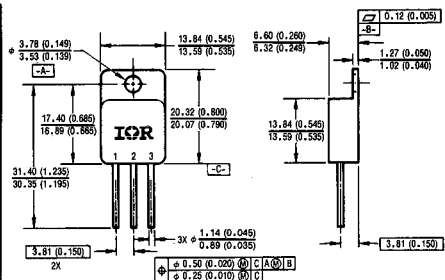
- Repetitive Avalanche Rating
- Isolated and Hermetically Sealed
- Alternative to TO-3 Package
- Simple Drive Requirements
- Ease of Paralleling
- Ceramic Eyelets

CASE STYLE AND DIMENSIONS



CAUTION

BERYLLIA WARNING PER MIL-S-19500
SEE PAGE I-316



LEGEND

- 1 DRAIN
- 2 SOURCE
- 3 GATE

NOTES:

- 1 DIMENSIONING & TOLERANCING PER ANSI Y14.5M - 1982.
- 2 ALL DIMENSIONS ARE SHOWN IN MILLIMETERS (INCHES).

Conforms to JEDEC Outline TO-254AA*
Dimensions in Millimeters and (Inches)

*For leadform configurations see page I-316, fig. 15

Absolute Maximum Ratings

Parameter	IRFM240, JANTXV, JANTX-, 2N7219	Units
I_D @ $V_{GS} = 10V$, $T_C = 25^\circ C$ Continuous Drain Current	18	A
I_D @ $V_{GS} = 10V$, $T_C = 100^\circ C$ Continuous Drain Current	11	
I_{DM} Pulsed Drain Current ①	72	
P_D @ $T_C = 25^\circ C$ Max. Power Dissipation	125	W
Linear Derating Factor	1.0	W/K ⑤
V_{GS} Gate-to-Source Voltage	± 20	V
E_{AS} Single Pulse Avalanche Energy ②	450 (See Fig. 12)	mJ
I_{AR} Avalanche Current ①	18 (See E _{AR})	A
E_{AR} Repetitive Avalanche Energy ①	12.5 (See Fig. 13)	mJ
dv/dt Peak Diode Recovery dv/dt ③	5.0 (See Fig. 13)	V/ns
T_J Operating Junction Temperature	-55 to 150	$^\circ C$
T_{STG} Storage Temperature Range		
Lead Temperature	300 (0.063 in. (1.6 mm) from case for 10s)	
Weight	9.3 (typical)	g

Electrical Characteristics @ $T_J = 25^\circ C$ (Unless Otherwise Specified)

Parameter	Min.	Typ.	Max.	Units	Test Conditions		
BV_{DSS} Drain-to-Source Breakdown Voltage	200	—	—	V	$V_{GS} = 0V$, $I_D = 1.0$ mA		
$\Delta BV_{DSS}/\Delta T_J$ Temperature Coefficient of Breakdown Voltage	—	0.29	—	V/°C	Reference to 25°C, $I_D = 1.0$ mA		
$R_{DS(on)}$ Static Drain-to-Source On-State Resistance	—	—	0.18	Ω	$V_{GS} = 10V$, $I_D = 11A$		
	—	—	0.25		$V_{GS} = 10V$, $I_D = 18A$ ④		
$V_{GS(th)}$ Gate Threshold Voltage	2.0	—	4.0	V	$V_{DS} = V_{GS}$, $I_D = 250$ μA		
g_{fs} Forward Transconductance	6.1	—	—	S (Ω)	$V_{DS} \geq 15V$, $I_{DS} = 11A$ ④		
I_{DSS} Zero Gate Voltage Drain Current	—	—	25	μA	$V_{DS} = 0.8 \times \text{Max. Rating}$, $V_{GS} = 0V$		
	—	—	250		$V_{DS} = 0.8 \times \text{Max. Rating}$, $V_{GS} = 0V$, $T_J = 125^\circ C$		
I_{GSS} Gate-to-Source Leakage Forward	—	—	100	nA	$V_{GS} = 20V$		
I_{GSS} Gate-to-Source Leakage Reverse	—	—	-100		$V_{GS} = -20V$		
Q_g Total Gate Charge	32	—	60	nC	$V_{GS} = 10V$, $I_D = 18A$		
Q_{gs} Gate-to-Source Charge	2.2	—	10.6		$V_{DS} = 0.5 \times \text{Max. Rating}$		
Q_{gd} Gate-to-Drain ("Miller") Charge	14.2	—	37.6		See Fig. 6 and 14		
$t_{d(on)}$ Turn-On Delay Time	—	—	20	ns	$V_{DD} = 100V$, $I_D = 11A$, $R_G = 9.1\Omega$		
t_r Rise Time	—	—	152		See Fig. 11		
$t_{d(off)}$ Turn-Off Delay Time	—	—	58				
t_f Fall Time	—	—	67				
L_D Internal Drain Inductance	—	8.7	—	nH	Measured from the drain lead, 6 mm (0.25 in.) from package to center of die.	Modified MOSFET symbol showing the internal inductances. 	
L_S Internal Source Inductance	—	8.7	—		Measured from the source lead, 6 mm (0.25 in.) from package to source bonding pad.		
C_{iss} Input Capacitance	—	1300	—	pF	$V_{GS} = 0V$, $V_{DS} = 25V$		
C_{oss} Output Capacitance	—	400	—		$f = 1.0$ MHz		
C_{rss} Reverse Transfer Capacitance	—	130	—		See Fig. 5		
C_{DC} Drain-to-Case Capacitance	—	12	—				



Source-Drain Diode Ratings and Characteristics

Parameter	Min.	Typ.	Max.	Units	Test Conditions
I_S Continuous Source Current (Body Diode)	—	—	18	A	Modified MOSFET symbol showing the integral Reverse p-n junction rectifier. 
I_{SM} Pulsed Source Current (Body Diode) ①	—	—	72		
V_{SD} Diode Forward Voltage	—	—	1.5	V	$T_J = 25^\circ\text{C}$, $I_S = 18\text{A}$, $V_{GS} = 0\text{V}$ ②
t_{rr} Reverse Recovery Time	—	—	500	nS	$T_J = 25^\circ\text{C}$, $I_F = 18\text{A}$, $dI/dt \leq 100\text{ A}/\mu\text{s}$ ③
Q_{RR} Reverse Recovery Charge	—	—	5.3	μC	$V_{DD} \leq 50\text{V}$
t_{on} Forward Turn-On Time	Intrinsic turn-on time is negligible. Turn-on speed is substantially controlled by $L_S + L_D$.				

Thermal Resistance

Parameter	Min.	Typ.	Max.	Units	Test Conditions
R_{thJC} Junction-to-Case	—	—	1.0	K/W ⑤	
R_{thJS} Case-to-Sink	—	0.21	—		Mounting surface flat, smooth, and greased
R_{thJA} Junction-to-Ambient	—	—	48		Typical socket mount

① Repetitive Rating: Pulse width limited by maximum junction temperature (see figure 9)
Refer to current HEXFET reliability report

② @ $V_{DD} = 50\text{V}$, Starting $T_J = 25^\circ\text{C}$,
 $L \geq 2.1\text{ mH}$, $R_G = 25\Omega$,
Peak $I_L = 18\text{A}$

③ $I_{SD} \leq 18\text{A}$, $dI/dt \leq 150\text{ A}/\mu\text{s}$,
 $V_{DD} \leq BVDSS$, $T_J \leq 150^\circ\text{C}$
Suggested $R_G = 9.1\Omega$

④ Pulse width $\leq 300\mu\text{s}$; Duty Cycle $\leq 2\%$

⑤ $K/W = ^\circ\text{C}/W$
 $W/K = W/^\circ\text{C}$

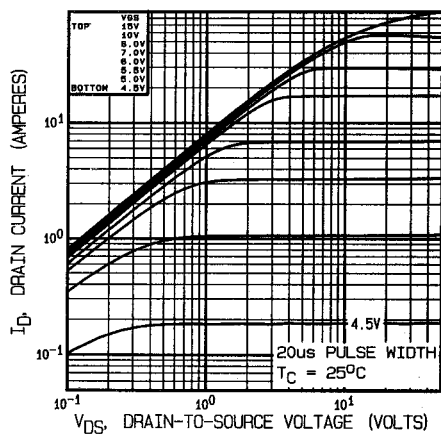
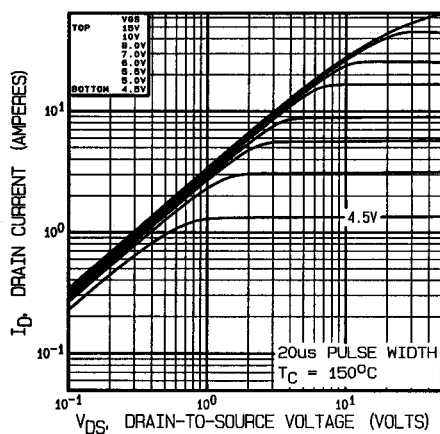
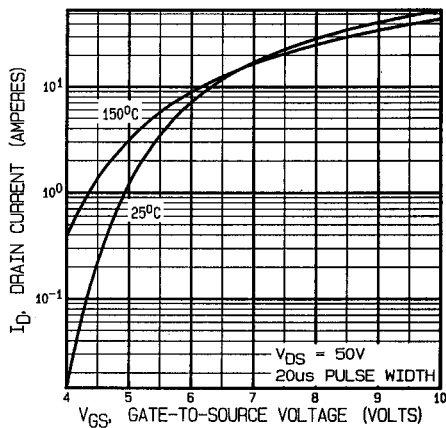
Fig. 1 — Typical Output Characteristics, $T_C = 25^\circ\text{C}$ Fig. 2 — Typical Output Characteristics, $T_C = 150^\circ\text{C}$ 

Fig. 3 — Typical Transfer Characteristics

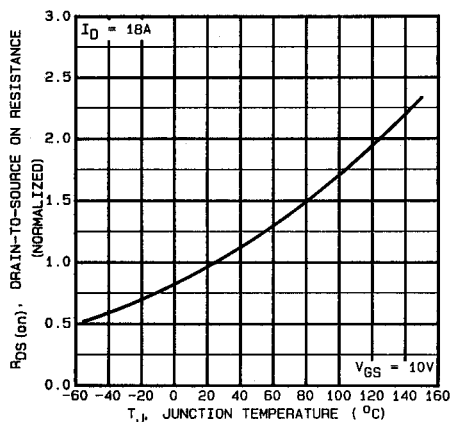
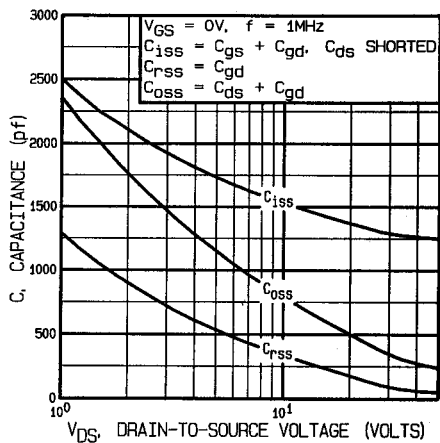
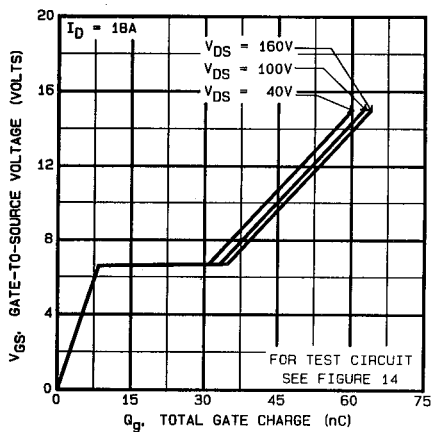
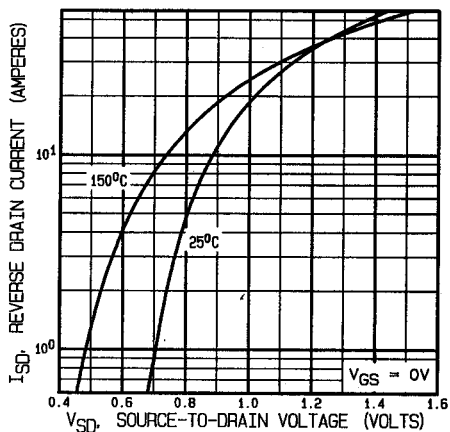
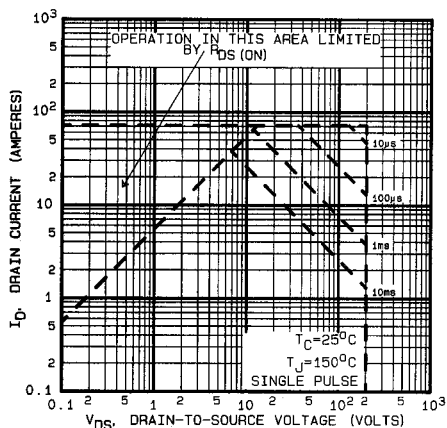


Fig. 4 — Normalized On-Resistance Vs. Temperature


Fig. 5 — Typical Capacitance Vs. Drain-to-Source Voltage

Fig. 6 — Typical Gate Charge Vs. Gate-to-Source Voltage

Fig. 7 — Typical Source-Drain Diode Forward Voltage

Fig. 8 — Maximum Safe Operating Area

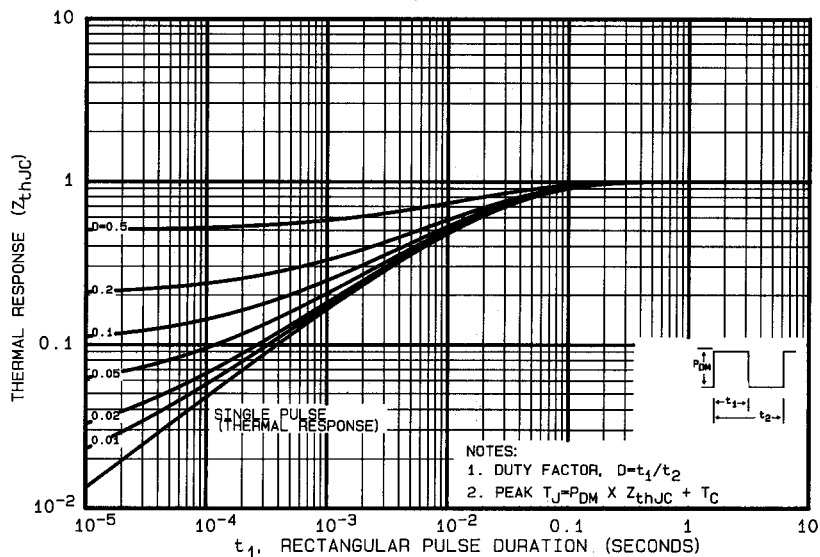


Fig. 9 — Maximum Effective Transient Thermal Impedance, Junction-to-Case Vs. Pulse Duration

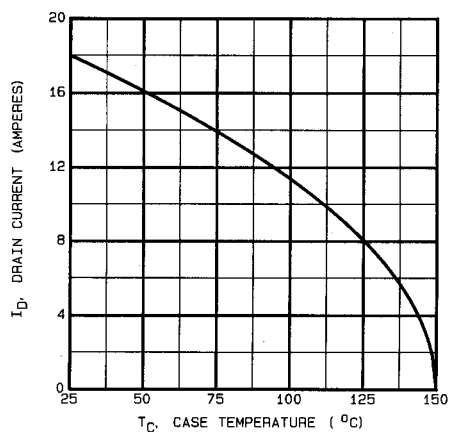


Fig. 10 — Maximum Drain Current Vs. Case Temperature

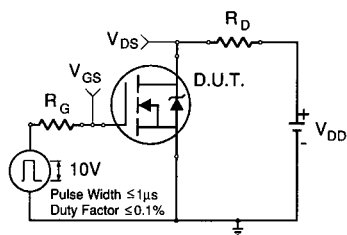


Fig. 11a — Switching Time Test Circuit

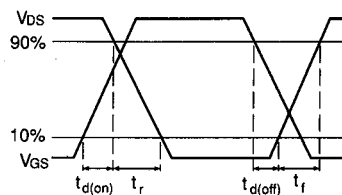
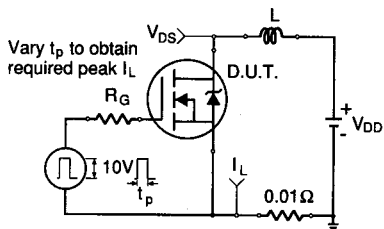
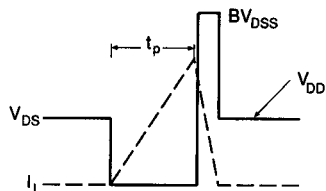
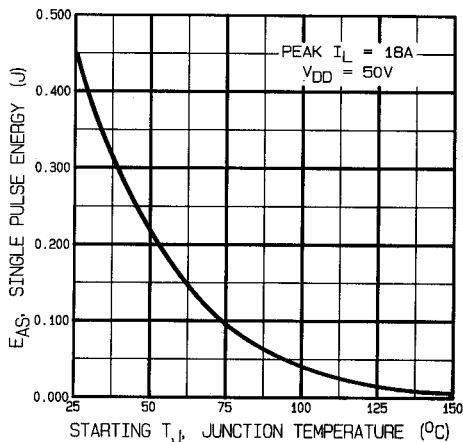
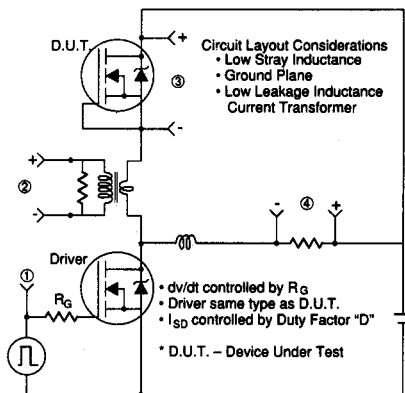
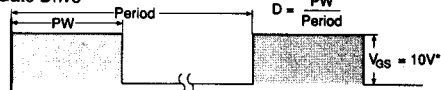
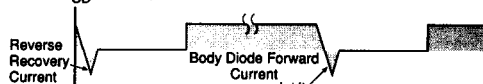
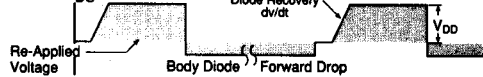


Fig. 11b — Switching Time Waveforms


Fig. 12a — Unclamped Inductive Test Circuit

Fig. 12b — Unclamped Inductive Waveforms

Fig. 12c — Maximum Avalanche Energy Vs. Starting Junction Temperature

① Driver Gate Drive

② D.U.T. I_{SD} Waveform

③ D.U.T. V_{DS} Waveform

④ Inductor Current


* $V_{GS} = 5V$ for Logic Level Devices

Fig. 13 — Peak Diode Recovery dv/dt Test Circuit

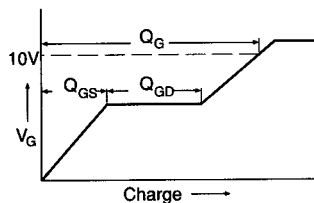


Fig. 14a — Basic Gate Charge Waveform

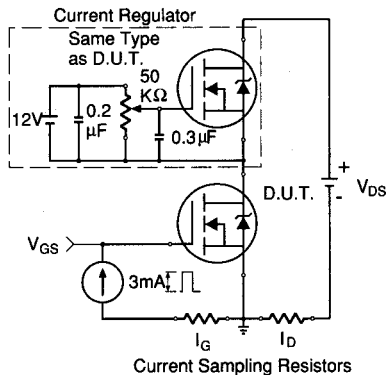


Fig. 14b — Gate Charge Test Circuit

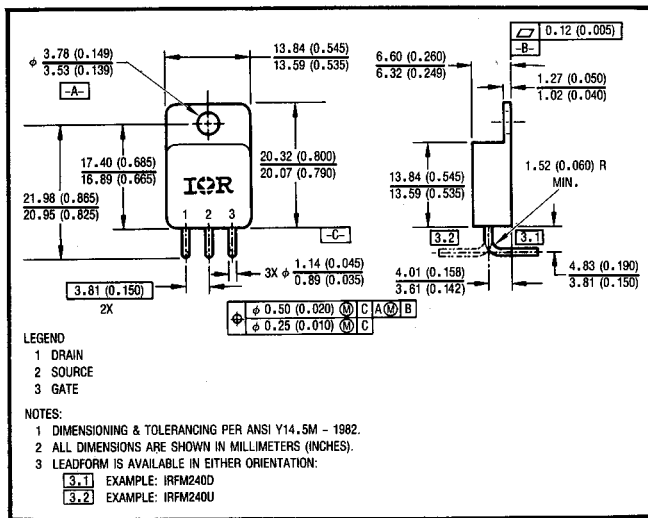


Fig. 15 – Optional Leadforms for Outline TO-254

BERYLLIA WARNING PER MIL-S-19500

Packages containing beryllia shall not be ground, sandblasted, machined, or have other operations performed on them which will produce beryllia or beryllium dust. Furthermore, beryllium oxide packages shall not be placed in acids that will produce fumes containing beryllium.