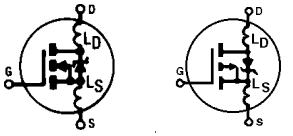
International
IOR Rectifier

Preliminary Data Sheet No. PD - 9.1664

HEXFET® TRANSISTORS

IRFG5210

COMBINATION
N AND P CHANNEL
(2 EACH)



200 Volt, 1.60Ω (N and P channel) HEXFET

The HEXFET technology is the key to International Rectifier's advanced line of power MOSFET transistors. The efficient geometry and unique processing of this latest "State of the Art" design achieves: very low on-state resistance combined with high transconductance; superior reverse energy and diode recovery dv/dt capability.

Ideal for AC applications, the P and N-Channel dice are physical complements such that their opposite polarity offers circuit simplification as well as all the other well established advantages of MOSFETs.

They are well-suited for both military and commercial applications such as switching power supplies, motor controls, inverters, choppers, audio amplifiers and high energy pulse circuits.

Product Summary

Part Number	BV_{DSS}	$R_{DS(on)}$		I_D	
		N	P	N	P
IRFG5210	200V	1.60Ω	1.60Ω	0.68A	-0.68A

Features:

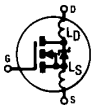
- Avalanche Energy Rating
- Dynamic dv/dt Rating
- Hermetically Sealed
- Lightweight
- For Automatic Insertion
- Matched RDS(on) Ratings
- Simple Drive Requirements
- Ease of Paralleling
- 2 N-Channel / 2 P-Channel Co-Packaged HEXFET's

Absolute Maximum Ratings

	Parameter	N-Channel	P-Channel	Units
I_D @ V_{GS} = 10V, T_C = 25°C	Continuous Drain Current	0.68	-0.68	A
I_D @ V_{GS} = 10V, T_C = 100°C	Continuous Drain Current	0.40	-0.40	
I_{DM}	Pulsed Drain Current ①	2.72①	-2.72⑤	
V_{GS}	Gate-to-Source Voltage	± 20		V
E_{AS}	Single Pulse Avalanche Energy	64②	110⑥	mJ
dv/dt	Peak Diode Recovery dv/dt	20 ③	-27⑦	V/ns
T_J	Operating Junction	-55 to 150		°C
T_{STG}	Storage Temperature Range			
	Lead Temperature	300 (0.063 in. (1.6mm) from case for 10s)		
	Weight	1.3 (typical)		g

IRFG5210 Device

Electrical Characteristics For Each N-Channel Chip @ Tj = 25°C (Unless Otherwise Specified)

	Parameter	Min	Typ	Max	Units	Test Conditions
BV_{DSS}	Drain-to-Source Breakdown Voltage	200	—	—	V	V_{GS} =0 V, I_D = 1.0mA
$\Delta BV_{DSS}/\Delta T_J$	Temperature Coefficient of Breakdown Voltage	—	0.27	—	V/°C	Reference to 25°C, I_D = 1.0mA
$R_{DS(on)}$	Static Drain-to-Source	—	—	1.6	Ω	V_{GS} = 10V, I_D = 0.40A④
	On-State Resistance	—	—	1.83		V_{GS} = 10V, I_D = 0.68 A,T_J =125°C
$V_{GS(th)}$	Gate Threshold Voltage	2.0	—	4.0	V	V_{DS} = V_{GS}, I_D = 0.25mA
g_{fs}	Forward Transconductance	0.54	—	—	S (℧)	V_{DS} ≥ 15V, I_{DS} = 0.40A ④
I_{DSS}	Zero Gate Voltage Drain Current	—	—	25	μA	V_{DS}= 0.8 x Max Rating,V_{GS}=0V
		—	—	250		V_{DS} = 0.8 x Max Rating V_{GS} = 0V, T_J = 125°C
I_{GSS}	Gate-to-Source Leakage Forward	—	—	100	nA	V_{GS} = 20V
I_{GSS}	Gate-to-Source Leakage Reverse	—	—	-100		V_{GS} = -20V
Q_g	Total Gate Charge	—	—	9.5	nC	V_{GS} = 10V, I_D =0.68A V_{DS} = Max Rating x 0.5
Q_{gs}	Gate-to-Source Charge	—	—	1.4		
Q_{gd}	Gate-to-Drain ('Miller') Charge	—	—	4.3		
$t_{d(on)}$	Turn-On Delay Time	—	—	8.7	ns	V_{DD} =100V, I_D = 0.68A, R_G = 7.5Ω
t_r	Rise Time	—	—	2.4		
$t_{d(off)}$	Turn-Off Delay Time	—	—	19		
t_f	Fall Time	—	—	24		
L_D	Internal Drain Inductance	—	4.0	—	nH	Measured from drain lead, 6mm (0.25 in) from package to center of die. Modified MOSFET symbol showing the internal inductances.
L_S	Internal Source Inductance	—	6.0	—		Measured from source lead, 6mm (0.25 in) from package to source bonding pad. 
C_{iss}	Input Capacitance	—	140	—	pF	V_{GS} = 0V, V_{DS} = 25V f = 1.0MHz
C_{oss}	Output Capacitance	—	56	—		
C_{rss}	Reverse Transfer Capacitance	—	14	—		

Source-Drain Diode Ratings and Characteristics For Each N-Channel Chip

	Parameter	Min	Typ	Max	Units	Test Conditions
I_S	Continuous Source Current (Body Diode)	—	—	0.63	A	Modified MOSFET symbol showing the integral reverse p-n junction rectifier. 
I_{SM}	Pulse Source Current (Body Diode) ①	—	—	2.5		
V_{SD}	Diode Forward Voltage	—	—	1.5	V	T_j = 25°C, I_S = 0.68A, V_{GS} = 0V ④
t_{rr}	Reverse Recovery Time	—	—	110	ns	T_j = 25°C, I_F = 0.68A, di/dt ≤ 100A/μs
Q_{RR}	Reverse Recovery Charge	—	—	310	nC	V_{DD} ≤ 50V ④
t_{on}	Forward Turn-On Time	Intrinsic turn-on time is negligible. Turn-on speed is substantially controlled by L_S + L_D.				

① Repetitive Rating; Pulse width limited by maximum junction temperature.
Refer to current HEXFET reliability report.

② Starting T_J = 25°C, V_{DD} = 50V
E_{AS} = [0.5 * L * (I_L^2)]
Peak I_L = 0.68, 25 ≤ R_G ≤ 200Ω

③ I_{SD} ≤ 0.68A, di/dt ≤ 290A/μs,
V_{DD} ≤ BV_{DSS}, T_J ≤ 150°C
Suggested RG = 2.35Ω

④ Pulse width ≤ 300 μs; Duty Cycle ≤ 2%

⑤ Repetitive Rating; Pulse width limited by maximum junction temperature.
Refer to current HEXFET reliability report.

⑥ V_{DD} = -50V, Starting T_J = 25°C,
E_{AS} = [0.5 * L * (I_L^2)]
Peak I_L = -0.68, 25 ≤ R_G ≤ 200Ω

⑦ I_{SD} ≤ -0.68, di/dt ≤ -290A/μs,
V_{DD} ≤ BV_{DSS}, T_J ≤ 150°C

IRFG5210 Device

Electrical Characteristics For Each P-Channel Chip @ Tj = 25°C (Unless Otherwise Specified)

	Parameter	Min	Typ	Max	Units	Test Conditions
BV_{DSS}	Drain-to-Source Breakdown Voltage	-200	—	—	V	V_{GS} =0 V, I_D = -1.0mA
$\Delta BV_{DSS}/\Delta T_J$	Temperature Coefficient of Breakdown Voltage	—	-0.22	—	V/°C	Reference to 25°C, I_D = -1.0mA
$R_{DS(on)}$	Static Drain-to-Source On-State Resistance	—	—	1.6	Ω	V_{GS} = -10V, I_D = -0.40A④
		—	—	1.83		V_{GS} = -10V, I_D = -0.68A,T_J =125°C
$V_{GS(th)}$	Gate Threshold Voltage	-2.0	—	-4.0	V	V_{DS} = V_{GS}, I_D = -0.25mA
g_{fs}	Forward Transconductance	0.64	—	—	S (℧)	V_{DS} ≥ -15V, I_{DS} = -0.40A ④
I_{DSS}	Zero Gate Voltage Drain Current	—	—	-25	μA	V_{DS}= 0.8 x Max Rating,V_{GS}=0V
		—	—	-250		V_{DS} = 0.8 x Max Rating V_{GS} = 0V, T_J = 125°C
I_{GSS}	Gate-to-Source Leakage Forward	—	—	-100	nA	V_{GS} = -20V
I_{GSS}	Gate-to-Source Leakage Reverse	—	—	100		V_{GS} = 20V
Q_g	Total Gate Charge	—	—	18	nC	V_{GS} = -10V, I_D = -0.68A V_{DS} = Max Rating x 0.5
Q_{gs}	Gate-to-Source Charge	—	—	2.8		
Q_{gd}	Gate-to-Drain ('Miller') Charge	—	—	8.4		
$t_{d(on)}$	Turn-On Delay Time	—	—	15	ns	V_{DD} = -100V, I_D = -0.68A, R_G = 7.5Ω
t_r	Rise Time	—	—	11		
$t_{d(off)}$	Turn-Off Delay Time	—	—	36		
t_f	Fall Time	—	—	43		
L_D	Internal Drain Inductance	—	4.0	—	nH	Measured from drain lead, 6mm (0.25 in) from package to center of die. Modified MOSFET symbol showing the internal inductances.
L_S	Internal Source Inductance	—	6.0	—		Measured from source lead, 6mm (0.25 in) from package to source bonding pad.
C_{iss}	Input Capacitance	—	320	—	pF	V_{GS} = 0V, V_{DS} = -25V f = 1.0MHz
C_{oss}	Output Capacitance	—	110	—		
C_{rss}	Reverse Transfer Capacitance	—	20	—		

Source-Drain Diode Ratings and Characteristics For Each P-Channel Chip

	Parameter	Min	Typ	Max	Units	Test Conditions
I_S	Continuous Source Current (Body Diode)	—	—	-0.61	A	Modified MOSFET symbol showing the integral reverse p-n junction rectifier.
I_{SM}	Pulse Source Current (Body Diode) ①	—	—	-2.4		
V_{SD}	Diode Forward Voltage	—	—	-4.8	V	T_j = 25°C, I_S = -0.68A, V_{GS} = 0V ④
t_{rr}	Reverse Recovery Time	—	—	120	ns	T_j = 25°C, I_F = -0.68A, di/dt ≤ -100A/μs V_{DD} ≤ -50V ④
Q_{RR}	Reverse Recovery Charge	—	—	420	nC	
t_{on}	Forward Turn-On Time	Intrinsic turn-on time is negligible. Turn-on speed is substantially controlled by L_S + L_D.				

① Repetitive Rating; Pulse width limited by maximum junction temperature. Refer to current HEXFET reliability report.

② V_{DD} = 50V, Starting T_J = 25°C, E_{AS} = [0.5 ∗ L ∗ (I_L^2)] Peak I_L = 0.68A, , 25 ≤ R_G ≤ 200Ω

③ I_{SD} ≤ 0.68A, di/dt ≤ 290A/μs, V_{DD} ≤ BV_{DSS}, T_J ≤150°C Suggested R_G = 2.35Ω

④ Pulse width ≤ 300 μs; Duty Cycle ≤ 2%

⑤ Repetitive Rating; Pulse width limited by maximum junction temperature. Refer to current HEXFET reliability report.

⑥ V_{DD} = -50V, Starting T_J = 25°C, E_{AS} = [0.5 ∗ L ∗ (I_L^2)] Peak I_L = -0.68A, , 25 ≤ R_G ≤ 200Ω

⑦ I_{SD} ≤ -0.68A, di/dt ≤ -290A/μs, V_{DD} ≤ BV_{DSS}, T_J ≤ 150°C Suggested R_G = 2.35Ω

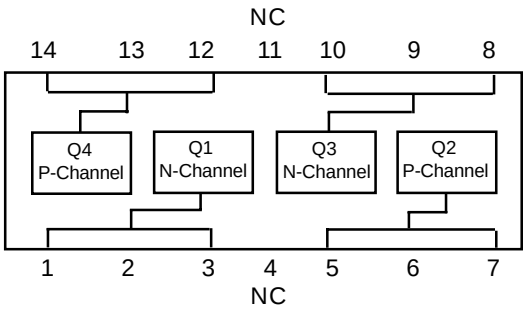
Power Ratings

	Power Ratings Test	Single FET	All Four FEts with Equal Power	Units
P_D @ T_A = 25°C	Max. Power Dissipation	14	2.5	W
	Linear Derating Factor	0.011	0.020	W/K
RthJC	Thermal Resistance Junction-to-case	17	—	K/W
RthJA	Thermal Resistance Junction-to-Ambient	90	50	K/W
K1, K2	Thermal Cooling Factors	45	40	%

The temperature rise of each device within the package is the result of the power dissipated by the device itself and the power dissipated by the other devices. The power dissipated by the adjacent devices does not have the same effect as the power dissipated within the junction itself. The temperature rise for any particular unit (e.g. (1)) within the package can be calculated with the following expression:

$$(1) \qquad T1 = 90\ (P1 + K12\ P2)$$

where the Kij are the thermal coupling coefficients shown in the Power Ratings Table.



N-Channel
Q1, Q3

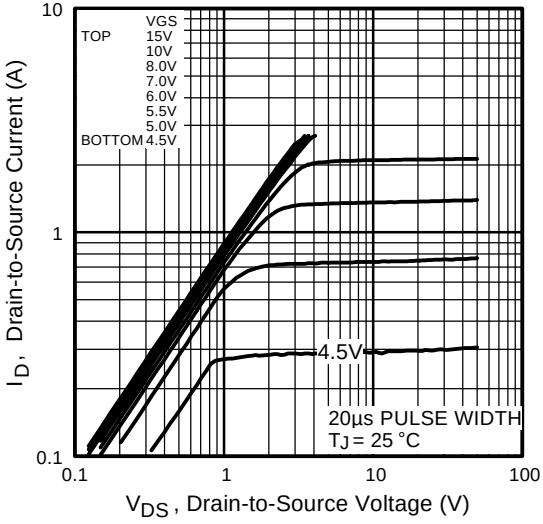


Fig 1. Typical Output Characteristics

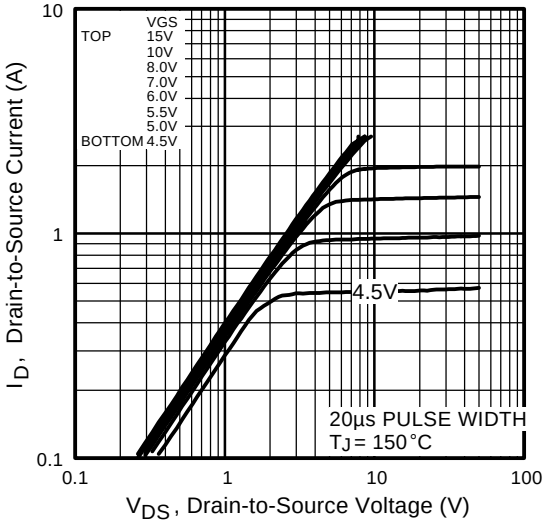


Fig 2. Typical Output Characteristics

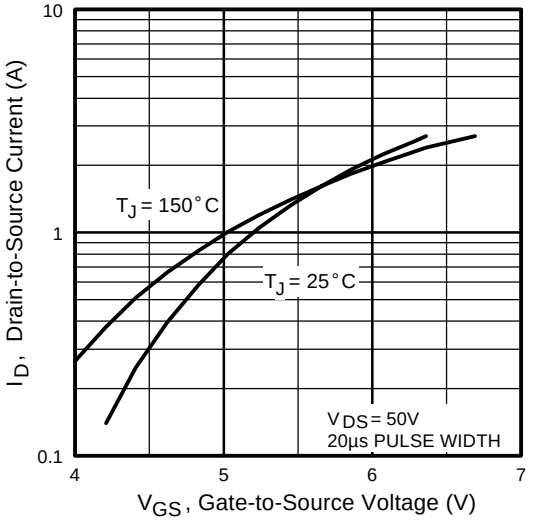


Fig 3. Typical Transfer Characteristics

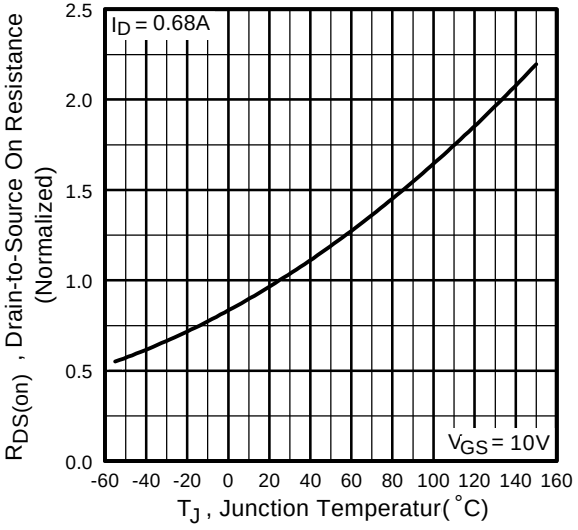


Fig 4. Normalized On-Resistance Vs. Temperature

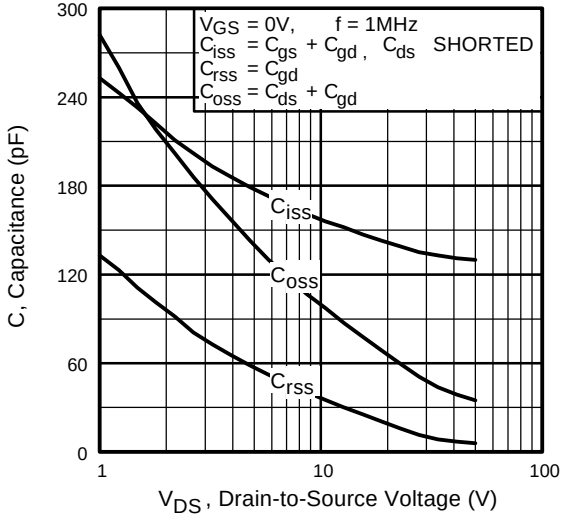


Fig 5. Typical Capacitance Vs. Drain-to-Source Voltage

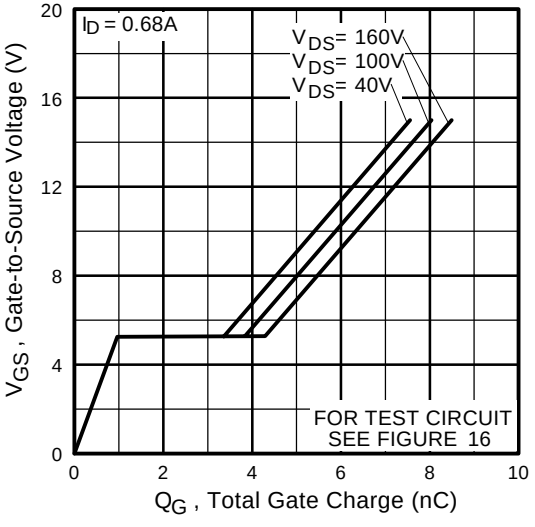


Fig 6. Typical Gate Charge Vs. Gate-to-Source Voltage

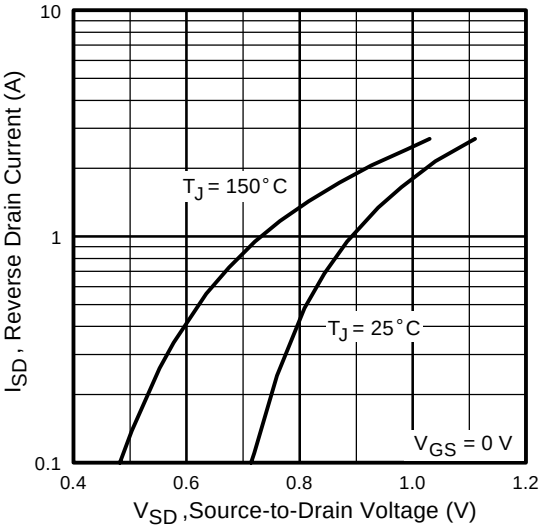


Fig 7. Typical Source-Drain Diode Forward Voltage

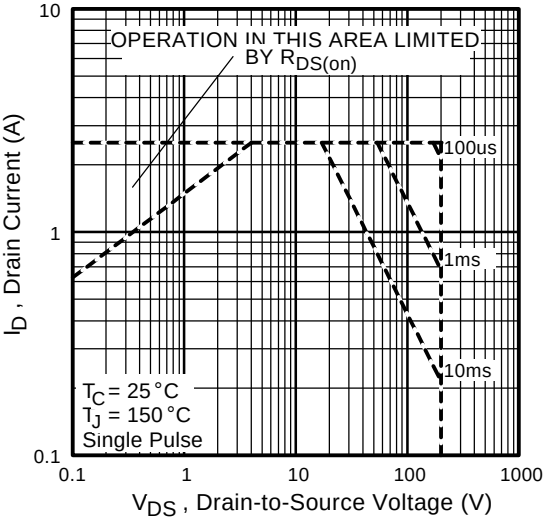


Fig 8. Maximum Safe Operating Area

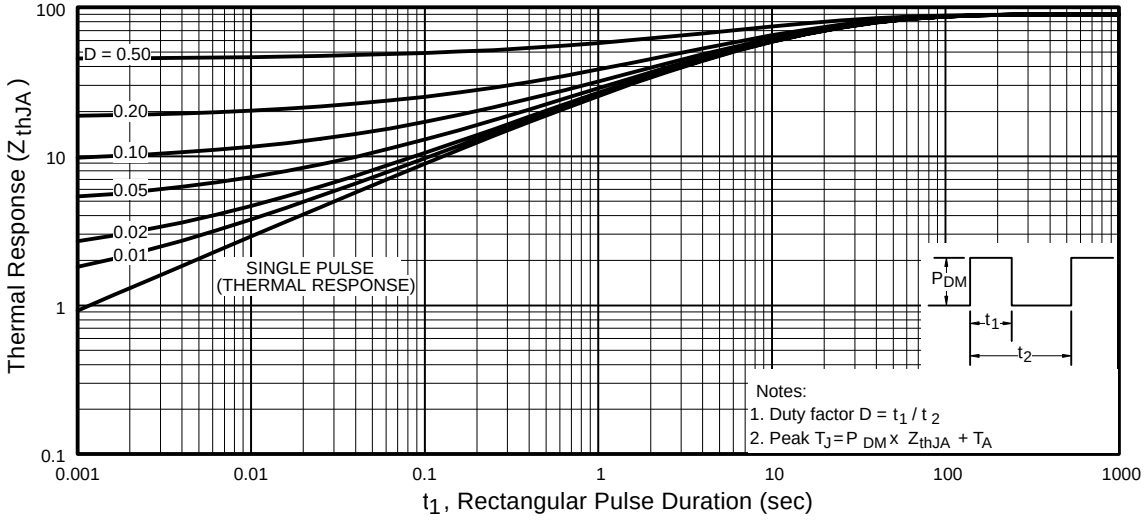


Fig 11. Maximum Effective Transient Thermal Impedance, Junction-to-Case

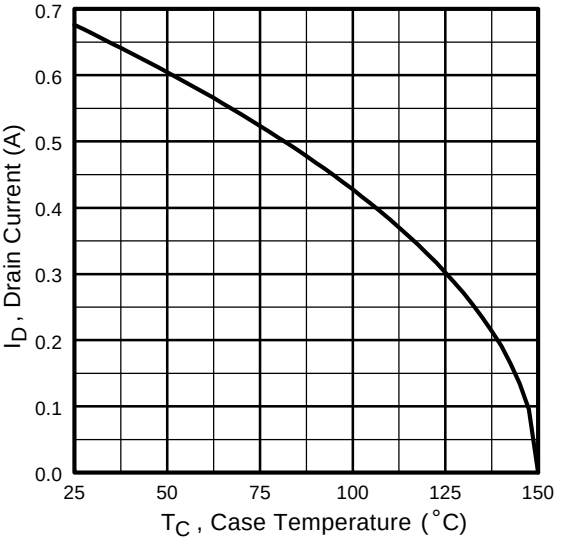


Fig 12. Maximum Drain Current vs. Case Temperature

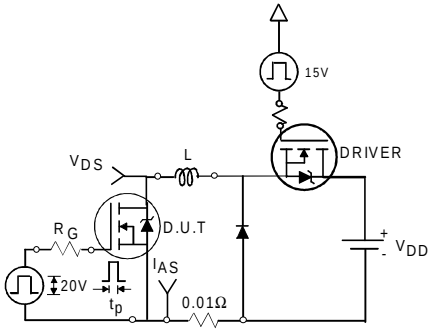


Fig 14a. Unclamped Inductive Test Circuit

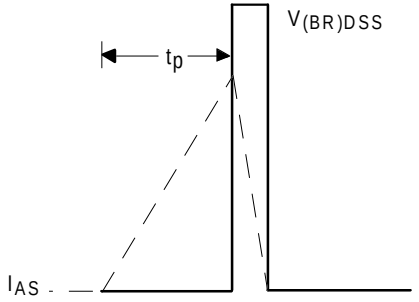


Fig 14b. Unclamped Inductive Waveforms

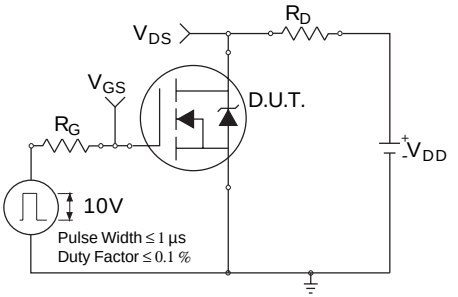


Fig 13a. Switching Time Test Circuit

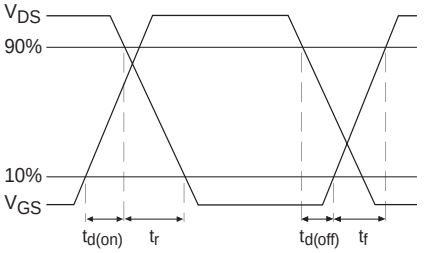


Fig 13b. Switching Time Waveforms

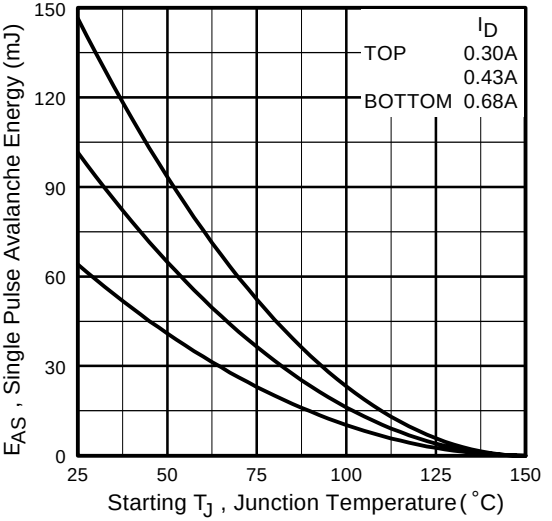
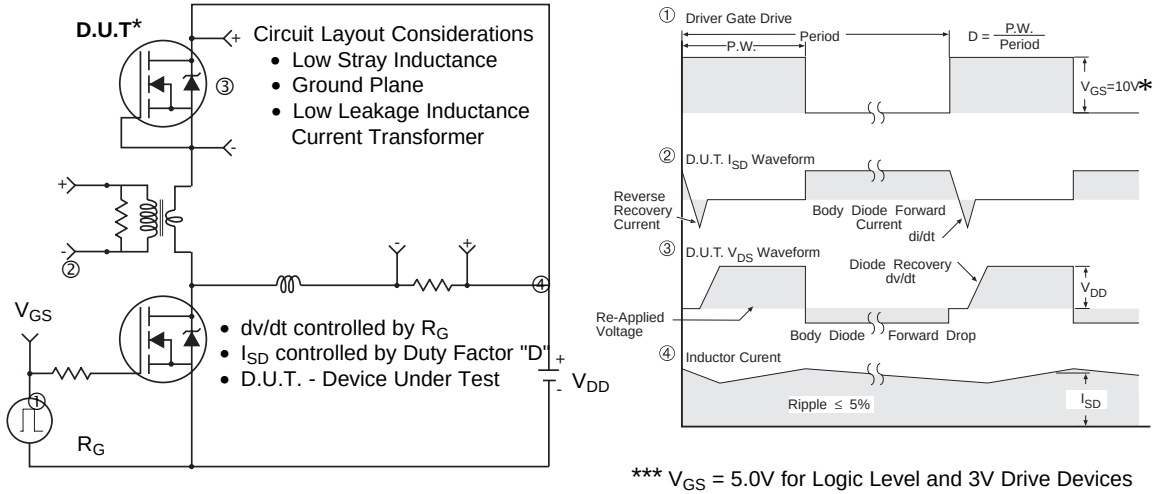


Fig 14c. Maximum Avalanche Energy Vs. Drain Current



*** V_{GS} = 5.0V for Logic Level and 3V Drive Devices

Fig. 15 - Peak Diode Recovery dv/dt Test Circuit

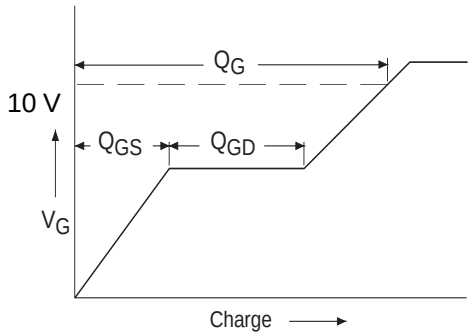


Fig 16a. Basic Gate Charge Waveform

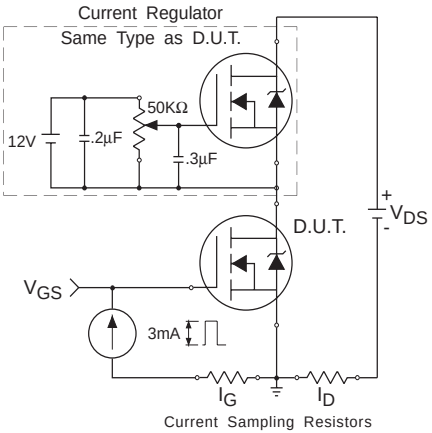


Fig 16b. Gate Charge Test Circuit

P-Channel
Q2, Q4

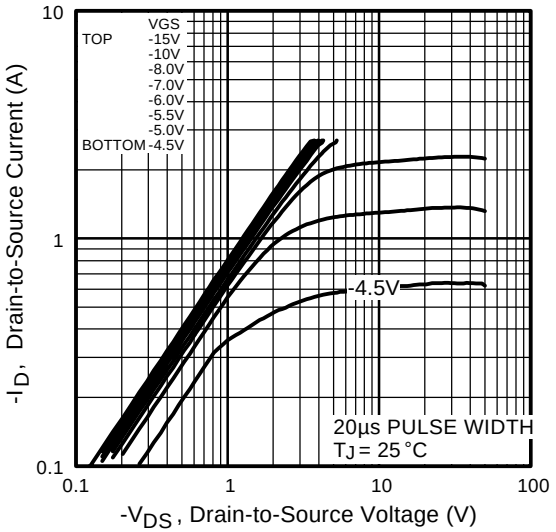


Fig 17. Typical Output Characteristics

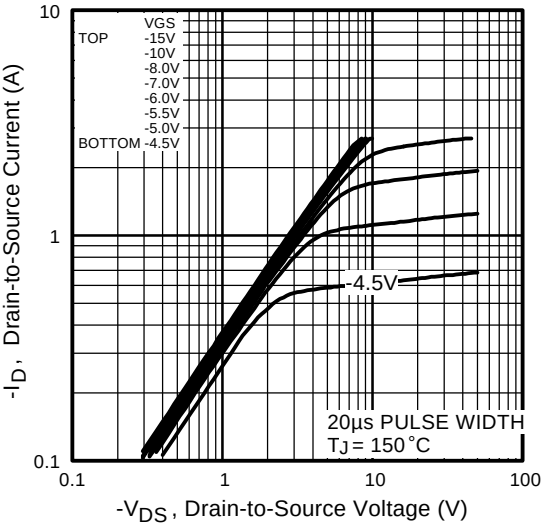


Fig 18. Typical Output Characteristics

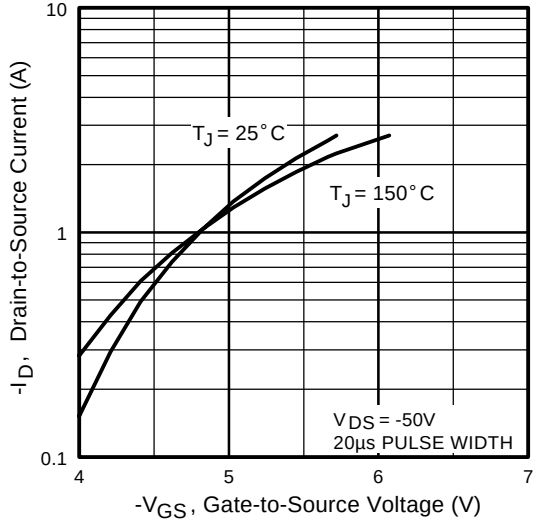


Fig 19. Typical Transfer Characteristics

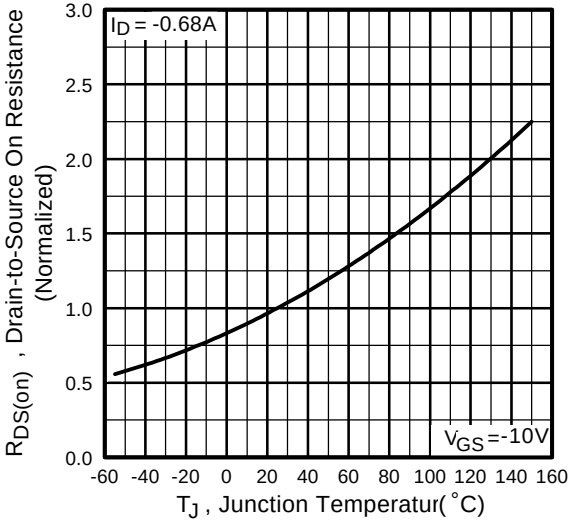


Fig 20. Normalized On-Resistance Vs. Temperature

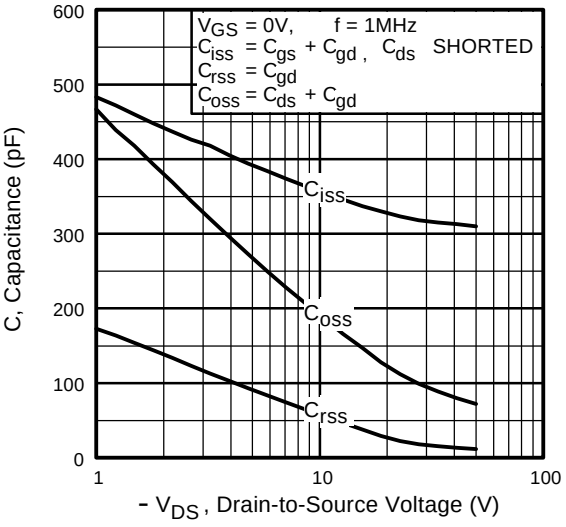


Fig 21. Typical Capacitance Vs. Drain-to-Source Voltage

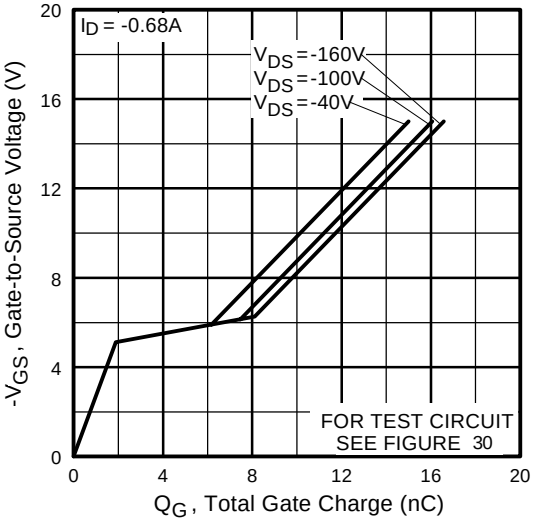


Fig22. Typical Gate Charge Vs. Gate-to-Source Voltage

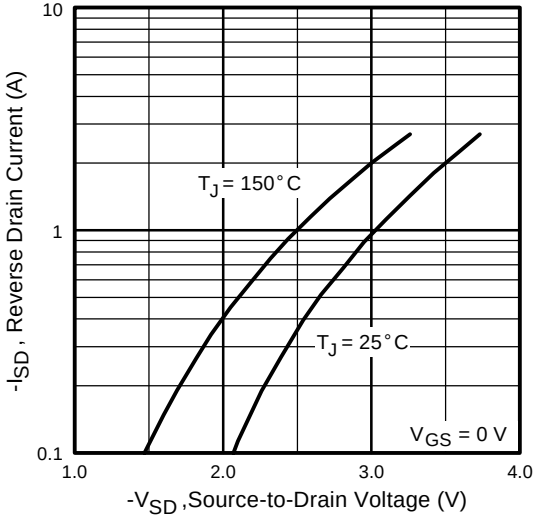


Fig23. Typical Source-Drain Diode Forward Voltage

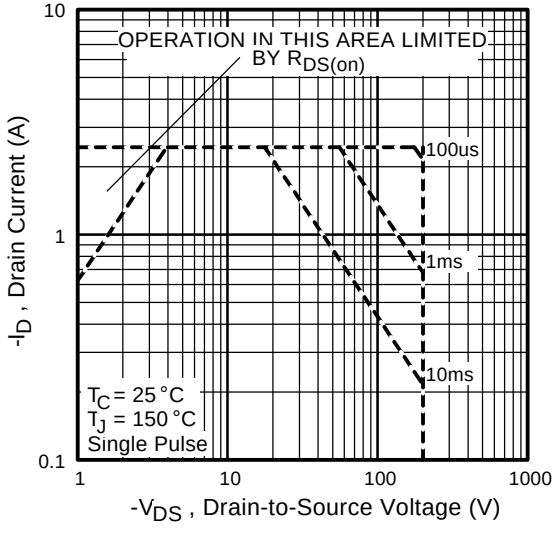


Fig 24. Maximum Safe Operating Area

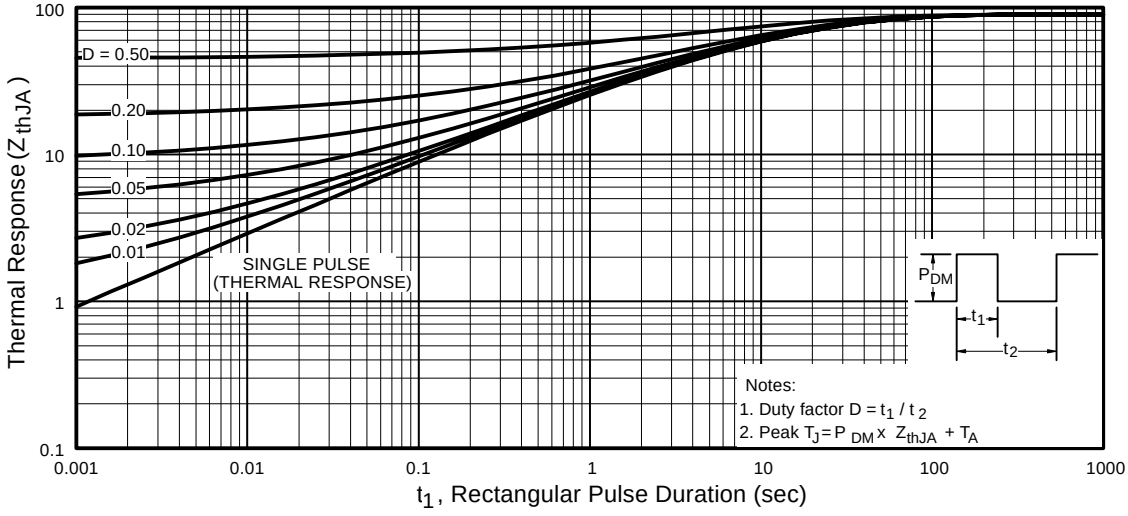


Fig 25. Maximum Effective Transient Thermal Impedance, Junction-to-Case

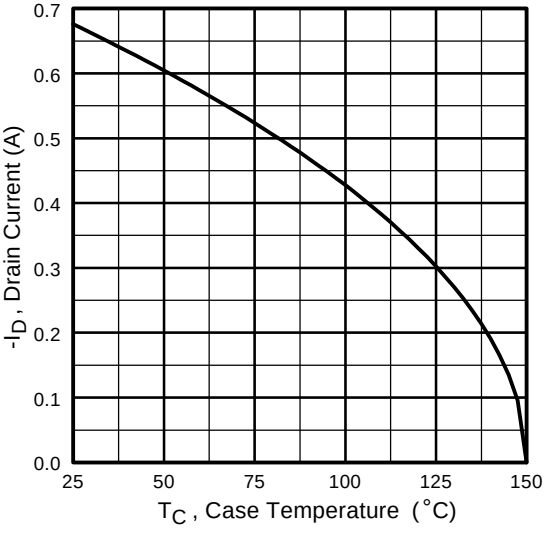


Fig 26. Maximum Drain Current Vs. Case Temperature

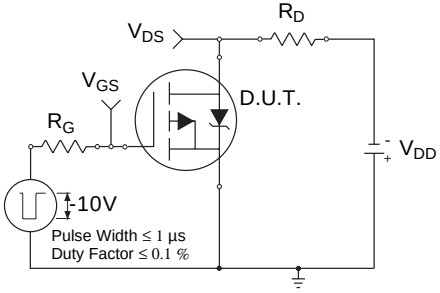


Fig 27a. Switching Time Test Circuit

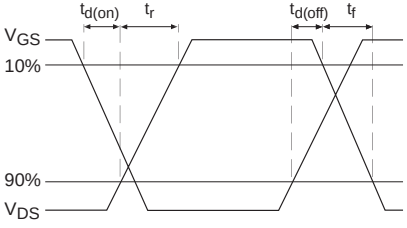


Fig 27b. Switching Time Waveforms

IRFG5210 Device

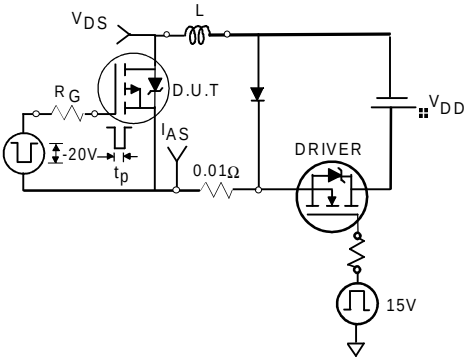


Fig 28a. Unclamped Inductive Test Circuit

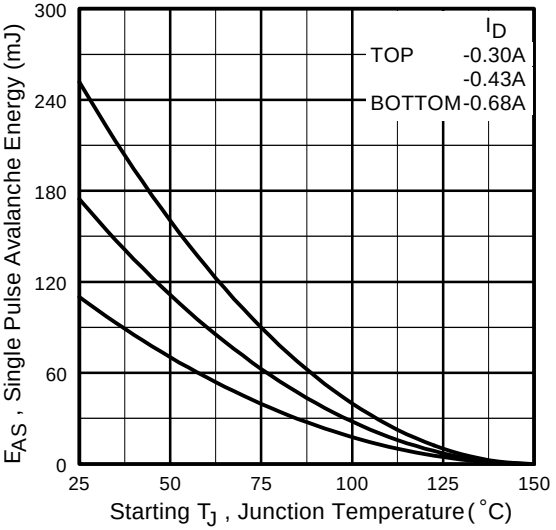


Fig 28c. Maximum Avalanche Energy Vs. Drain Current

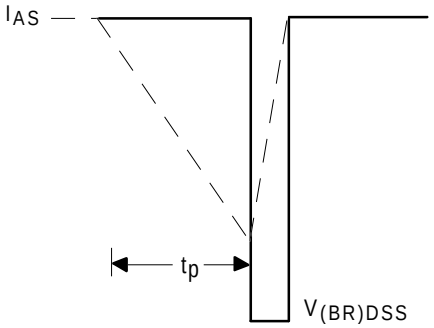
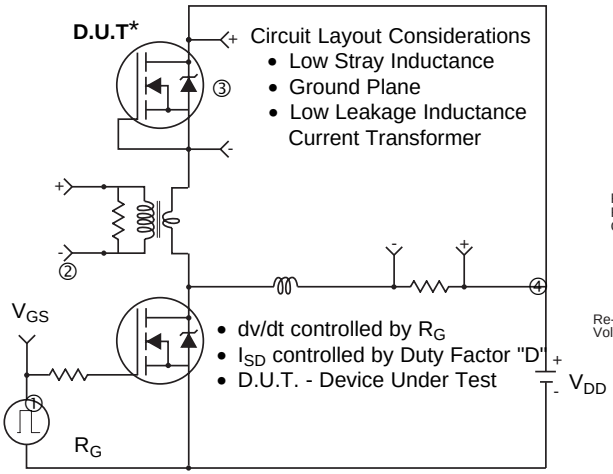
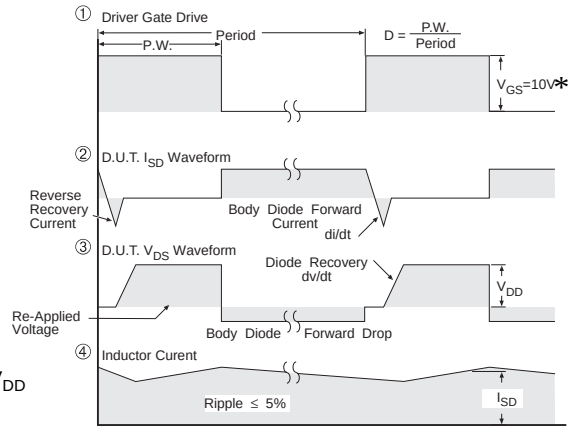


Fig 28b. Unclamped Inductive Waveforms



* Reverse Polarity of D.U.T for P-Channel



*** V_{GS} = 5.0V for Logic Level and 3V Drive Devices

Fig. 29. - Peak Diode Recovery dv/dt Test Circuit

IRFG5210 Device

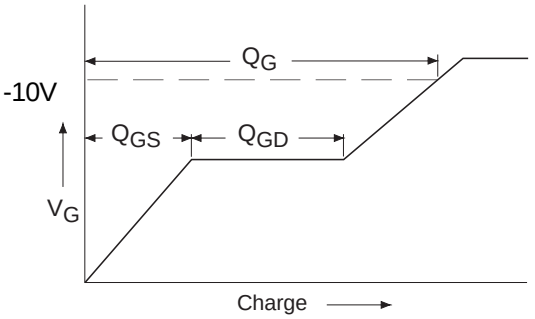


Fig 30a. Basic Gate Charge Waveform

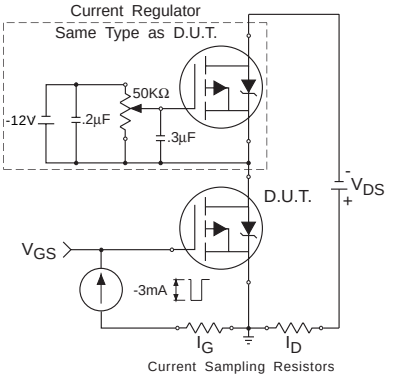
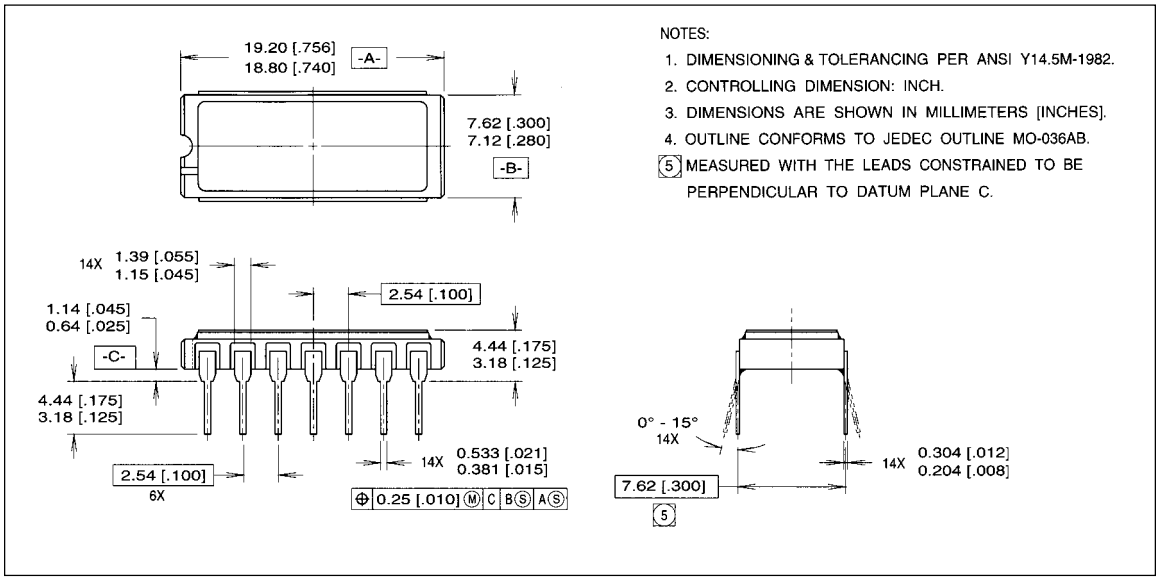


Fig 30b. Gate Charge Test Circuit

Case Outline and Dimensions — MO-036AB



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IOR Rectifier

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