

International

Rectifier

REPETITIVE AVALANCHE AND dv/dt RATED

HEXFET® TRANSISTOR

Provisional Data Sheet No. PD - 9.1716

IRFE9130

JANTX2N6849U

JANTXV2N6849U

JANS2N6849U

[REF:MIL-PRF-19500/564]

P-CHANNEL

-100Volt, 0.30Ω, HEXFET

The leadless chip carrier (LCC) package represents the logical next step in the continual evolution of surface mount technology. The LCC provides designers the extra flexibility they need to increase circuit board density. International Rectifier has engineered the LCC package to meet the specific needs of the power market by increasing the size of the bottom source pad, thereby enhancing the thermal and electrical performance. The lid of the package is grounded to the source to reduce RF interference.

HEXFET transistors also feature all of the well-established advantages of MOSFETs, such as voltage control, very fast switching, ease of paralleling and electrical parameter temperature stability. They are well-suited for applications such as switching power supplies, motor controls, inverters, choppers, audio amplifiers and high-energy pulse circuits, and virtually any application where high reliability is required.

Product Summary

Part Number	BV _{DSS}	R _{DS(on)}	I _D
IRFE9130	-100V	0.30Ω	-6.5A

Features:

- Hermetically Sealed
- Simple Drive Requirements
- Ease of Paralleling
- Small footprint
- Surface Mount
- Lightweight

Absolute Maximum Ratings

	Parameter	IRFE9130, JANTX-, JANTXV-, JANS-, 2N6849	Units
I _D @ V _{GS} = -10V, T _C = 25°C	Continuous Drain Current	-6.5	A
I _D @ V _{GS} = -10V, T _C = 100°C	Continuous Drain Current	-4.1	
I _{DM}	Pulsed Drain Current ①	25	
P _D @ T _C = 25°C	Max. Power Dissipation	25	W
	Linear Derating Factor	0.20	W/K ⑤
V _{GS}	Gate-to-Source Voltage	±20	V
E _{AS}	Single Pulse Avalanche Energy ②	165	mJ
dv/dt	Peak Diode Recovery dv/dt ③	-30	V/ns
T _J	Operating Junction	-55 to 150	°C
T _{STG}	Storage Temperature Range		
	Surface Temperature	300 (for 5 seconds)	
	Weight	0.42 (typical)	g

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Electrical Characteristics @ T_j = 25°C (Unless Otherwise Specified)

	Parameter	Min	Typ	Max	Units	Test Conditions
BV _{DSS}	Drain-to-Source Breakdown Voltage	-100	—	—	V	V _{GS} = 0 V, I _D = -1.0mA
ΔBV _{DSS} /ΔT _j	Temperature Coefficient of Breakdown Voltage	—	-0.10	—	V/°C	Reference to 25°C, I _D = -1.0mA
R _{DS(on)}	Static Drain-to-Source On-State Resistance	—	—	0.30	Ω	V _{GS} = -10V, I _D = -4.1A ④
		—	—	0.345		V _{GS} = -10V, I _D = -6.5A
V _{GS(th)}	Gate Threshold Voltage	-2.0	—	-4.0	V	V _{DS} = V _{GS} , I _D = -250μA
g _{fs}	Forward Transconductance	1.9	—	—	S (r)	V _{DS} > 15V, I _{DS} = -4.1A ④
I _{DSS}	Zero Gate Voltage Drain Current	—	—	-25	μA	V _{DS} = 0.8 x Max Rating, V _{GS} = 0V
		—	—	-250		V _{DS} = 0.8 x Max Rating V _{GS} = 0V, T _j = 125°C
I _{GSS}	Gate-to-Source Leakage Forward	—	—	100	nA	V _{GS} = 20 V
I _{GSS}	Gate-to-Source Leakage Reverse	—	—	-100		V _{GS} = -20V
Q _g	Total Gate Charge	—	—	35	nC	V _{GS} = -10V, I _D = -6.5A
Q _{gs}	Gate-to-Source Charge	—	—	6.8		V _{DS} = Max Rating x 0.5
Q _{gd}	Gate-to-Drain ('Miller') Charge	—	—	23		
t _{d(on)}	Turn-On Delay Time	—	—	60	ns	V _{DD} = -50V, I _D = -6.5A, R _G = 7.5Ω
t _r	Rise Time	—	—	140		
t _{d(off)}	Turn-Off Delay Time	—	—	140		
t _f	Fall Time	—	—	140		
L _D	Internal Drain Inductance	—	1.8	—	nH	Measured from drain pad to die.
L _S	Internal Source Inductance	—	4.3	—		Measured from center of source pad to the end of source bonding wire.
						Modified MOSFET symbol showing the internal inductances.
C _{iss}	Input Capacitance	—	790	—	pF	V _{GS} = 0V, V _{DS} = -25 V f = 1.0MHz
C _{oss}	Output Capacitance	—	340	—		
Cr _{ss}	Reverse Transfer Capacitance	—	71	—		

Source-Drain Diode Ratings and Characteristics

	Parameter	Min	Typ	Max	Units	Test Conditions
I _S	Continuous Source Current (Body Diode)	—	—	-6.5	A	Modified MOSFET symbol showing the integral reverse p-n junction rectifier. 
I _{SM}	Pulse Source Current (Body Diode) ①	—	—	-25		
V _{SD}	Diode Forward Voltage	—	—	-4.3	V	T _J = 25°C, I _S = -6.5A, V _{GS} = 0V ④
t _{rr}	Reverse Recovery Time	—	—	250	ns	T _J = 25°C, I _F = -6.5A, di/dt ≤ -100A/μs V _{DD} ≤ -50V ④
Q _{RR}	Reverse Recovery Charge	—	—	3.0	μC	
t _{on}	Forward Turn-On Time	Intrinsic turn-on time is negligible. Turn-on speed is substantially controlled by L _S + L _D .				

Thermal Resistance

	Parameter	Min	Typ	Max	Units	Test Conditions
R _{thJC}	Junction-to-Case	—	—	5.0	K/W ⑤	
R _{thJPCB}	Junction-to-PC Board	—	—	19		Soldered to a copper clad PC board

Details of notes ① through ⑤ are on the last page

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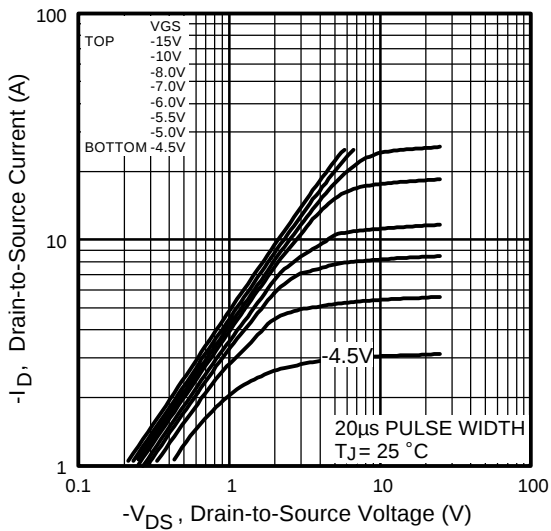


Fig 1. Typical Output Characteristics

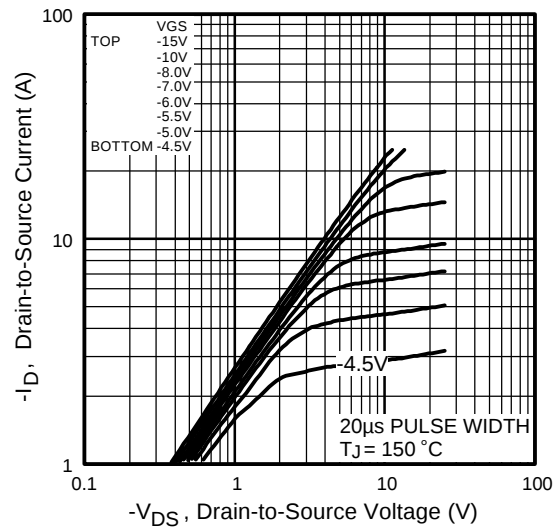


Fig 2. Typical Output Characteristics

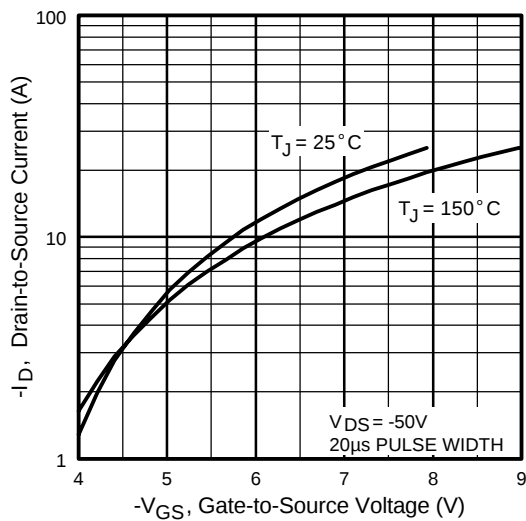


Fig 3. Typical Transfer Characteristics

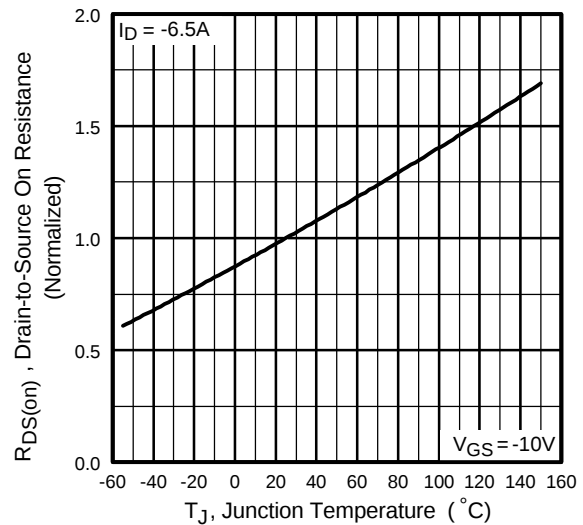


Fig 4. Normalized On-Resistance Vs. Temperature

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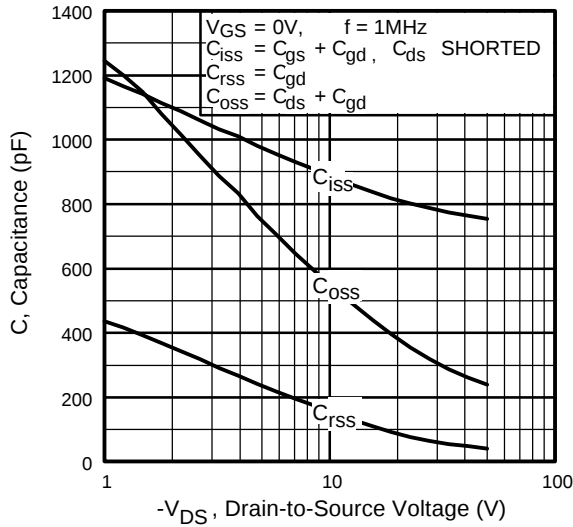


Fig 5. Typical Capacitance Vs. Drain-to-Source Voltage

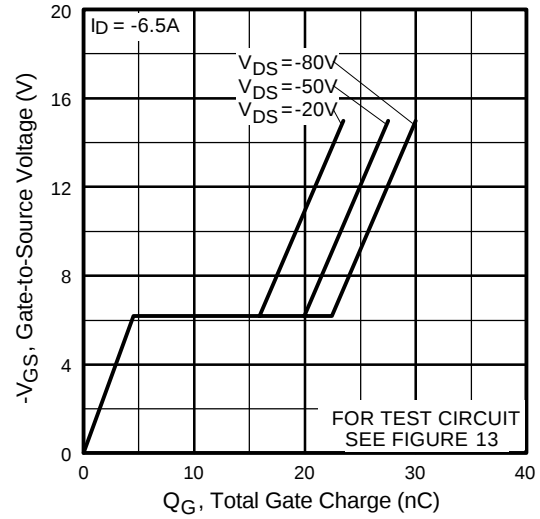


Fig 6. Typical Gate Charge Vs. Gate-to-Source Voltage

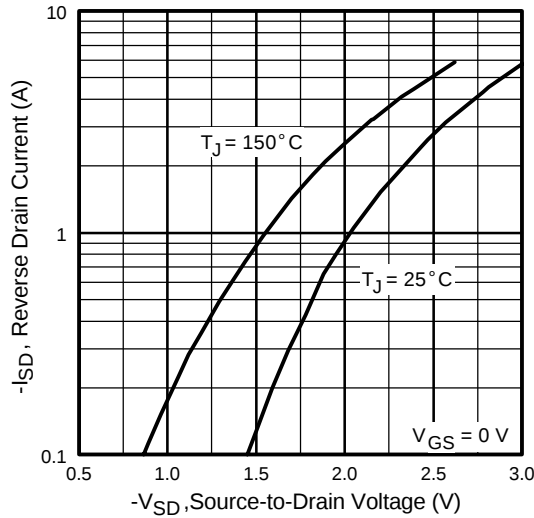


Fig 7. Typical Source-Drain Diode Forward Voltage

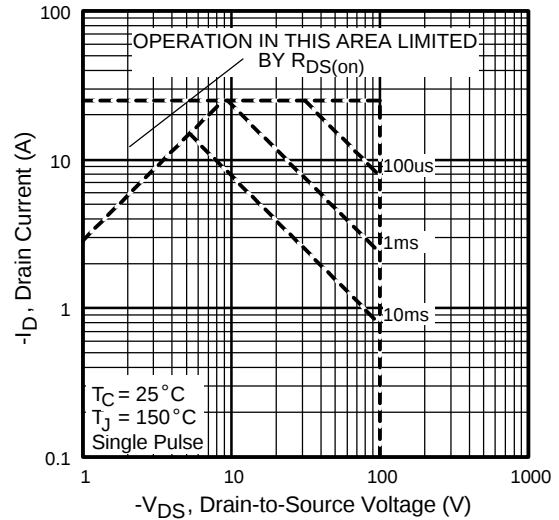


Fig 8. Maximum Safe Operating Area

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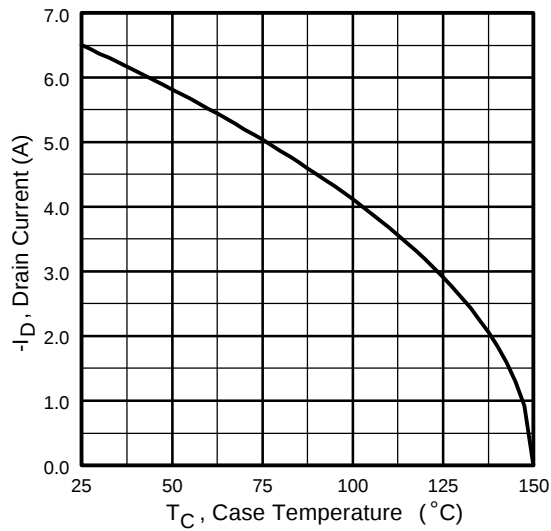


Fig 9. Maximum Drain Current Vs. Case Temperature

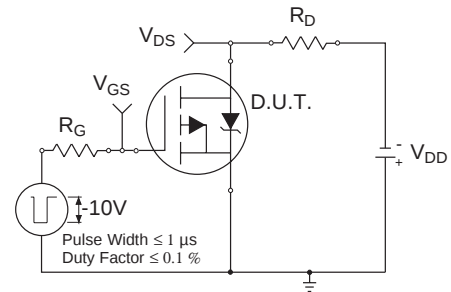


Fig 10a. Switching Time Test Circuit

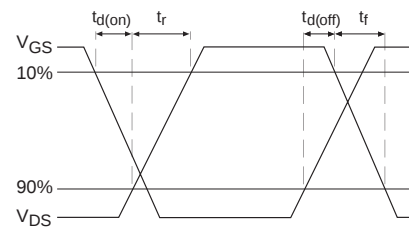


Fig 10b. Switching Time Waveforms

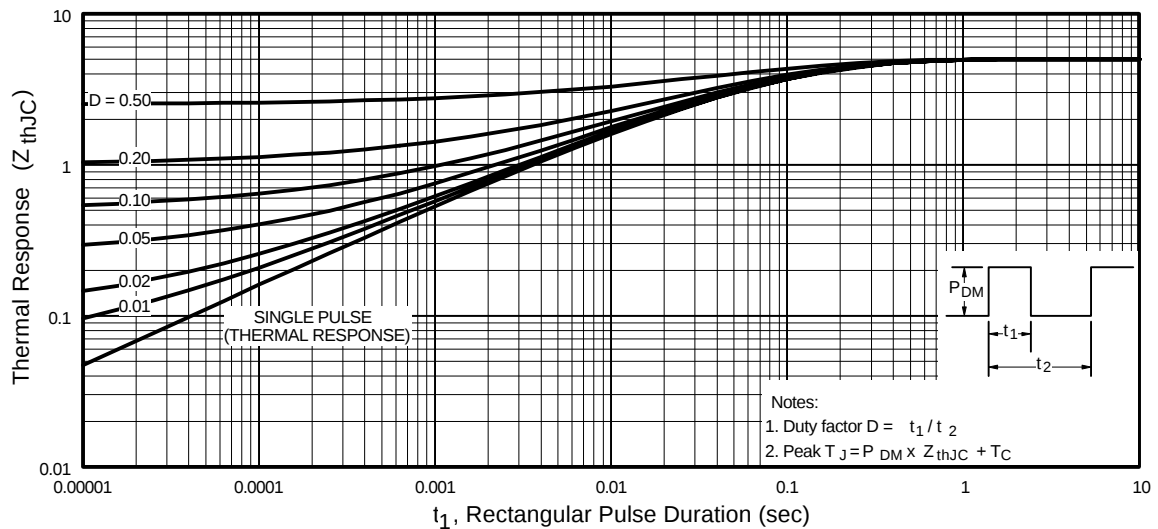


Fig 11. Maximum Effective Transient Thermal Impedance, Junction-to-Case

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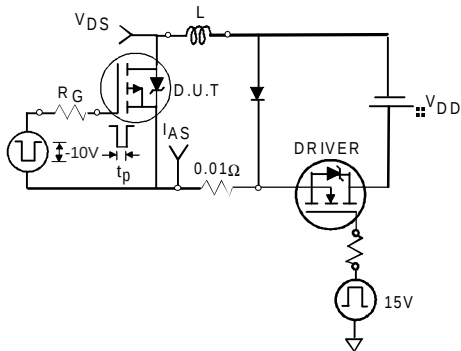


Fig 12a. Unclamped Inductive Test Circuit

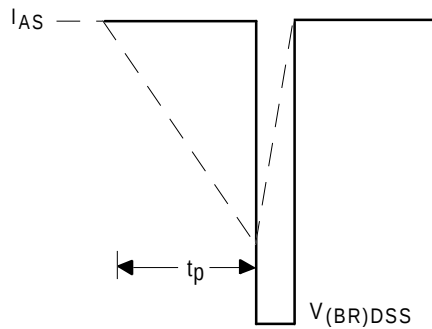


Fig 12b. Unclamped Inductive Waveforms

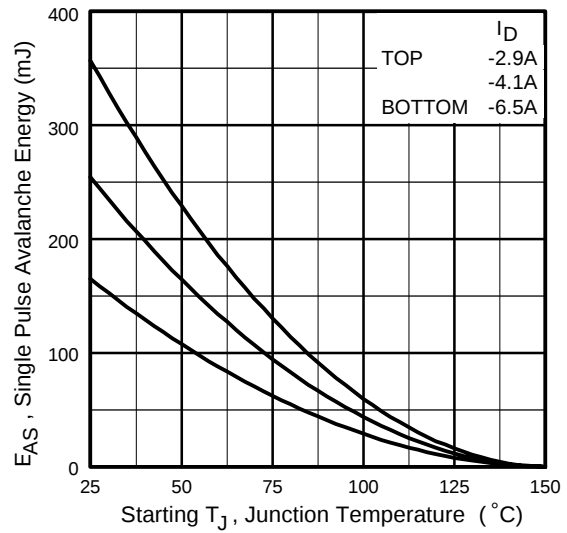


Fig 12c. Maximum Avalanche Energy Vs. Drain Current

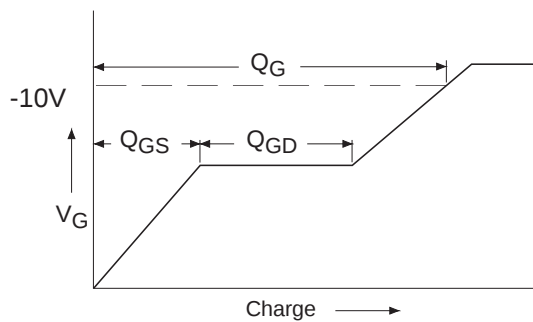


Fig 13a. Basic Gate Charge Waveform

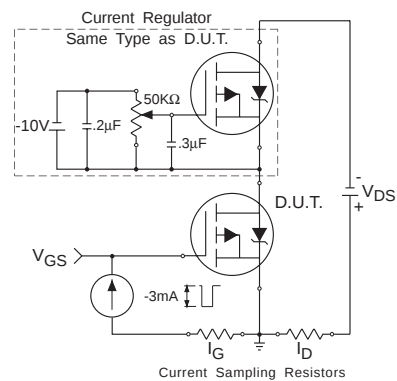
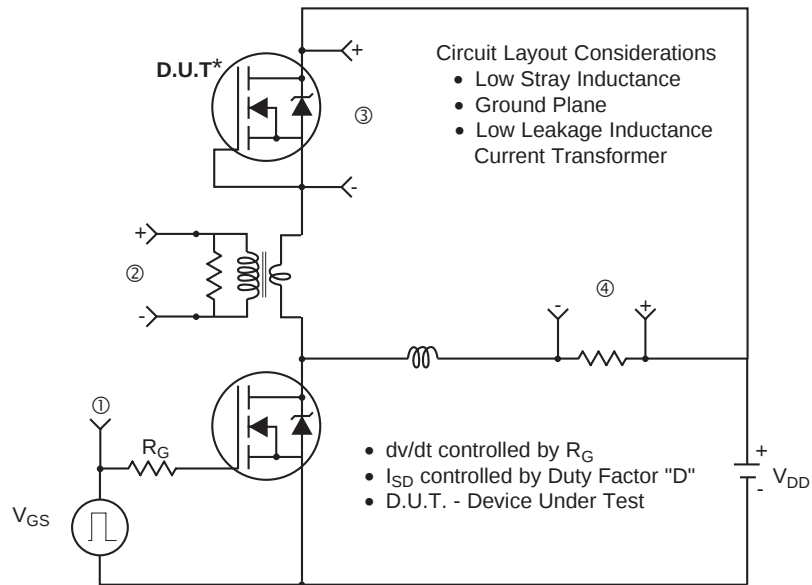


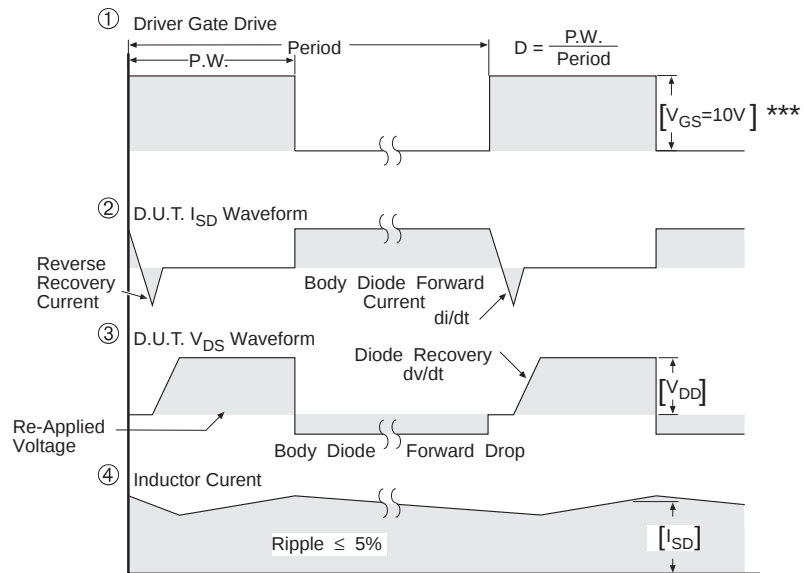
Fig 13b. Gate Charge Test Circuit

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Peak Diode Recovery dv/dt Test Circuit



* Reverse Polarity of D.U.T for P-Channel



*** $V_{GS} = 5.0V$ for Logic Level and 3V Drive Devices

Fig 14. For P-Channel HEXFETS

