International Rectifier

Provisional Data Sheet No. PD - 9.1666A

# IRFE130
# JANTX2N6796U
# JANTXV2N6796U
# [REF:MIL-PRF-19500/557]

**REPETITIVE AVALANCHE AND dv/dt RATED**
**HEXFET® TRANSISTOR**

N-CHANNEL

### 100Volt, 0.18Ω, HEXFET

The leadless chip carrier (LCC) package represents the logical next step in the continual evolution of surface mount technology. The LCC provides designers the extra flexibility they need to increase circuit board density. International Rectifier has engineered the LCC package to meet the specific needs of the power market by increasing the size of the bottom source pad, thereby enhancing the thermal and electrical performance. The lid of the package is grounded to the source to reduce RF interference.

HEXFET transistors also feature all of the well-established advantages of MOSFETs, such as voltage control, very fast switching, ease of paralleling and electrical parameter temperature stability. They are well-suited for applications such as switching power supplies, motor controls, inverters, choppers, audio amplifiers and high-energy pulse circuits, and virtually any application where high reliability is required.

### Product Summary

| Part Number | $BV_{DSS}$ | $R_{DS(on)}$ | $I_D$ |
|---|---|---|---|
| IRFE130 | 100V | 0.18Ω | 8.0A |

### Features:

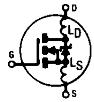
- Hermetically Sealed
- Simple Drive Requirements
- Ease of Paralleling
- Small footprint
- Surface Mount
- Lightweight

## Absolute Maximum Ratings

| | Parameter | IRFE130, JANTX-, JANTXV-, 2N6796U | Units |
|---|---|---|---|
| $I_D$ @ $V_{GS}$ = 10V, $T_C$ = 25°C | Continuous Drain Current | 8.0 | A |
| $I_D$ @ $V_{GS}$ = 10V, $T_C$ = 100°C | Continuous Drain Current | 5.0 | |
| $I_{DM}$ | Pulsed Drain Current ① | 32 | |
| $P_D$ @ $T_C$ = 25°C | Max. Power Dissipation | 25 | W |
| | Linear Derating Factor | 0.17 | W/K ⑤ |
| $V_{GS}$ | Gate-to-Source Voltage | ±20 | V |
| $E_{AS}$ | Single Pulse Avalanche Energy ② | 134 | mJ |
| dv/dt | Peak Diode Recovery dv/dt ③ | 8.3 | V/ns |
| $T_J$<br>$T_{STG}$ | Operating Junction<br>Storage Temperature Range | -55 to 150 | °C |
| | Surface Temperature | 300 ( for 5 seconds) | |
| | Weight | 0.42 (typical) | g |

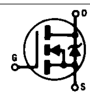
## IRFE130, JANTX-, JANTXV-, 2N6796U Device

## Electrical Characteristics @ $T_j$ = 25°C (Unless Otherwise Specified)

| | Parameter | Min | Typ | Max | Units | Test Conditions |
|---|---|---|---|---|---|---|
| $BV_{DSS}$ | Drain-to-Source Breakdown Voltage | 100 | — | — | V | $V_{GS}$ =0 V, $I_D$ = 1.0mA |
| $\Delta BV_{DSS}/\Delta T_J$ | Temperature Coefficient of Breakdown Voltage | — | 0.11 | — | V/°C | Reference to 25°C, $I_D$ = 1.0mA |
| $R_{DS(on)}$ | Static Drain-to-Source | — | — | 0.18 | Ω | $V_{GS}$ = 10V, $I_D$ = 5.0A ④ |
| | On-State Resistance | — | — | 0.207 | | $V_{GS}$ = 10V, $I_D$ = 8.0A |
| $V_{GS(th)}$ | Gate Threshold Voltage | 2.0 | — | 4.0 | V | $V_{DS}$ = $V_{GS}$, $I_D$ = 250μA |
| $g_{fs}$ | Forward Transconductance | 3.0 | — | — | S (℧) | $V_{DS}$ > 15V, $I_{DS}$ = 5.0A ④ |
| $I_{DSS}$ | Zero Gate Voltage Drain Current | — | — | 25 | μA | $V_{DS}$= 0.8 x Max Rating,$V_{GS}$=0V |
| | | — | — | 250 | | $V_{DS}$ = 0.8 x Max Rating<br>$V_{GS}$ = 0V, $T_J$ = 125°C |
| $I_{GSS}$ | Gate-to-Source Leakage Forward | — | — | 100 | nA | $V_{GS}$ = 20 V |
| $I_{GSS}$ | Gate-to-Source Leakage Reverse | — | — | -100 | | $V_{GS}$ = -20V |
| $Q_g$ | Total Gate Charge | — | — | 29 | nC | $V_{GS}$ = 10V, $I_D$ = 8.0A<br>$V_{DS}$ = Max Rating x 0.5 |
| $Q_{gs}$ | Gate-to-Source Charge | — | — | 6.5 | | |
| $Q_{gd}$ | Gate-to-Drain (‘Miller’) Charge | — | — | 17 | | |
| $t_{d(on)}$ | Turn-On Delay Time | — | — | 30 | ns | $V_{DD}$ = 50V, $I_D$ = 8.0A,<br>$R_G$ = 7.5Ω |
| $t_r$ | Rise Time | — | — | 75 | | |
| $t_{d(off)}$ | Turn-Off Delay Time | — | — | 40 | | |
| $t_f$ | Fall Time | — | — | 45 | | |
| $L_D$ | Internal Drain Inductance | — | 1.8 | — | nH | Measured from drain pad to die. / Modified MOSFET symbol showing the internal inductances.  |
| $L_S$ | Internal Source Inductance | — | 4.3 | — | | Measured from center of source pad to the end of source bonding wire. |
| $C_{iss}$ | Input Capacitance | — | 660 | — | pF | $V_{GS}$ = 0V, $V_{DS}$ = 25 V<br>f = 1.0MHz |
| $C_{oss}$ | Output Capacitance | — | 260 | — | | |
| $C_{rss}$ | Reverse Transfer Capacitance | — | 51 | — | | |



## Source-Drain Diode Ratings and Characteristics

| | Parameter | Min | Typ | Max | Units | Test Conditions |
|---|---|---|---|---|---|---|
| $I_S$ | Continuous Source Current (Body Diode) | — | — | 8.0 | A | Modified MOSFET symbol showing the integral reverse p-n junction rectifier.  |
| $I_{SM}$ | Pulse Source Current (Body Diode) ① | — | — | 32 | | |
| $V_{SD}$ | Diode Forward Voltage | — | — | 1.5 | V | $T_j$ = 25°C, $I_S$ = 8.0A, $V_{GS}$ = 0V ④ |
| $t_{rr}$ | Reverse Recovery Time | — | — | 300 | ns | $T_j$ = 25°C, $I_F$ = 8.0A, di/dt ≤ 100A/μs<br>$V_{DD}$ ≤ 50V ④ |
| $Q_{RR}$ | Reverse Recovery Charge | — | — | 970 | nC | |
| $t_{on}$ | Forward Turn-On Time | Intrinsic turn-on time is negligible. Turn-on speed is substantially controlled by $L_S$ + $L_D$. | | | | |



## Thermal Resistance

| | Parameter | Min | Typ | Max | Units | Test Conditions |
|---|---|---|---|---|---|---|
| $R_{thJC}$ | Junction-to-Case | — | — | 5.0 | K/W ⑤ | |
| $R_{thJPCB}$ | Junction-to-PC Board | — | — | 19 | | Soldered to a copper clad PC board |

Details of notes ① through ⑤ are on the last page

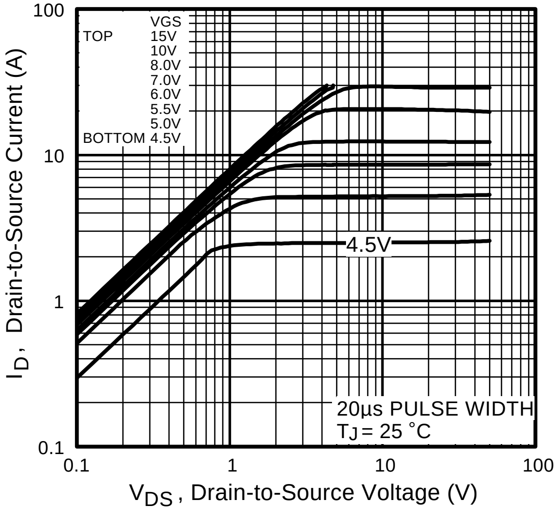



**Fig 1.** Typical Output Characteristics

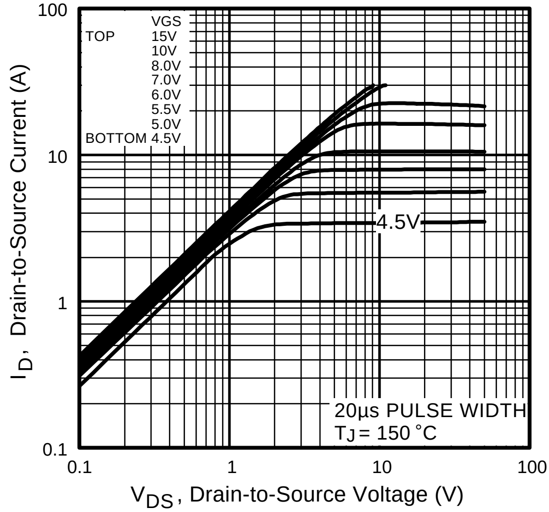



**Fig 2.** Typical Output Characteristics

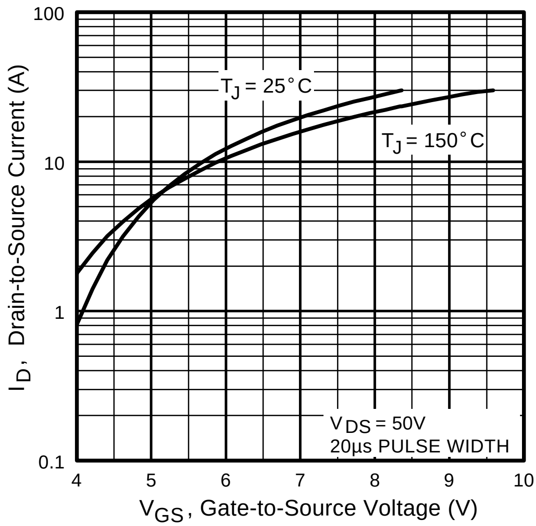



**Fig 3.** Typical Transfer Characteristics

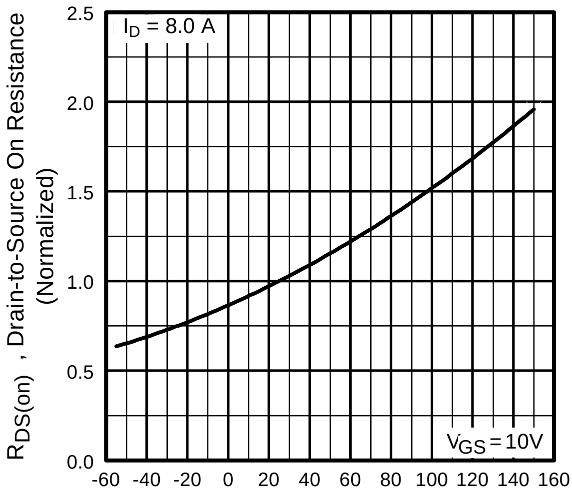



**Fig 4.** Normalized On-Resistance Vs. Temperature

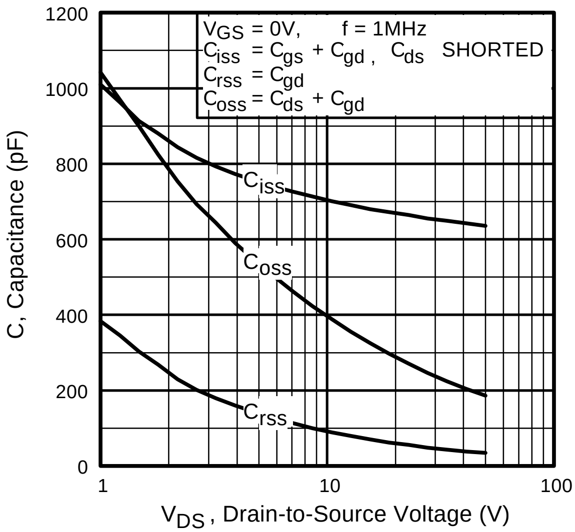



**Fig 5.** Typical Capacitance Vs. Drain-to-Source Voltage

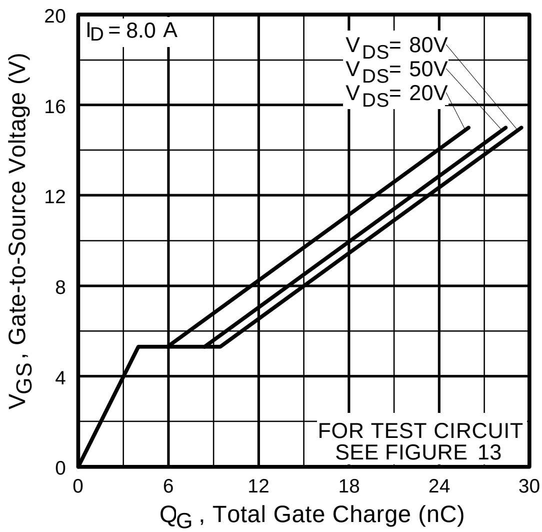



**Fig 6.** Typical Gate Charge Vs. Gate-to-Source Voltage

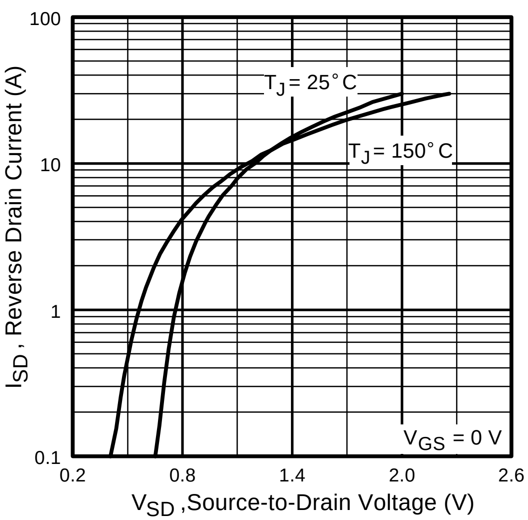



**Fig 7.** Typical Source-Drain Diode Forward Voltage

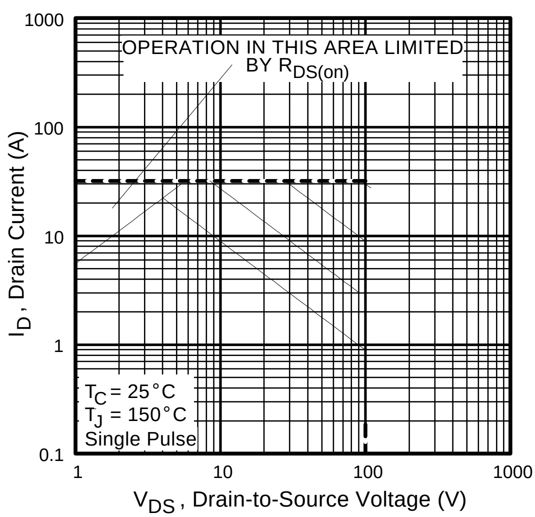



**Fig 8.** Maximum Safe Operating Area

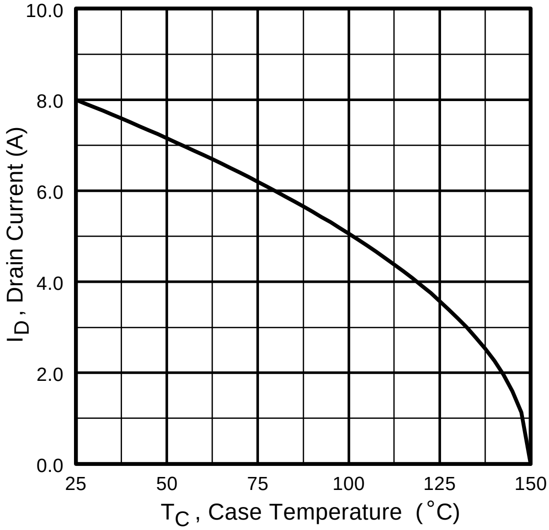



**Fig 9.** Maximum Drain Current Vs. Case Temperature

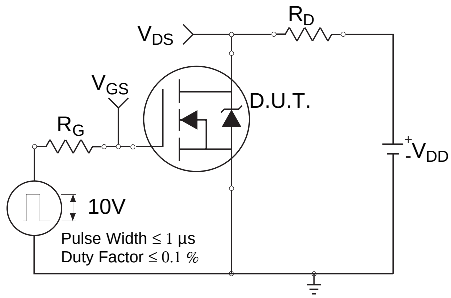



**Fig 10a.** Switching Time Test Circuit

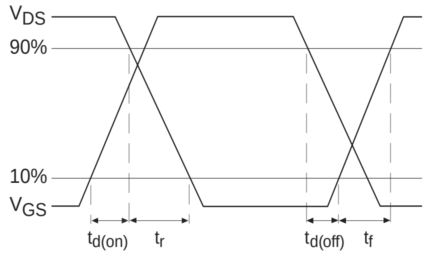



**Fig 10b.** Switching Time Waveforms

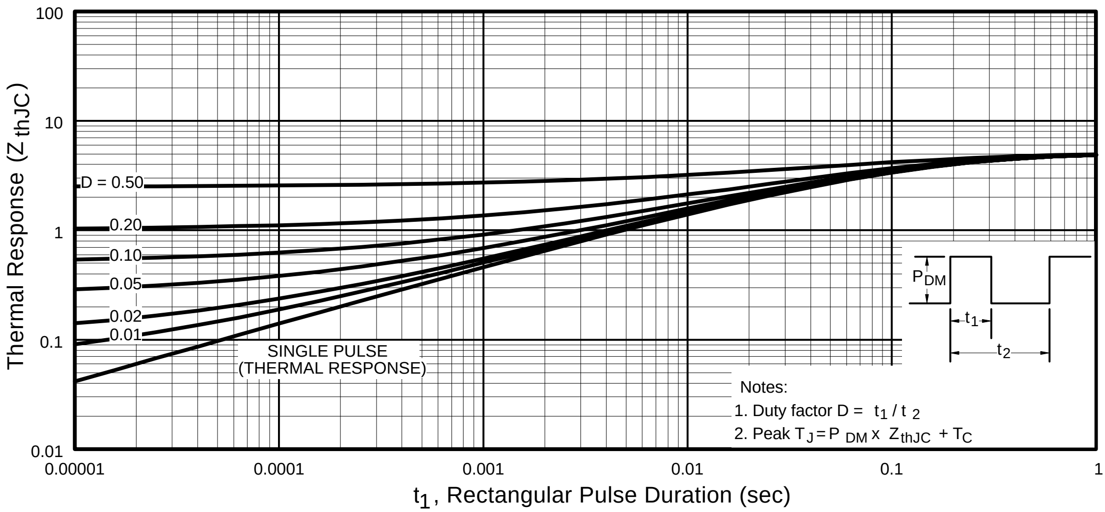



**Fig 11.** Maximum Effective Transient Thermal Impedance, Junction-to-Case

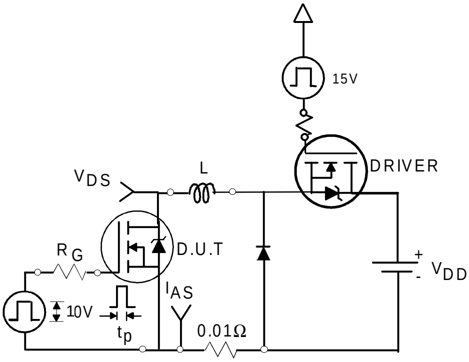



**Fig 12a.** Unclamped Inductive Test Circuit

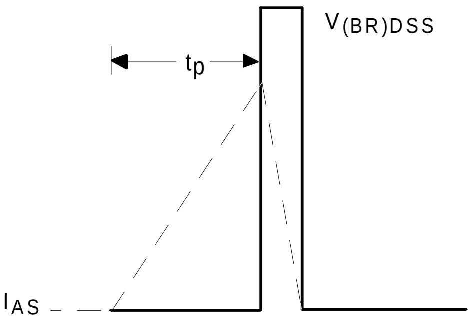



**Fig 12b.** Unclamped Inductive Waveforms

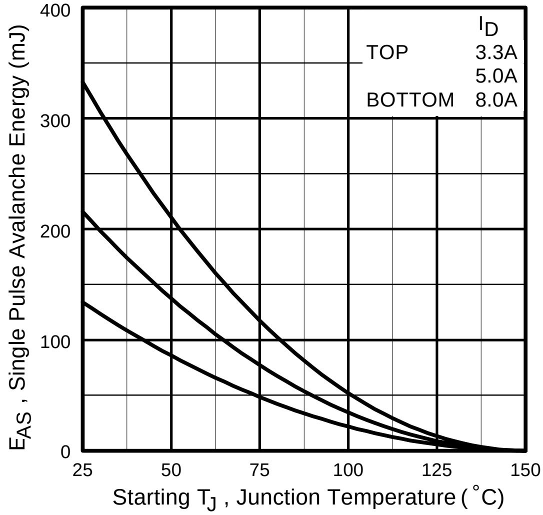



**Fig 12c.** Maximum Avalanche Energy Vs. Drain Current

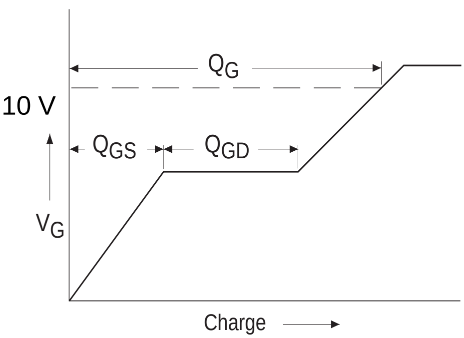



**Fig 13a.** Basic Gate Charge Waveform

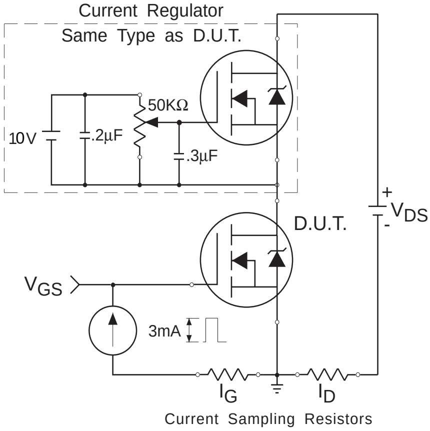
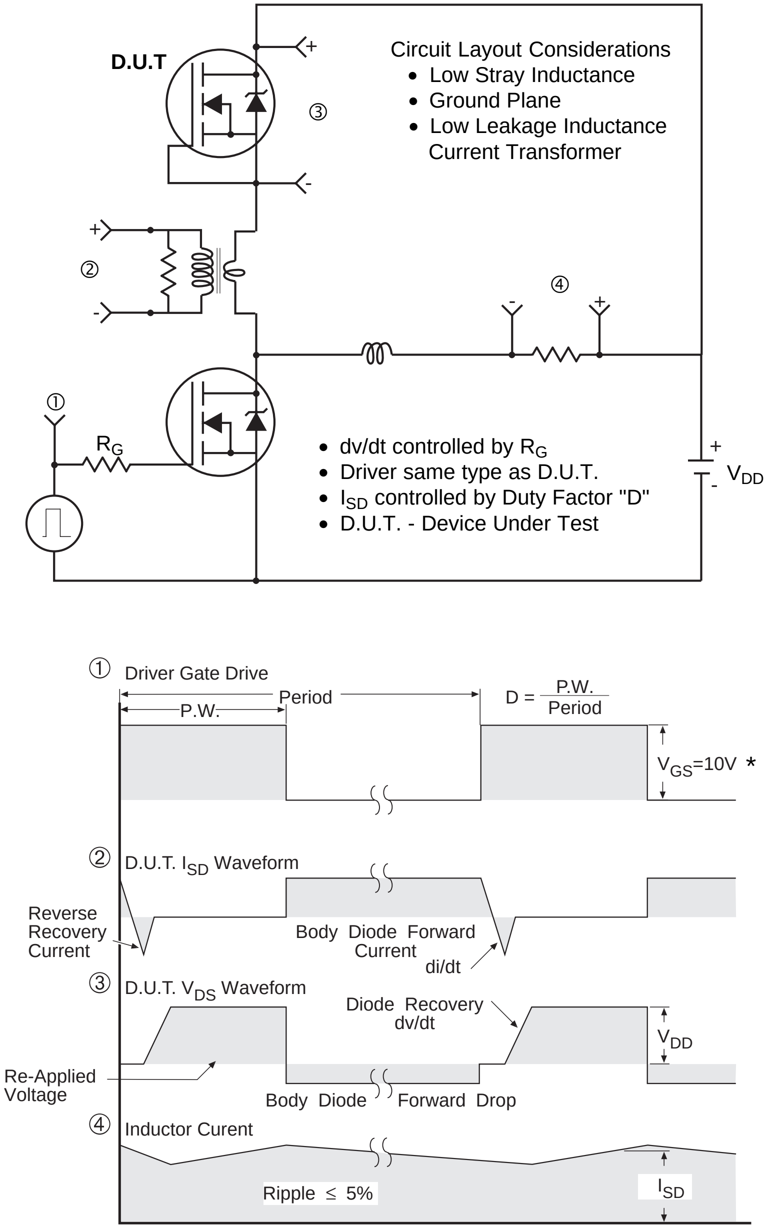



**Fig 13b.** Gate Charge Test Circuit

## Peak Diode Recovery dv/dt Test Circuit




* $V_{GS}$ = 5V for Logic Level Devices

**Fig 14.** For N-Channel HEXFETS

Notes:

① Repetitive Rating; Pulse width limited by maximum junction temperature. Refer to current HEXFET reliability report.

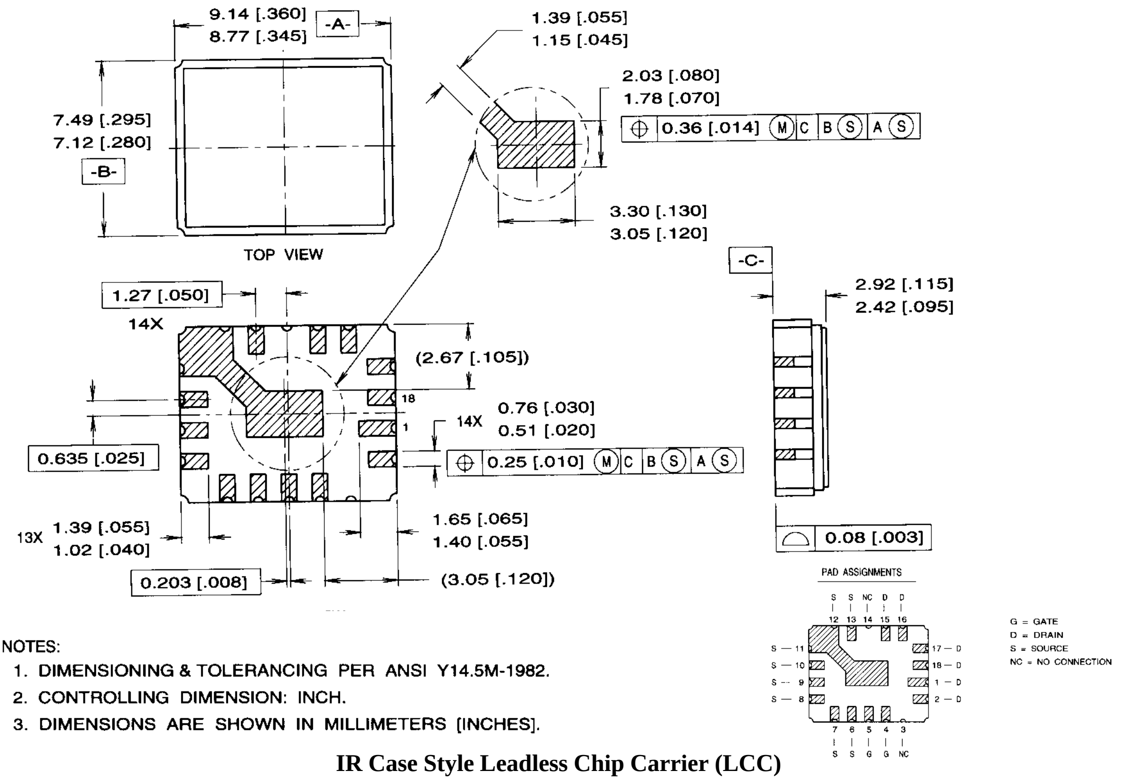
② @ $V_{DD}$ = 50 V, Starting $T_J$ = 25°C, $E_{AS} = [0.5 * L * (I_L^2)]$ Peak $I_L$ = 8.0A, $V_{GS}$ =10 V, 25 ≤ $R_G$ ≤ 200Ω

③ $I_{SD}$ ≤ 8.0A, di/dt ≤ 480 A/µs, $V_{DD} \leq BV_{DSS}$, $T_J$ ≤ 150°C Suggested $R_G$ = 2.35Ω

④ Pulse width ≤ 300 µs; Duty Cycle ≤ 2%

⑤ K/W = °C/W

## Case Outline and Dimensions — Leadless Chip Carrier (LCC) Package




NOTES:
1. DIMENSIONING & TOLERANCING PER ANSI Y14.5M-1982.
2. CONTROLLING DIMENSION: INCH.
3. DIMENSIONS ARE SHOWN IN MILLIMETERS [INCHES].

**IR Case Style Leadless Chip Carrier (LCC)**

International
IOR Rectifier

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